

1200 V Motion SPM[®] 2 Series

FNA25012A

General Description

The FNA25012A is a Motion SPM[®] 2 module providing a fully-featured, high-performance inverter output stage for AC induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features: under-voltage lockouts, over-current shutdown, temperature sensing, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to high-voltage, high-current drive signals to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

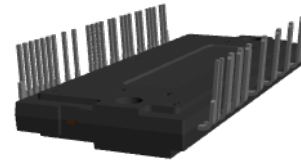
- 1200 V – 50 A 3-Phase IGBT Inverter, Including Control Ics for Gate Drive and Protections
- Low-Loss, Short-Circuit-Rated IGBTs
- Very Low Thermal Resistance Using AlN DBC Substrate
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply Supported
- Built-In NTC Thermistor for Temperature Monitoring and Management
- Adjustable Over-Current Protection via Integrated Sense-IGBTs
- Isolation Rating of 2500 Vrms/1 min.

Applications

- Motion Control – Industrial Motor (AC 400 V Class)

Related Resources

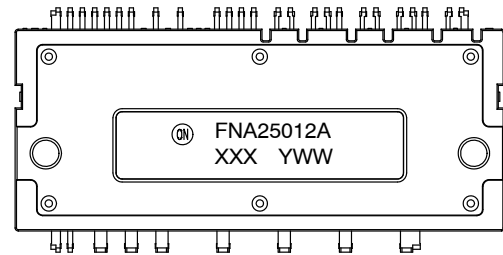
- [AN9075](#) – Users Guide for 1200 V SPM[®] 2 Series
- [AN9076](#) – Mounting Guide for New SPM[®] 2 Package
- [AN9079](#) – Thermal Performance of 1200 V Motion SPM[®] 2 Series by Mounting Torque



SPMCA-A34/34 LD, PDD STD, DBC DIP TYPE
CASE MODFQ

Figure 1. 3D Package Drawing
(Click to Activate 3D Content)

MARKING DIAGRAM



FNA25012A	= Specific Device Code
XXX	= Lot Code
YWW	= Work Week Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FNA25012A

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Packing Type	Quantity
FNA25012A	FNA25012A	SPMCB-A34	Rail	6

Integrated Power Functions

- 1200 V – 50 A IGBT inverter for three-phase DC/AC power conversion (Refer to Figure 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate-drive circuit, high-voltage isolated high-speed level shifting control circuit, Under-Voltage Lock-Out Protection (UVLO), Available bootstrap circuit example is given in Figures 5 and 15
- For inverter low-side IGBTs: gate-drive circuit, Short-Circuit Protection (SCP) control circuit, Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling: corresponding to UV (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3/5 V logic, Schmitt-trigger input

PIN CONFIGURATION

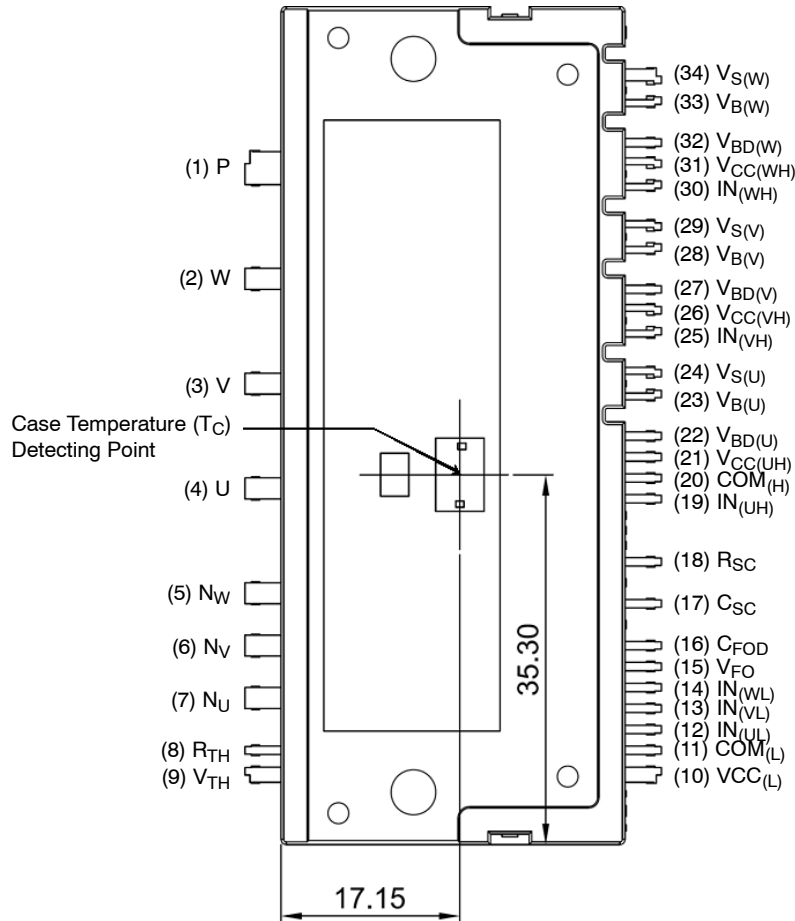


Figure 2. Top View

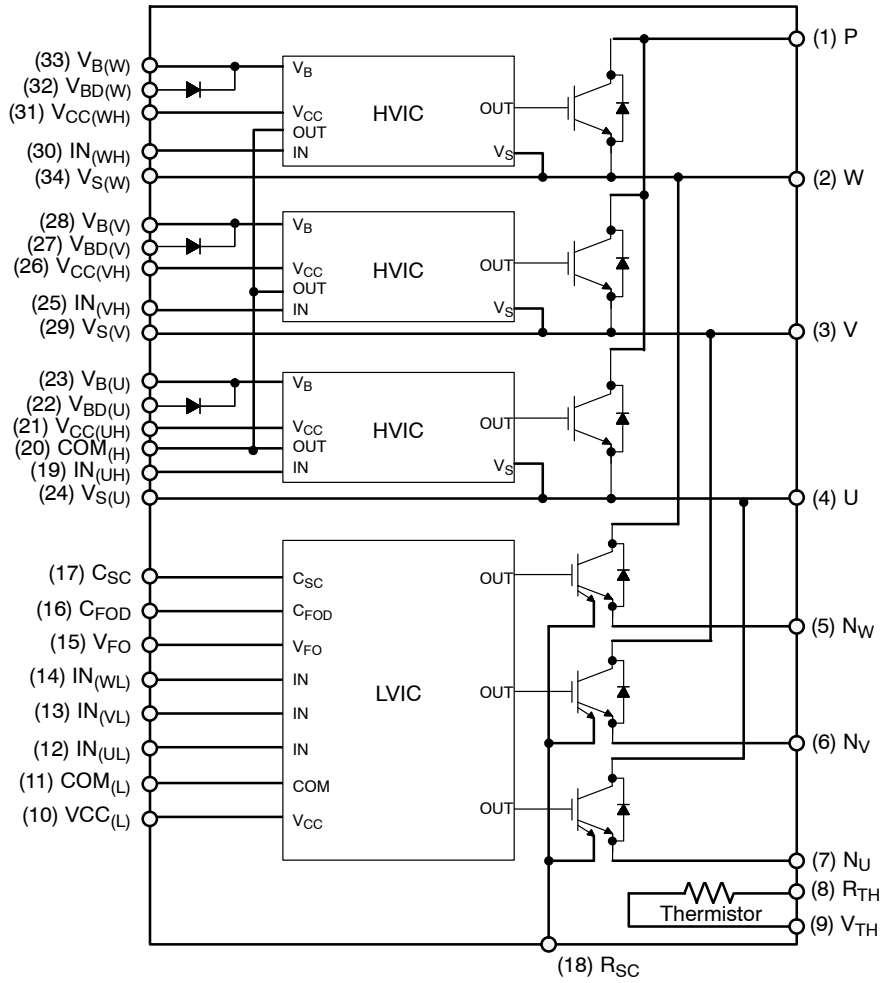
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PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	P ₊	Positive DC-Link Input
2	W	Output for W-Phase
3	V	Output for V-Phase
4	U	Output for U-Phase
5	N _W	Negative DC-Link Input for W-Phase
6	N _V	Negative DC-Link Input for V-Phase
7	N _U	Negative DC-Link Input for U-Phase
8	R _{TH}	Series Resistor for Thermistor (Temperature Detection)
9	V _{TH}	Thermistor Bias Voltage
10	V _{CC(L)}	Low-Side Bias Voltage for IC and IGBTs Driving
11	COM _(L)	Low-Side Common Supply Ground
12	IN _(UL)	Signal Input for High-Side U-Phase
13	IN _(VL)	Signal Input for High-Side V-Phase
14	IN _(WL)	Signal Input for High-Side W-Phase
15	V _{FO}	Fault Output
16	C _{FOD}	Capacitor for Fault Output Duration Selection
17	C _{SC}	Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input
18	R _{SC}	Resistor for Short-Circuit Current Detection
19	IN _(UH)	Signal Input for High-Side U Phase
20	COM _(H)	High-Side Common Supply Ground
21	V _{CC(UH)}	High-Side Bias Voltage for U Phase IC
22	V _{BD(U)}	Anode of Bootstrap Diode for U Phase High-Side Bootstrap Circuit
23	V _{B(U)}	High-Side Bias Voltage for U Phase IGBT Driving
24	V _{S(U)}	High-Side Bias Voltage Ground for U Phase IGBT Driving
25	IN _(VH)	Signal Input for High-Side V Phase
26	V _{CC(VH)}	High-Side Bias Voltage for V Phase IC
27	V _{BD(V)}	Anode of Bootstrap Diode for V Phase High-Side Bootstrap Circuit
28	V _{B(V)}	High-Side Bias Voltage for V Phase IGBT Driving
29	V _{S(V)}	High-Side Bias Voltage Ground for V Phase IGBT Driving
30	IN _(WH)	Signal Input for High-Side W Phase
31	V _{CC(WH)}	High-Side Bias Voltage for W Phase IC
32	V _{BD(W)}	Anode of Bootstrap Diode for W Phase High-Side Bootstrap Circuit
33	V _{B(W)}	High-Side Bias Voltage for W Phase IGBT Driving
34	V _{S(W)}	High-Side Bias Voltage Ground for W Phase IGBT Driving

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INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTES:

1. Inverter high-side is composed of three normal-IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three sense-IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Figure 3. Internal Block Diagram

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ABSOLUTE MAXIMUM RATINGS (T_J = 25°C UNLESS OTHERWISE NOTED)

INVERTER PART

Symbol	Parameter	Conditions	Rating	Unit
V _{PN}	Supply Voltage	Applied between P-N _U , N _V , N _W	900	V
V _{PN(Surge)}	Supply Voltage (Surge)	Applied between P-N _U , N _V , N _W	1000	V
V _{CES}	Collector-Emitter Voltage		1200	V
±I _C	Each IGBT Collector Current	T _C = 25°C, T _J = 150°C (Note 4)	50	A
±I _{CP}	Each IGBT Collector Current (Peak)	T _C = 25°C, T _J = 150°C, Under 1 ms Pulse Width (Note 4)	75	A
P _C	Collector Dissipation	T _C = 25°C per One Chip (Note 4)	347	W
T _J	Operating Junction Temperature		-40~150	°C

CONTROL PART

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Control Supply Voltage	Applied between V _{CC(H)} , V _{CC(L)} -COM	20	V
V _{BS}	High-Side Control Bias Voltage	Applied between V _{B(U)} -V _{S(U)} , V _{B(V)} -V _{S(V)} , V _{B(W)} -V _{S(W)}	20	V
V _{IN}	Input Signal Voltage	Applied between IN _(UH) , IN _(VH) , IN _(WH) , IN _(UL) , IN _(VL) , IN _(WL) -COM	-0.3~V _{CC} +0.3	V
V _{FO}	Fault Output Supply Voltage	Applied between V _{FO} -COM	-0.3~V _{CC} +0.3	V
I _{FO}	Fault Output Current	Sink Current at V _{FO} pin	2	mA
V _{SC}	Current Sensing Input Voltage	Applied between C _{SC} -COM	-0.3~V _{CC} +0.3	V

BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Rating	Unit
V _{RRM}	Maximum Repetitive Reverse Voltage		1200	V
I _F	Forward Current	T _C = 25°C, T _J ≤ 150°C (Note 4)	1.0	A
I _{FP}	Forward Current (Peak)	T _C = 25°C, T _J = 150°C, Under 1 ms Pulse Width (Note 4)	2.0	A
T _J	Operating Junction Temperature		-40~150	°C

TOTAL SYSTEM

Symbol	Parameter	Conditions	Rating	Unit
V _{PN(PROT)}	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	V _{CC} = V _{BS} = 13.5~16.5 V, T _J = 150°C, V _{CES} = < 1200 V, Non-repetitive, < 2 μs	800	V
T _C	Module Case Operation Temperature	See Figure 2	-40~125	°C
T _{STG}	Storage Temperature		-40~125	°C
V _{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V _{rms}

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R _{th(j-c)Q}	Junction to Case Thermal Resistance (Note 5)	Inverter IGBT part (per 1/6 module)	-	-	0.36	°C/W
R _{th(j-c)F}		Inverter FWD part (per 1/6 module)	-	-	0.66	°C/W

4. These values had been made an acquisition by the calculation considered to design factor.
5. For the measurement point of case temperature (T_C), please refer to Figure 2.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED)

INVERTER PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V _{CE(SAT)}	Collector – Emitter Saturation Voltage	V _{DD} = V _{BS} = 15 V, V _{IN} = 5 V, I _C = 50 A, T _J = 25°C	-	2.20	2.80	V	
V _F	FWDi Forward Voltage	V _{IN} = 0 V, I _F = 50 A, T _J = 25°C	-	2.40	3.00	V	
HS	Switching Times	V _{PN} = 600 V, V _{CC} = 15 V, I _C = 50 A, T _J = 25°C V _{IN} = 0 V ↔ 5 V, Inductive Load See Figure 5 (Note 6)	t _{ON}	0.90	1.40	2.00	μs
			t _{C(ON)}	-	0.50	0.95	μs
			t _{OFF}	-	1.10	1.70	μs
			t _{C(OFF)}	-	0.15	0.55	μs
			t _{rr}	-	0.20	-	μs
LS	Switching Times	V _{PN} = 600 V, V _{CC} = 15 V, I _C = 50 A, T _J = 25°C V _{IN} = 0 V ↔ 5 V, Inductive Load See Figure 5 (Note 6)	t _{ON}	0.50	1.00	1.60	μs
			t _{C(ON)}	-	0.50	0.95	μs
			t _{OFF}	-	1.10	1.70	μs
			t _{C(OFF)}	-	0.15	0.55	μs
			t _{rr}	-	0.25	-	μs
I _{CES}	Collector-Emitter Leakage Current	V _{CE} = V _{CES}	-	-	5	mA	

6. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. t_{C(ON)} and t_{C(OFF)} are the switching time of IGBT itself under the given gate-driving condition internally. For the detailed information see Figure 4.

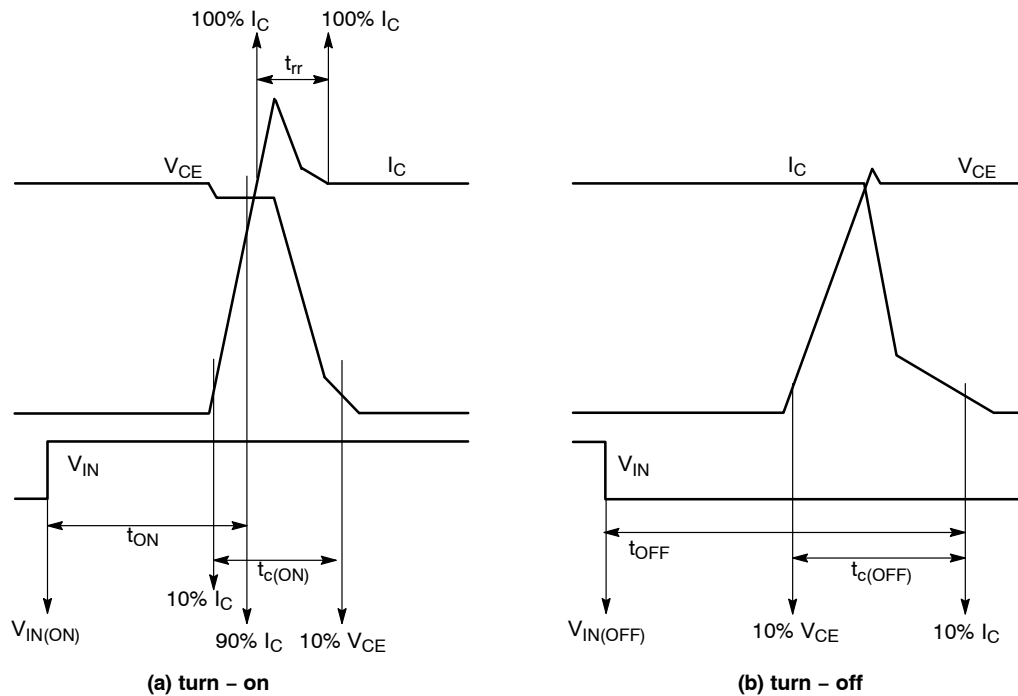


Figure 4. Switching Time Definition

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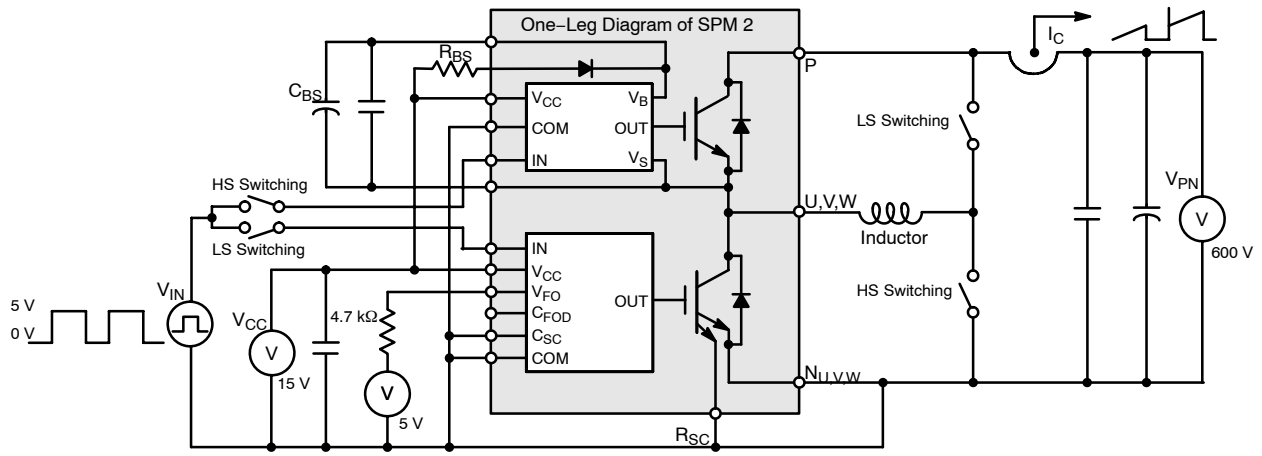


Figure 5. Example Circuit for Switching Test

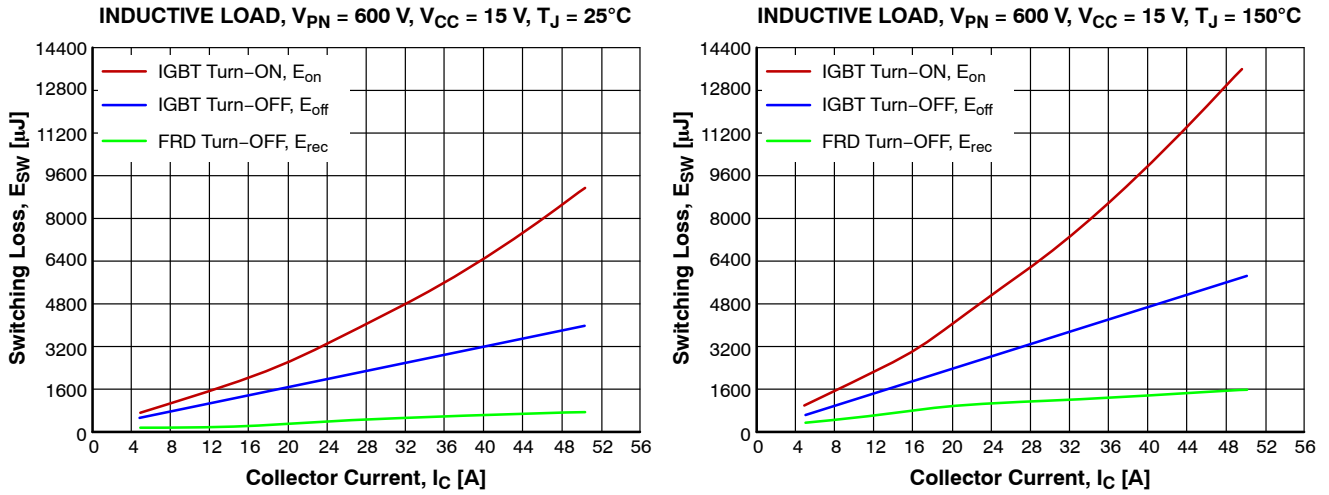


Figure 6. Switching Loss Characteristics (Typical)

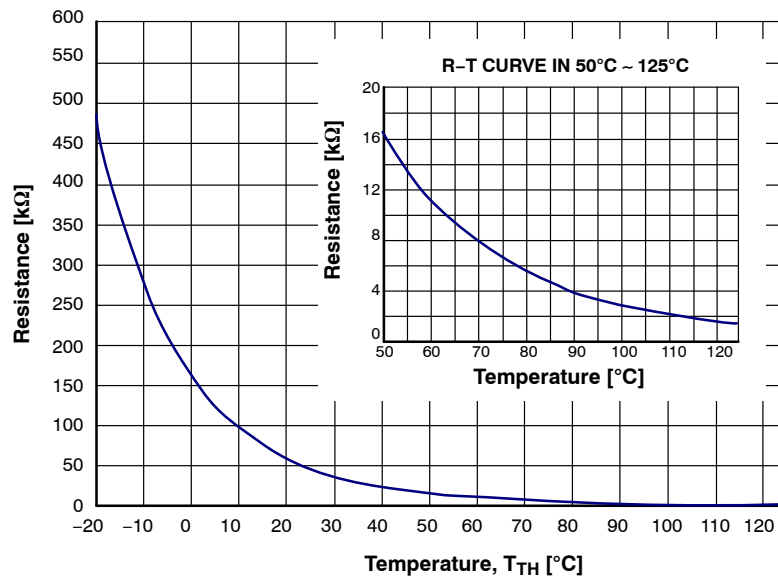


Figure 7. R-T Curve of Built-in Thermistor

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BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	$I_F = 1.0 \text{ A}$, $T_J = 25^\circ\text{C}$	-	2.2	-	V
t_{rr}	Reverse-Recovery Time	$I_F = 1.0 \text{ A}$, $di_F/dt = 50 \text{ A}$, $T_J = 25^\circ\text{C}$	-	80	-	ns

CONTROL PART ($T_J = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I_{QCC}	Quiescent V_{CC} Supply Current	$V_{CC(UH,VH.WH)} = 15 \text{ V}$, $I_{N(UH,VH.WH)} = 0 \text{ V}$	-	-	0.15	mA	
I_{QCCL}		$V_{CC(L)} = 15 \text{ V}$, $I_{N(UH,VH.WH)} = 0 \text{ V}$	-	-	5.00	mA	
I_{PDDH}	Operating V_{DD} Supply Current	$V_{CC(UH,VH.WH)} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for High-Side	-	-	0.30	mA	
I_{PDDL}		$V_{CC(L)} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for Low-Side	-	-	15.5	mA	
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{BS} = 15 \text{ V}$, $I_{N(UH,VH.WH)} = 0 \text{ V}$	-	-	0.30	mA	
I_{PBS}	Operating V_{BS} Supply Current	$V_{CC} = V_{BS} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for High-Side	-	-	12.0	mA	
V_{FOH}	Fault Output Voltage	$V_{CC} = 15 \text{ V}$, $V_{SC} = 0 \text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up	4.5	-	-	V	
V_{FOL}		$V_{CC} = 15 \text{ V}$, $V_{SC} = 1 \text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up	-	-	0.5	V	
$V_{SC(ref)}$	Short Circuit Trip Level	$V_{CC} = 15 \text{ V}$ (Note 7)	$C_{SC} - COM_{(L)}$	0.43	0.50	0.57	V
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level		10.3	-	12.8	V
UV_{CCR}		Reset Level		10.8	-	13.3	V
UV_{BSD}		Detection Level		9.5	-	12.0	V
UV_{BSR}		Reset Level		10.0	-	12.5	V
t_{FOD}	Fault-Out Pulse Width	$C_{FOD} = \text{Open}$	(Note 8)	50	-	-	μs
		$C_{FOD} = 2.2 \text{ nF}$		1.7	-	-	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $I_{N(UH,VH.WH)} - COM_{(H)}$, $I_{N(UL,VL.WL)} - COM_{(L)}$		-	-	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	-	-	V
R_{TH}	Resistance of Thermistor	at $T_{TH} = 25^\circ\text{C}$	See Figure 7 (Note 9)	-	47	-	k Ω
		at $T_{TH} = 100^\circ\text{C}$		-	2.9	-	k Ω

7. Short-circuit current protection is functioning only at the low-sides because the sense current is divided from main current at low-side IGBTs. Inserting the shunt resistor for monitoring the phase current at N_U , N_V , N_W terminal, the trip level of the short-circuit current is changed.
8. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation :
 $t_{FOD} = 0.8 \times 10^6 \times C_{FOD} [\text{s}]$.
9. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), conduct experiments considering the application.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	300	600	800	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH, VH, WH)} - COM_{(H)}$, $V_{CC(L)} - COM_{(L)}$	14.0	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD}/dt , dV_{BS}/dt ,	Control Supply Variation		-1	-	1	V/ μ s
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	2.0	-	-	μ s
f_{PWM}	PWM Input Signal	$-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$	-	-	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between $N_U, N_V, N_W - COM_{(H,L)}$ (Including Surge Voltage)	-5	-	5	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	$V_{CC} = V_{BS} = 15\text{ V}$, $I_C \leq 75\text{ A}$, Wiring Inductance between $N_{U,V,W}$ and DC Link $N < 10\text{ nH}$ (Note 10)	2.5	-	-	μ s
$PW_{IN(OFF)}$			2.5	-	-	
T_J	Junction Temperature		-40	-	150	$^{\circ}\text{C}$

10. This product might not make response if input pulse width is less than the recommended value.

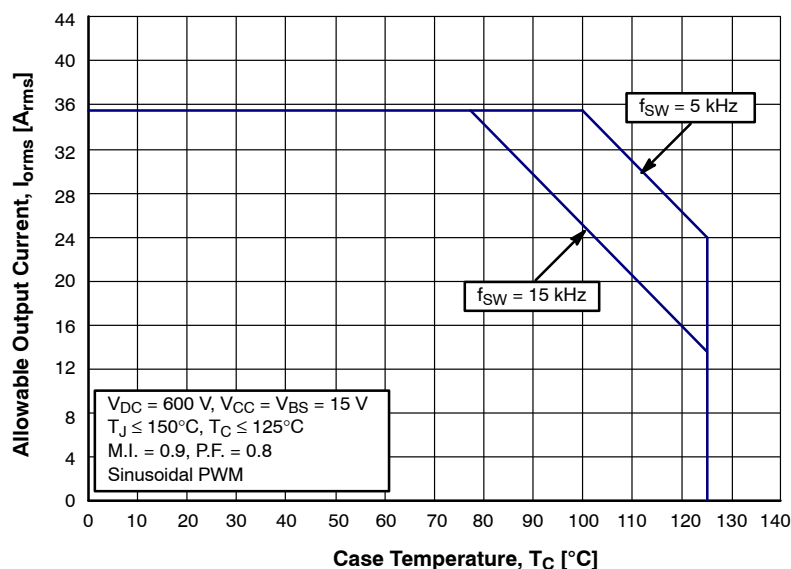


Figure 8. Allowable Maximum Output Current

NOTE:

11. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

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MECHANICAL CHARACTERISTICS AND RATINGS

	Min.	Typ.	Max.			
Device Flatness	See Figure 9		0	-	+200	μm
Mounting Torque	Mounting Screw: M4 See Figure 10	Recommended 1.0 N•m	0.9	1.0	1.5	N•m
		Recommended 10.1 kg•cm	9.1	10.1	15.1	kg•cm
Terminal Pulling Strength	Load 19.6 N		10	-	-	s
Terminal Bending Strength	Load 9.8 N, 90 degrees Bend		2	-	-	times
Weight			-	50	-	g

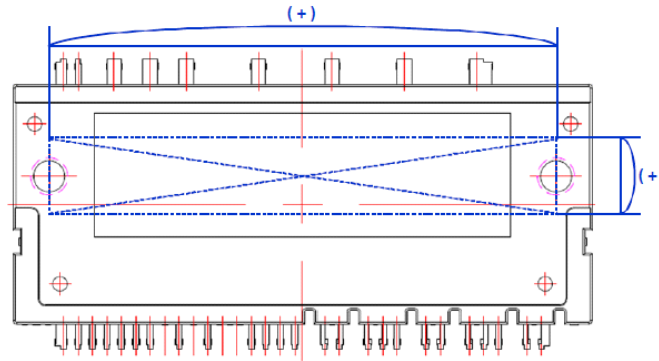


Figure 9. Flatness Measurement Position

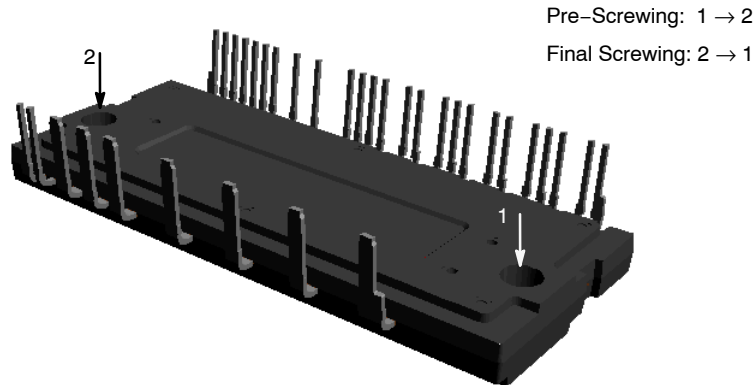
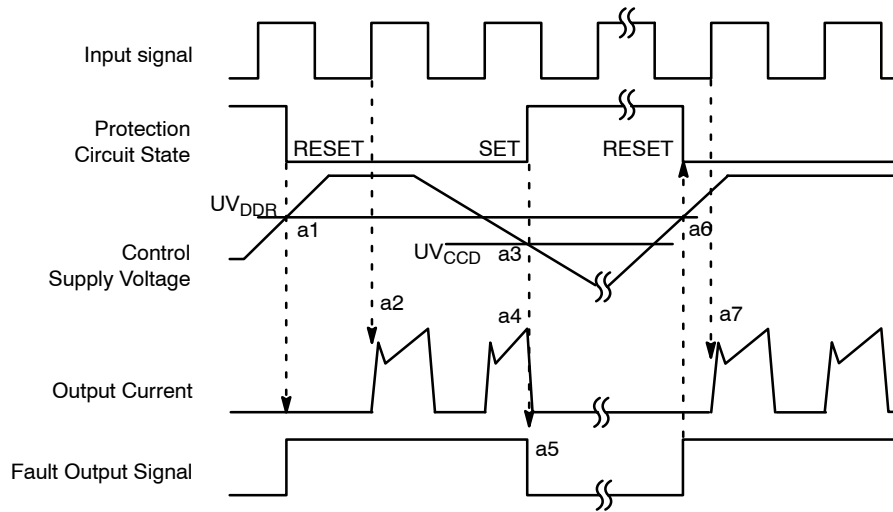


Figure 10. Mounting Screws Torque Order

NOTES:

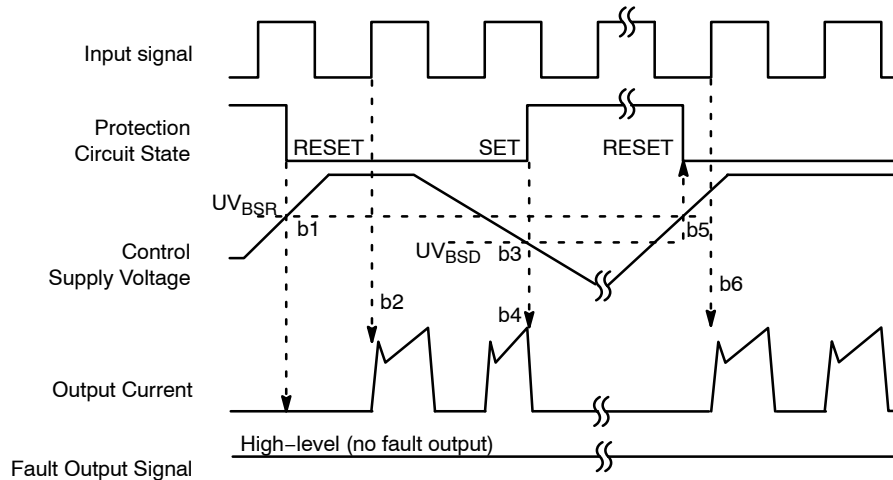
12. Do not make over torque when mounting screws. Much mounting torque may cause DBC cracks, as well as bolts and Al heat-sink destruction.
13. Avoid one-sided tightening stress. Figure 10 shows the recommended torque order for mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

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- a1: Control supply voltage rises: After the voltage rises UV_{CCR} , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UV_{CCD}).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .
- a6: Under-voltage reset (UV_{CCR}).
- a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

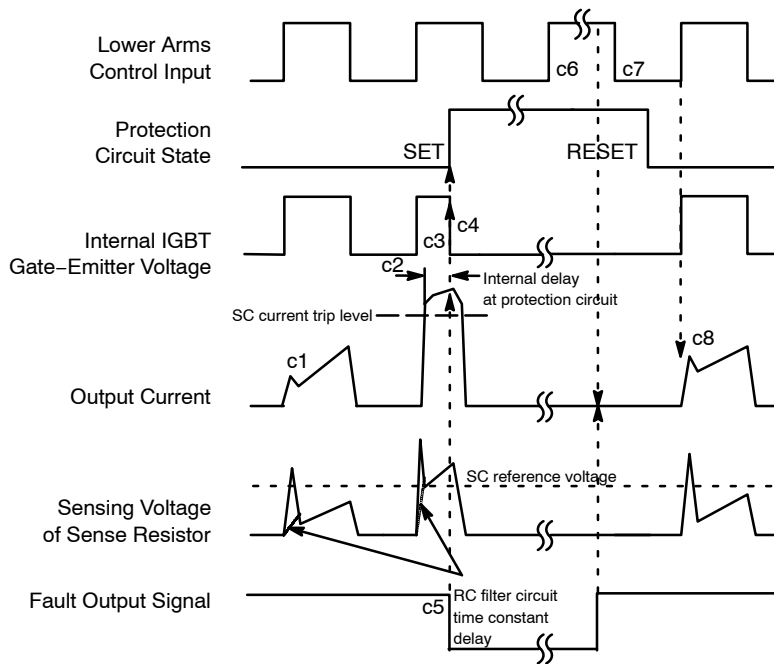
Figure 11. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: After the voltage rises UV_{BSR} , the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection (UV_{BSD}).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset (UV_{BSR}).
- b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 12. Under-Voltage Protection (High-Side)

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(with the external sense resistance and RC filter connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short circuit current detection (SC trigger).

c3: All low-side IGBTs gate are hard interrupted.

c4: All low-side IGBTs turn OFF.

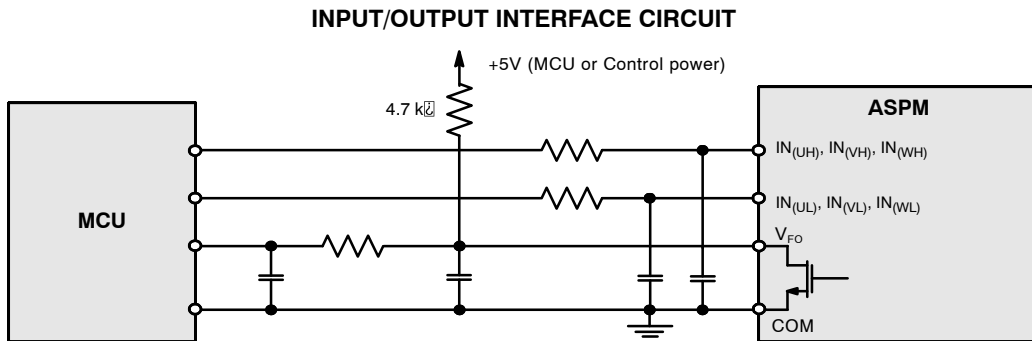
c5: Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .

c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7: Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.

c8: Normal operation: IGBT ON and carrying current.

Figure 13. Short-Circuit Current Protection (Low-Side Operation Only)

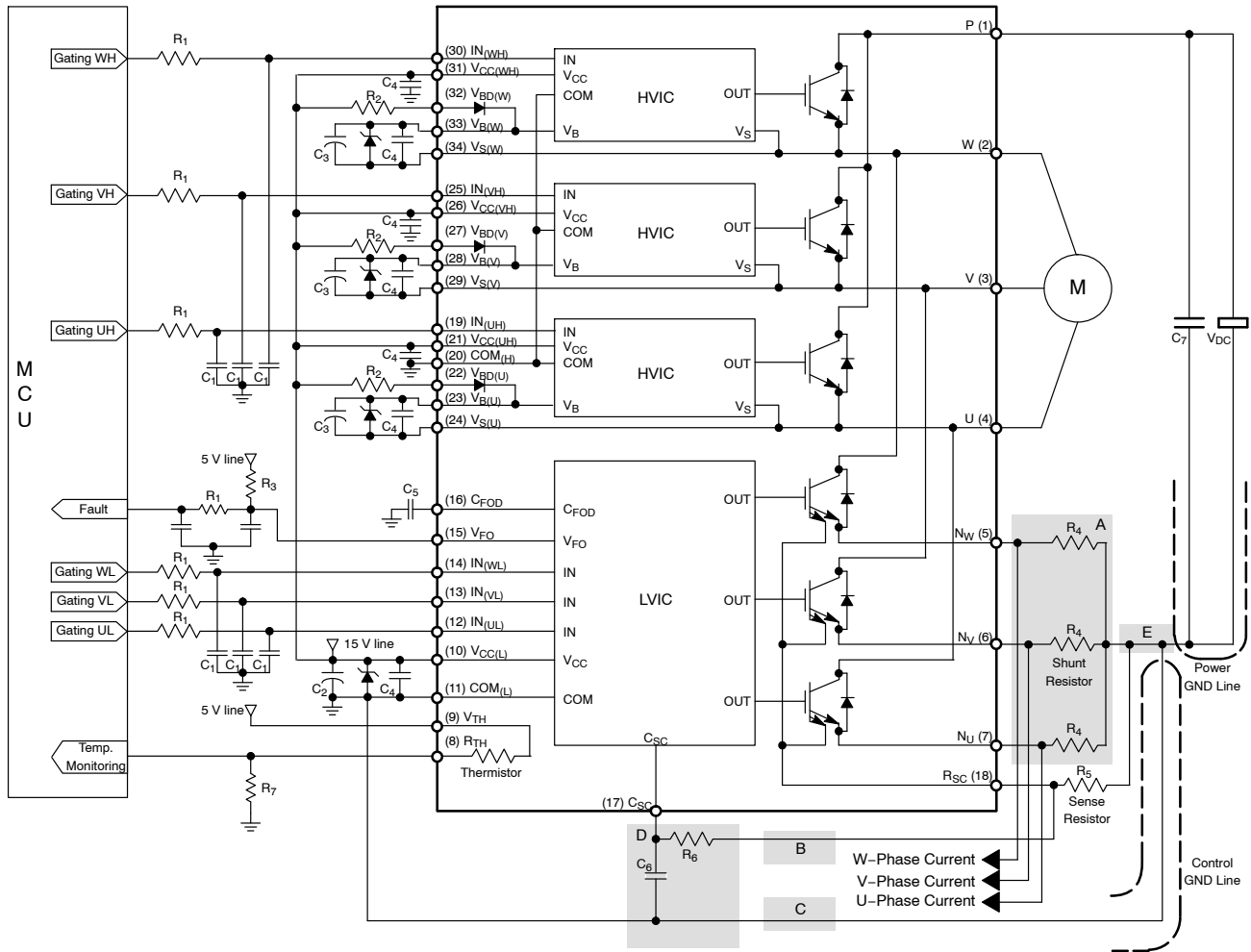


NOTE:

14. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the ASPM27 product integrates 5kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 14. Recommended CPU I/O Interface Circuit

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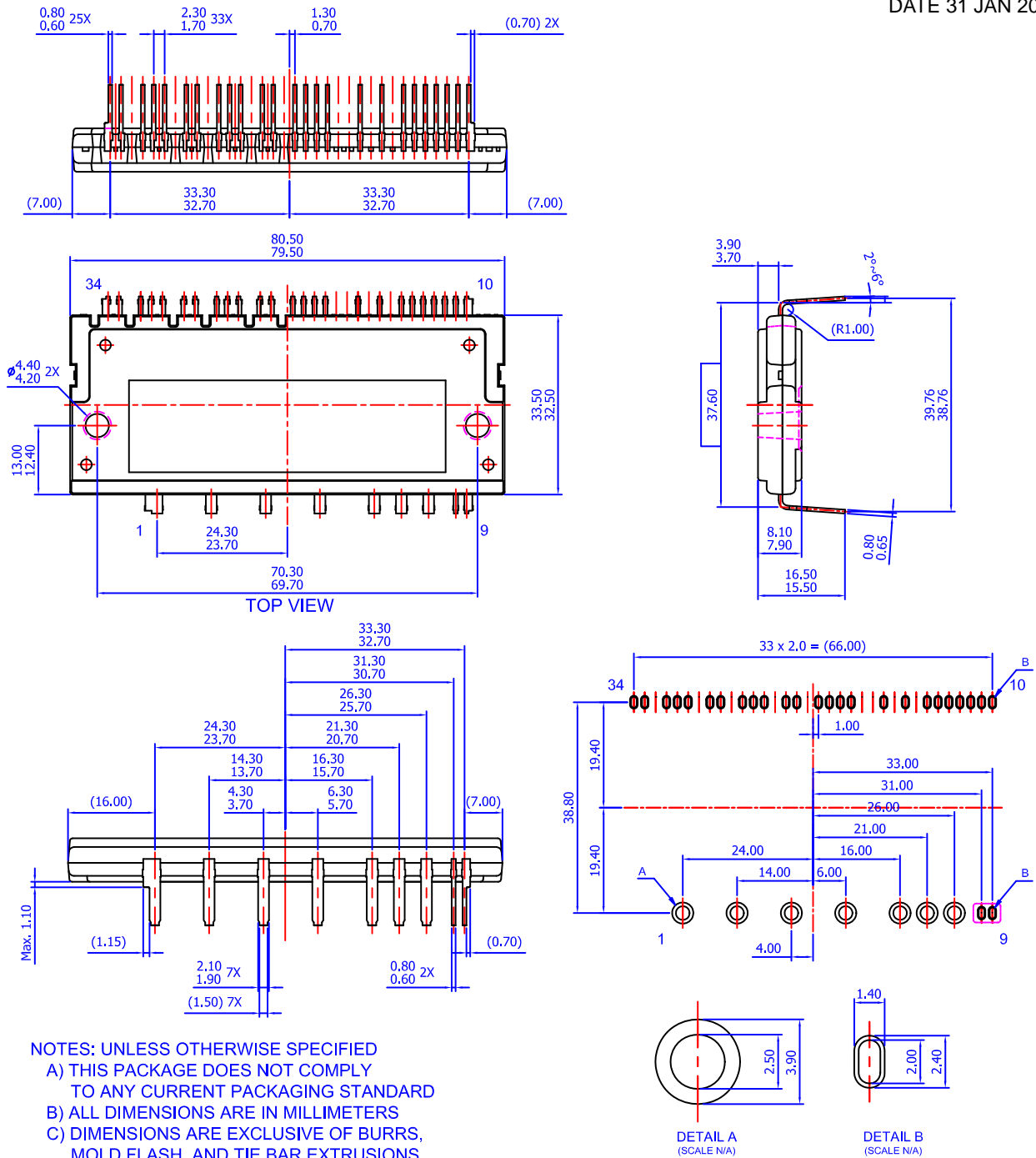
NOTES:

15. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2–3 cm)
16. V_{FO} output is open–drain type. The signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 2 mA. Please refer to Figure 14.
17. Fault out pulse width can be adjust by capacitor C_5 connected to the C_{FOD} terminal.
18. Input signal is active–HIGH type. There is a 5 Ω resistor inside the IC to pull–down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R_1C_1 time constant should be selected in the range 50 ~ 150 ns (recommended $R_1 = 100 \Omega$, $C_1 = 1$ nF).
19. Each wiring pattern inductance of point A should be minimized (recommended less than 10 nH). Use the shunt resistor R_4 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R_4 as close as possible.
20. To insert the shunt resistor to measure each phase current at N_U , N_V , N_W terminal, it makes to change the trip level I_{SC} about the short–circuit current.
21. To prevent errors of the protection function, the wiring of B, C and D point should be as short as possible. The wiring of B between C_{SC} filter and R_{SC} terminal should be divided at the point that is close to the terminal of sense resistor R_5 .
22. For stable protection function, use the sense resistor R_5 with resistance variation within 1% and low inductance value.
23. In the short–circuit protection circuit, select the R_6C_6 time constant in the range 1.0 ~ 1.5 μ s. R_6 should be selected with a minimum of 10 times larger resistance than sense resistor R_5 . Do enough evaluation on the real system because short–circuit protection time may vary wiring pattern layout and value of the R_6C_6 time constant.
24. Each capacitor should be mounted as close to the pins of the Motion SPM[®] 2 product as possible.
25. To prevent surge destruction, the wiring between the smoothing capacitor C_7 and the P & GND pins should be as short as possible. The use of a high–frequency non–inductive capacitor of around 0.1 ~ 0.22 μ F between the P & GND pins is recommended.
26. Relays are used in most systems of electrical equipment at industrial application. In these cases, there should be sufficient distance between the MCU and the relays.
27. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended Zener diode is 22 V/1 W, which has the lower Zener impedance characteristic than about 15 Ω).
28. C_2 of around seven times larger than bootstrap capacitor C_3 is recommended.
29. Please choose the electrolytic capacitor with good temperature characteristic in C_3 . Choose 0.1 ~ 0.2 μ F R–category ceramic capacitors with good temperature and frequency characteristics in C_4 .

Figure 15. Typical Application Circuit

SPMCA-A34 / 34LD, PDD STD, DBC DIP TYPE
CASE MODFQ
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DATE 31 JAN 2017



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
 - B) ALL DIMENSIONS ARE IN MILLIMETERS
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D) PACKAGE SURFACE VOID SHALL NOT EXCEED 2.3 x 2.3 x 1.0mm
 - E) () IS REFERENCE

LAND PATTERN RECOMMENDATIONS

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