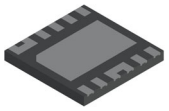
22 V/5.5 A Protection Switch with OVP/OTP and IDTRCB

FPF2890



DFN12 3x3, 0.5P
CASE 506FD

Description

The FPF2890MN features 5.5 A continuous and 15 A surge current for 10 ms @ 2% power switch for USB type C/PD application, which offers Over−Voltage Protection (OVP), Over−Temperature−Protection (OTP) and Idea Diode True Reverse Current Block (IDTRCB) to protect system. It has low On−resistance of typical 33 mΩ with DFN package can operate from 3.4 V to 22 V and up to 28 V absolute maximum.

The FPF2890MN is the ideal solution for multi−port Type−C PD current sinking application. The Ideal Diode True Reverse Current Blocking (IDTRCB) feature prevents VIN to rise due to reverse current flow from VOUT under all conditions. An internal soft−start circuit controls inrush current due to capacitive loads and the slew rate can be adjusted using an external capacitor. The integrated back−to−back MOSFET offer industry's lowest ON resistance and highest SOA to safely handle high current and wide range of output capacitances on VOUT.

The FPF2890MN is available in a thermal enhanced 3 mm x 3 mm DFN−12 package which can operate over −40°C to +125°C junction temperature range.

Features

- 22 V/5.5 A Capable OTP/OVP/IDTRCB Power Switch
- 15 A Peak Current for 10 ms @ 2% Duty Cycle
- Input Voltage Range:
  - VIN : 3.4 V~22 V
- Ultralow On−resistance
  - Typical 33 mΩ
- Up to 28 V Input/Output Voltage ABS
- Active HIGH EN Polarity
- Ideal Diode True Reverse Current Blocking (IDTRCB)
- Configurable Soft−Start
- Thermal Shutdown
- Open Drain Fault FTLB Output to Indicate INRUSH, OTP, OVP, IDTRCB Event
- Thermally Enhanced DFN 3x3 − 12L Package
- IEC 61000−4−5: ±35 V on VIN and VOUT
- IEC 61000−4−2: ±8 kV on VIN and VOUT

Applications

- Computing and Laptop

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Application Diagram

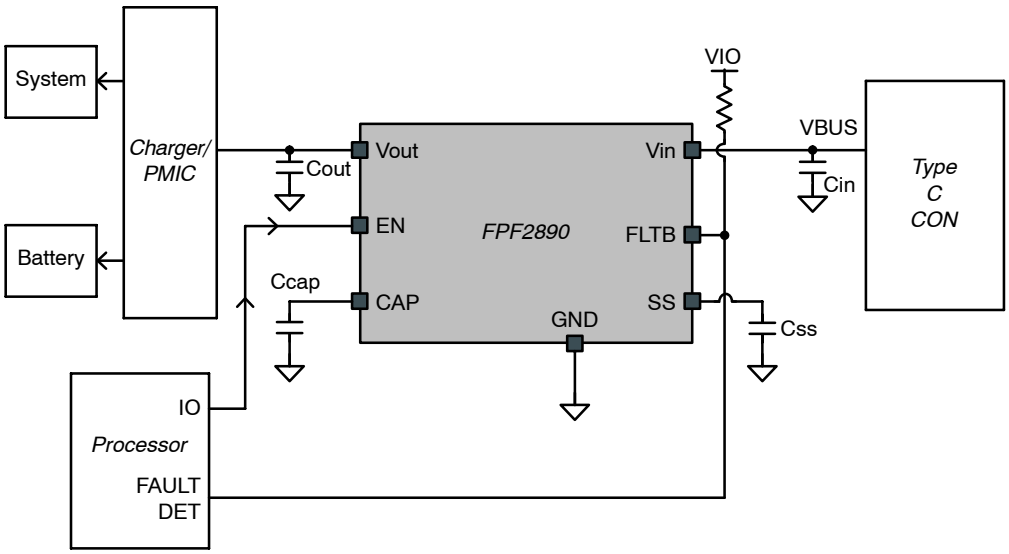


Figure 1. Typical Application

Block Diagram

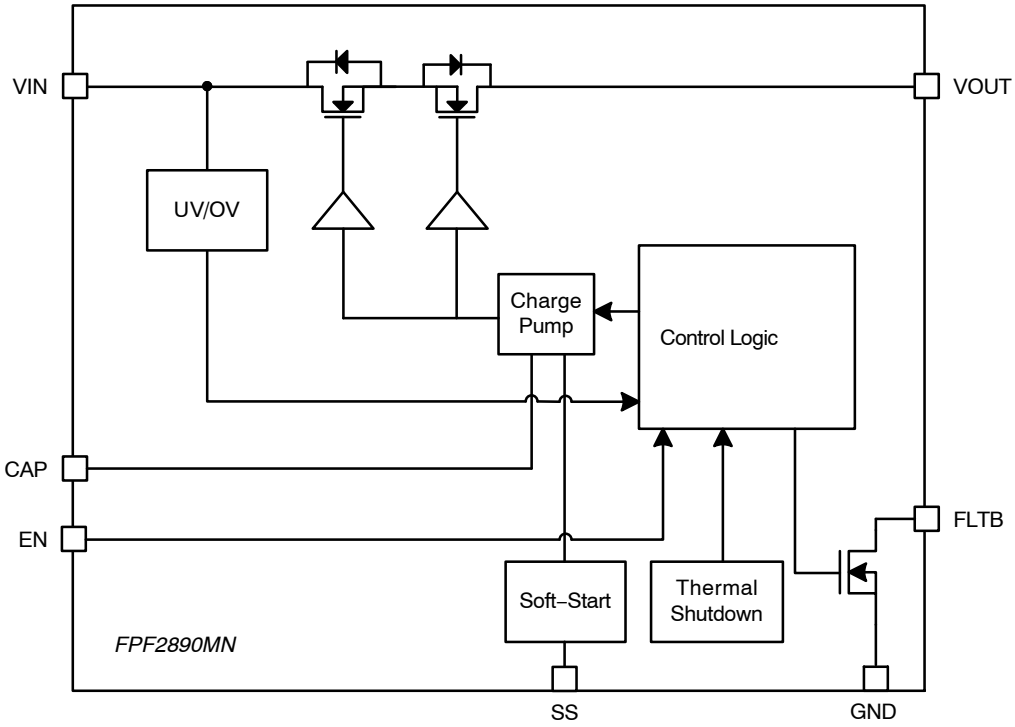
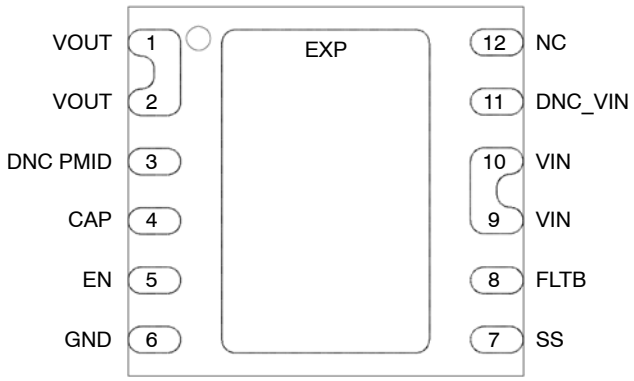


Figure 2. Typical Application

Pin Configuration



DFN3x3−12L

Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

Pin Number	Pin Name	Description
1, 2	VOUT	Output pins. Connect to internal load.
3	DNC_PMID	Do Not Connect.
4	CAP	Connect a 1 nF capacitor to GND.
5	EN	Enable active high.
6	GND	Ground.
7	SS	Soft−start pin. Connect a capacitor CSS from SS to GND to set the soft−start time.
8	FLTB	Fault Indicator, open−drain output. Pull low after a fault condition is detected.
9,10	VIN	Connect to adapter or power input. Place a 10 μF capacitor from VIN to GND.
11	DNC_VIN	Internally connected to VIN. If outside connected to VIN, can effectively reduce the Ron. recommend connecting to VIN.
12	NC	No connect
EXP	EXP	Exposed Thermal Pad. It must be electrically isolated. Solder to a metal surface directly underneath the EXP and connect to floating copper thermal pads on multiple PCB layers through many Vias. For best thermal performance, make the floating copper pads as large as possible.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
VIN/CAP	VIN, CAP to GND		−0.3	28	V
VOUT	VOUT to GND		−0.3	28	V
V EN/SS/FLTB	EN, FLTB, SS to GND		−0.3	6	V
I_{IN_VOUT}	Continuous VIN to VOUT Current		–	5.5	A
	Peak VIN to VOUT Current (10 ms / 2% Duty Cycle)		–	15	A
T_{STG}	Storage Junction Temperature Range		−65	+150	°C
T_J	Junction Temperature		–	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		–	+260	°C
θ_{JC}	Thermal Resistance, Junction−to−Case (2S2P.1in. (Note 1) pad of 2 oz. Copper)		–	2.38	°C/W
θ_{JA}	Thermal Resistance, Junction−to−Ambient (2S2P.1in. (Note 1) pad of 2 oz. Copper)		–	32.18	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS−001	2	–	kV
		Charged Device Model, JESD22−C101	2	–	
	IEC61000−4−2 System Level	Air Discharge at VIN and VOUT (Note 2)	8	–	
		Contact Discharge at VIN and VOUT (Note 2)	8	–	
Surge	IEC61000−4−5	VIN, VOUT	35	–	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured using 2S2P JEDEC std. PCB.
2. External TVS is required to guarantee.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VIN	VIN Operating Voltage	3.4	22.0	V
V EN/FLAGB	EN, FLTB	0	5.5	V
VCAP	CAP to VIN	0	5.5	V
Vss	SS to Ground	0	3	V
T_A	Ambient Operating Temperature	−40	85	°C
T_J	Operating Junction Temperature	–	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A= −40 to 85°C; Typical values are at VIN = 20 V, EN = 5 V, T_A = 25°C, CCAP = 1 nF, CIN = 10 μF, COUT = 10 μF, CSS = 5.6 nF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Validate device functionality across the VIN recommended operating range.	3.4	–	22	V
V_{UVLO}	Under−voltage Lockout Threshold	VIN rising	3	–	3.35	V
V_{UVLO_HYS}	Under−voltage Lockout Hysteresis		–	250	–	mV
I_{VIN_ON}	Input Quiescent Current	IOUT = 0 mA, EN = 5 V	–	380	–	μA
I_{VIN_OFF}	VIN Shutdown Current	EN = GND, VIN = 20 V, IOUT = 0 A	–	32	48	μA
I_{VOUT_OFF}	Output Leakage Current	EN = 0, VOUT = 20 V, VIN = 0 V	–	4.5	7.5	μA
R_{ON_20V}	On Resistance	VIN = 20 V, IOUT = 1000 mA, EN = 5 V	–	33	–	mΩ
R_{ON_5V}	On Resistance	VIN = 5.0 V, IOUT = 1000 mA, EN = 5 V	–	35	–	mΩ
V_IH_EN	Input Logic High Voltage	Rising	–	–	1.4	V
V_IL_EN	Input Logic Low Voltage	Falling	0.6	–	–	V
V_OL_FLTB	Output Logic Low Voltage	FLTB sinking 3 mA	–	–	0.3	V
R_EN_LOW	Input Pull−down Resistance		475	730	985	kΩ
V_{OVP}	Over−voltage Protection Threshold	VIN Increasing	23	24	25	V
t_{OVP_DEB}	Over−voltage Protection Debounce Time	Latch off. No restart	–	512	–	μs
V_{IDTRCB}	Ideal Diode TRCB Regulation Voltage	VIN − VOUT	–	70	–	mV
V_{T_RCB}	TRCB Protection Trip Point	VOUT − VIN	–	50	–	mV
t_{RCB_DEL}	TRCB Delay Time (Note 3)		–	0.5	–	μs
T_{SD}	Thermal Shutdown	Temperature rising. System latch off.	–	140	–	°C
t_{D_ON}	Turn−On Delay Time	From EN rising edge to VOUT reaching 10% of VIN	–	8	–	ms
t_{ON}	Turn−On Rise Time	VOUT from 10% to 90% of VIN = 20 V	–	1.9	–	ms
t_{OFF}	Turn−Off Fall Time	From EN falling edge to IOUT = 0 A	–	32	–	μs
t_{RESET}	Current Clamping Timer (Note 3)		–	512	–	μs
t_{RETRY}	Current Clamping Retry Timer (Note 3)		–	8	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by characterization and design.

Timing Diagrams

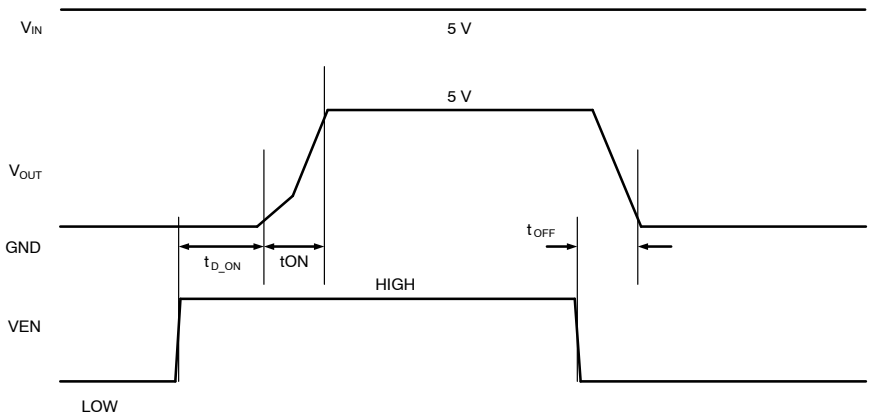


Figure 4. VIN to VOUT Power Up/Down and Normal Operation

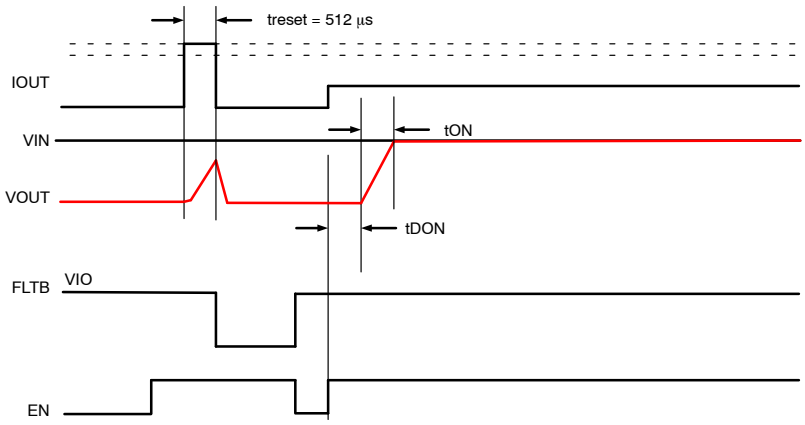


Figure 5. Inrush Current Limit and SCP Operation (Latch−Off)

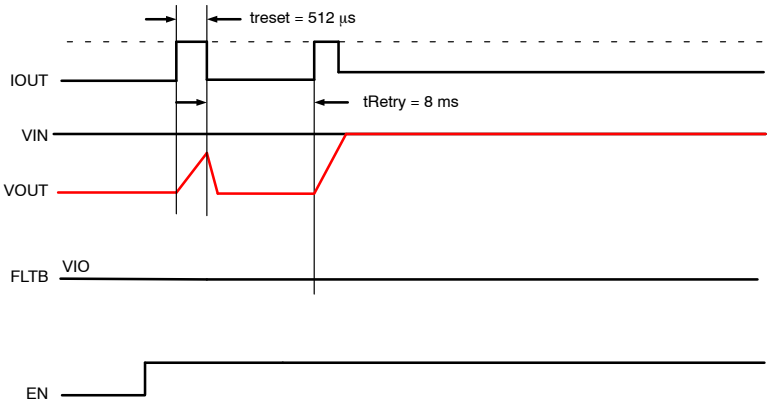


Figure 6. Inrush Current Limit and SCP Operation (Auto−Retry)

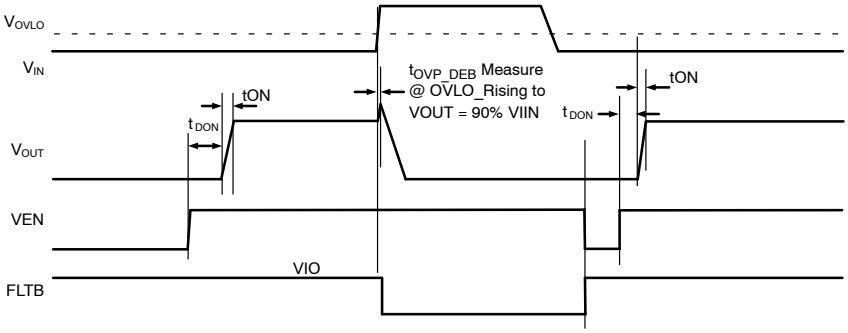


Figure 7. OVP Operation

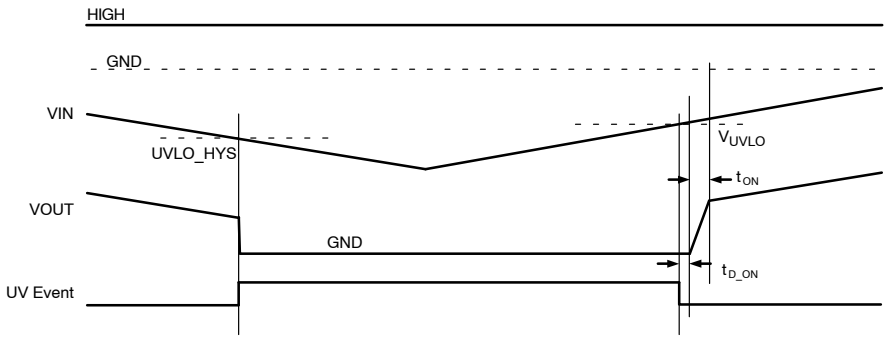


Figure 8. UVLO Operation

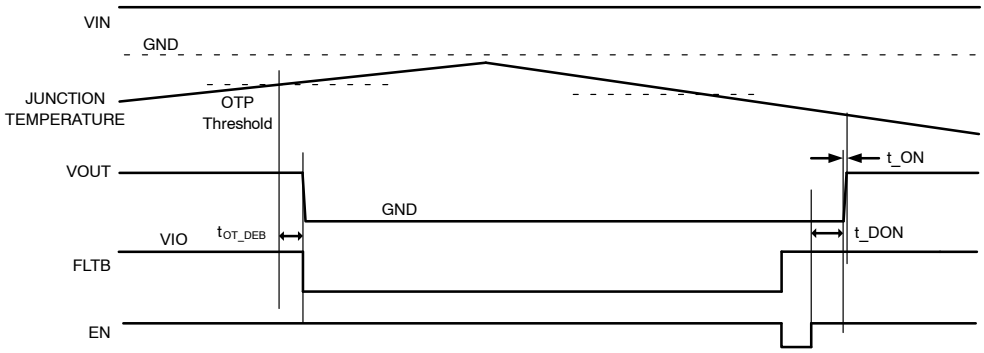


Figure 9. Thermal Shutdown Operation

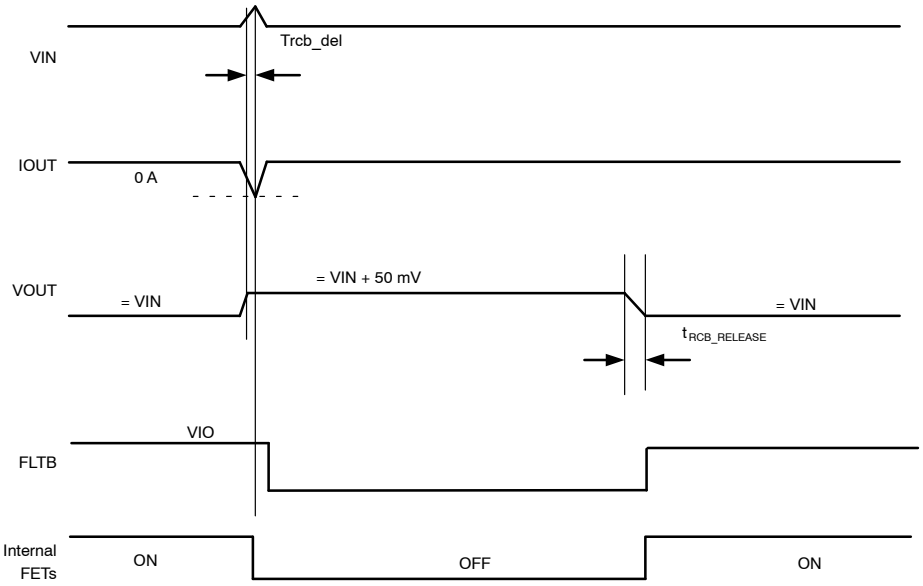


Figure 10. TRCB Operation (FLTB was configured active)

Operation Description

FPF2890MN is a protection switch with soft−start, over−voltage, and over temperature protections. It is capable of operating from 3.4 V to 22 V. The internal power switch consists of back−to−back connected MOSFET. When the switch is enabled, the overall resistance between VIN and VOUT is only 33 mΩ. The back−to−back configuration of MOSFET completely isolates VIN and VOUT when the switch is turned off, preventing leakage between the two pins with IDTRCB function integrated.

Soft−Start Slew−Rate Control

TA = 25°C, CCAP = 1 nF, CIN = 10 μF, COUT = 10 μF, CSS = 5.6 nF. Soft−start control process as the below reference.

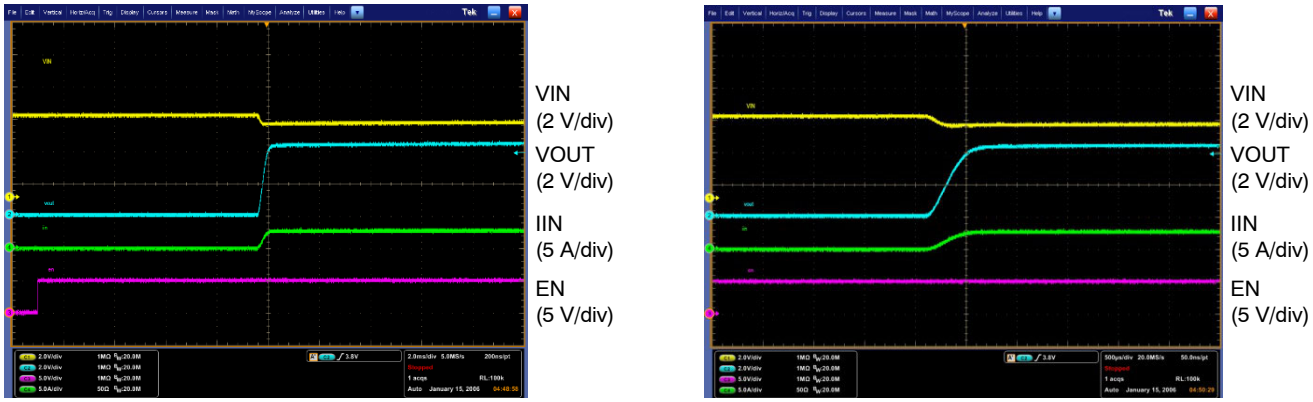


Figure 11. VIN = 5 V, ROUT = 0.86 Ω

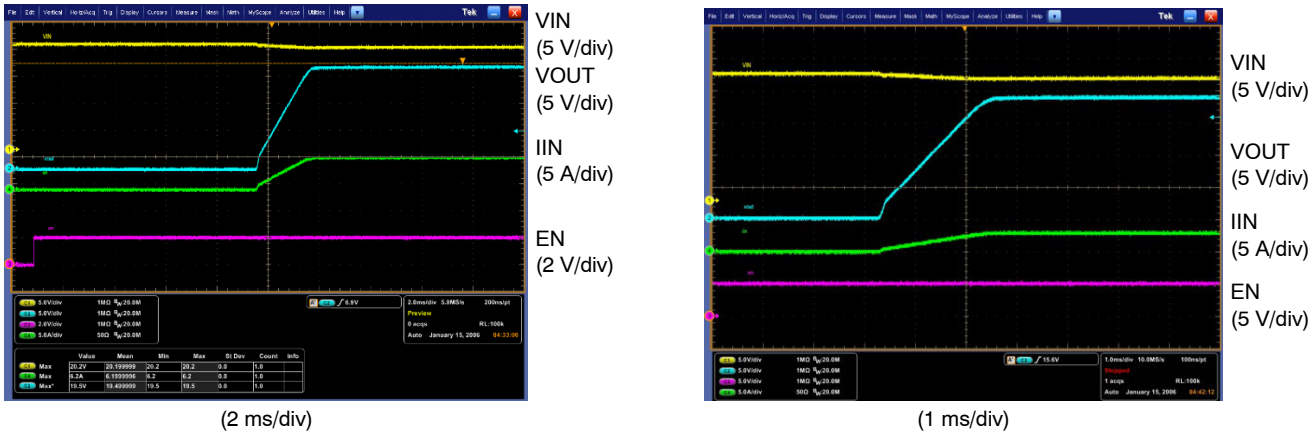


Figure 12. VIN = 20 V, ROUT = 3.4 Ω

When EN pin is asserted high, the slew rate control applies voltage on the gate of the power switch in a manner such that the output voltage is ramped up linearly until VOUT reaches VIN voltage level. The output ramps up time (tON) is programmable by an external soft−start capacitor (CSS). The following formula provides the estimated 10% to 90% ramp up time.

$$t_{ON} = \frac{2 \times C_{SS} \times V_{IN}}{112.5} \times 10^3 \qquad \text{(eq. 1)}$$

Where Css is nF and t_{ON} is μs.

Inrush Current Limit and SCP at Start Up

FPF2890MN has the current limit and short circuit protection functions at start up period .Once the loading current pass through FPF2890MN is higher than current limitation or the power consumption is higher than power limitation during start up condition , then an current limitation will be triggered and load current will be regulated to Ilimit = Plimit / (Vin − Vout), there are two power limitation levels will be applied according to different voltage level of Vout , when Vout < 1.1 V like Vout was short to ground directly, power limitation is about 24 W and the current limitation is about 4.8 A, while vout goes up above 1.1 V, the power limitation increased to 42 W, the current will not over than 8 A max at any condition, and when the limitation last more than 512 μs, then FPF2890MN will turn off switch and signal system by pulling down the FLTB pin (latch off version), and FLTB will be released and next try will be applied once system toggle EN pin low and high again or cycling the Vin. If the inrush protection was finished earlier than 512 μs, then timer will be reset. Also, an auto−retry mode with 8 ms delay can be enabled by changing fuse setting as back up. Below showed is VIN = 10 V, Cout = 1000 μF, EN from low to high, VOUT from a low voltage more than 1.1 V (The residual charge on the large capacitor) then start−up process, First trigger the power limit protection, then trigger current limit

protection. But please note both current limit and SCP shutdown are disable after soft−start time is finished.

Figure 13. Start−up Protection

SOA Curves

Figure 14 illustrates the power switch Safe Operating Area (SOA) Curves. FPF2890MN power switch is robust enough to drive a large output capacitance with load in reasonable soft−start time.

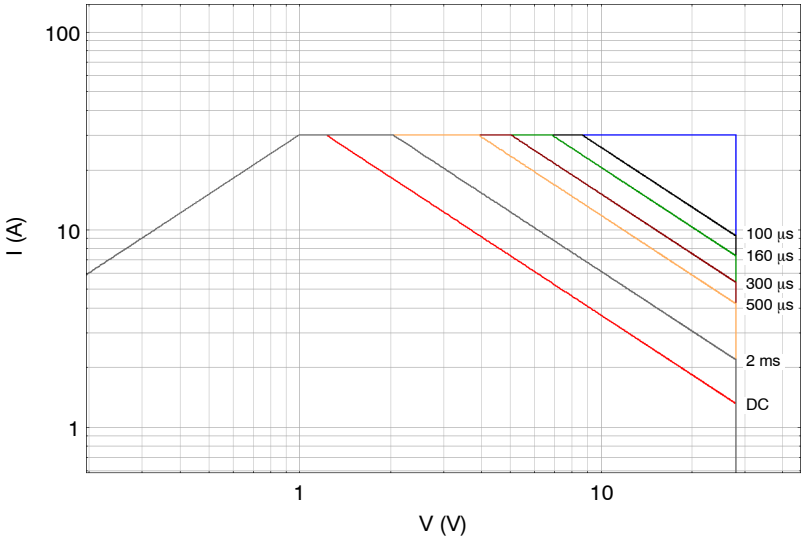


Figure 14. Safe Operating Area (SOA) Curves for Power Switch

Input Under−Voltage Lockout (UVLO)

The internal control circuit is powered from VIN. The under−voltage lockout (UVLO) circuit monitors the voltage at the input pin (VIN) and only allows the power switches to turn on when it is higher than 3.35 V (VUVLO).

Over Voltage Lockout (OVLO)

The voltages at VIN pin are constantly monitored once the device is enabled. In case the voltage exceeds the OVLO threshold, over−voltage protection is activated:

1. If the power switch is on, it will be turned off after OVP debounce time (tOVP_DEB) to isolate VOUT from VIN;
2. OVP will prevent power switch to be turned on if it is in off state; In either case FLTB pin is pulled low to report the fault condition. The device can only be re−enabled by either toggling EN pin or cycling the input power supply, for OVP response time setting, it is 512 μs in default, can also be removed by different fuse setting.

Ideal Diode and True Reverse Current Blocking (ID−TRCB)

When the device is ON with no load or under light load conditions, it regulates VOUT to be 70 mV below VIN. As the load current is increasing or decreasing, the device

adjusts the gate drive to maintain the 70 mV drop from VIN to VOUT. As the load current continues to increase the device increases the gate drive until the gate is fully turned on and VIN to VOUT drop is determined by IR drop through the MOSFET. If for any reason VOUT increases such that VIN to VOUT drop to less than 70 mV, the gate driver forces the switch to turn off.

The FPF2890MN also features a fast comparator that turns off the power switch upon detection of VOUT – VIN is higher than 50 mV (VTRCB) after TRCB delay time (tTRCB_DEL). When the FPF2890MN is first enabled or during each auto−restart, power switch will be kept off if VOUT is 50 mV higher than VIN. The below show is the TRCB behavior test, VIN and VOUT offset is 16 V, VOUT increased by difference slew rate.

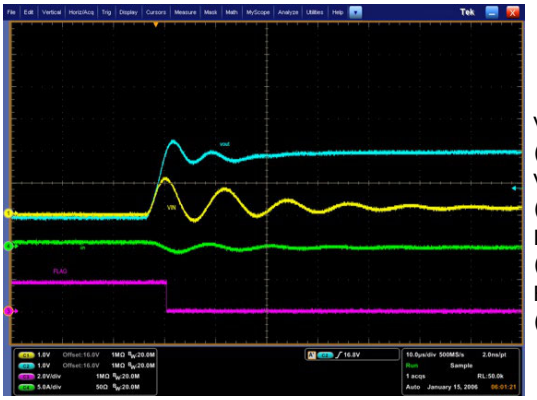


Figure 15. TRCB Behavior for Rout = 20 Ω (FLTB was configured active)

Fault FLTB

Open drain output requiring external bias and pull−up resistor. 1~2 mA capability is preferred to drive LED or GPIO port as an indicator if necessary.

Table 1.

FLTB	Description
LOW	Device is in fault condition: Inrush protection, OVP and Thermal Shutdown or TRCB was triggered (fuse configurable, default will not pull down FLTB)
Hi−Z	Device is in normal condition

Thermal Shutdown (OTP)

Protect the device from over temperature, the power switch turn OFF and FLTB turn to Low immediately when the junction temperature exceeds TSD, then if junction temperature drop to lower than thermal shutdown hysteresis and toggle EN or cycling VIN then FLTB will release and take another try to close back switch.

Layout Design Notes

FPF2890MN is a protection switch designed deliver high current. Layout is critical to remove the heat generated by this current. For the most efficient heat sinking, connect as much copper as possible to the exposed pad. The exposed pad must be electrically isolated. On the top layer expand the exposed pad island as much as possible for optimal thermal performance. The exposed pad copper plane must be electrically isolated. See example as the below figure.

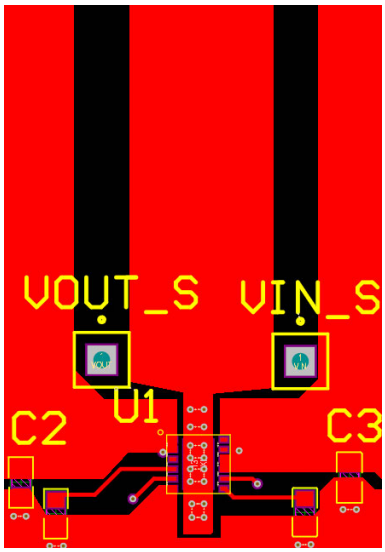


Figure 16. Top Layer Layout

There are two ways to create thermal islands on the inner layers as showed at below figures. The more layers that have these electrically isolated thermal heat sink islands the better the thermal performance will be. Connect all isolated thermal island (top, inner layer, and bottom) together with as many VIAs as possible. Please refer to the below figure inner 2 and 3 layers.

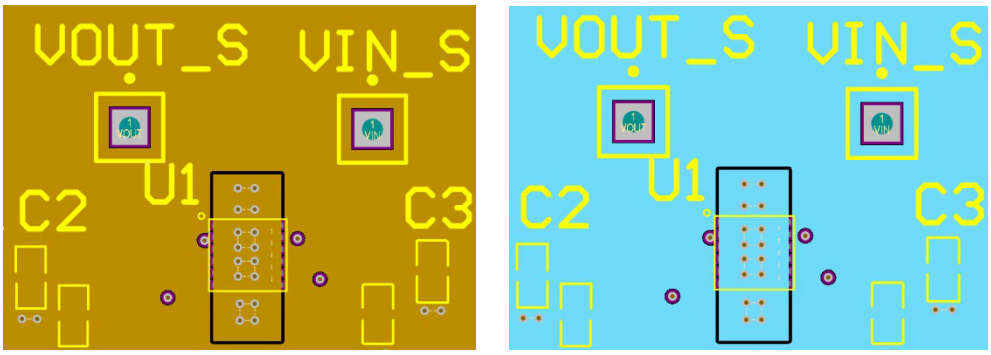


Figure 17. Inner 2− and 3−layer Layout

On the bottom layer, like the inner layers, create an isolated thermal island. Typically, there is more area available on the bottom area for a larger thermal pad. The top and bottom layers have better thermal performance than the inner layers because they are exposed to the atmosphere. See example as the below figure.

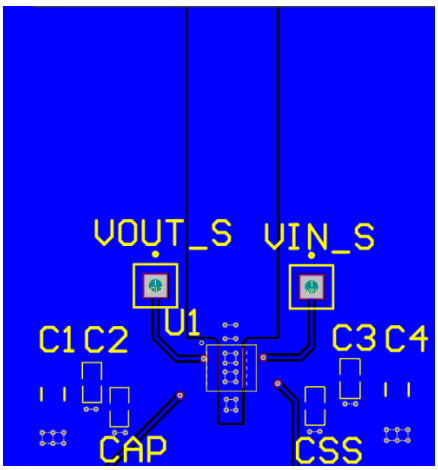
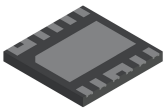


Figure 18. Bottom Layer Layout

ORDERING INFORMATION

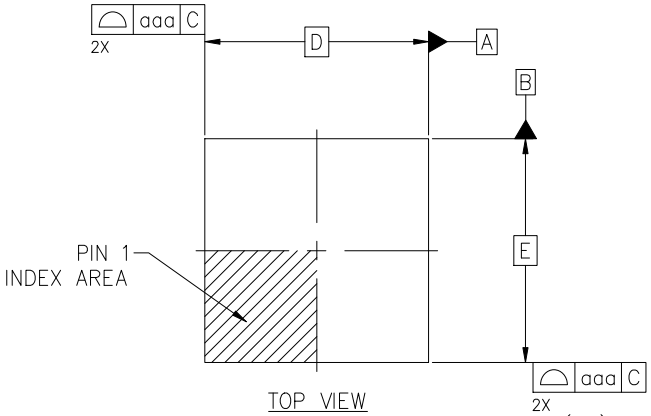
Part Number	SCP Operation	Power Limit (V_{OUT}>1.1V)	Operating Temperature Range	Top Mark	Package Type	Shipping†
FPF2890MNTXG−F	Auto−Retry	60W	−40°C − +85°C	FPF2890F	DFN12 (Pb−Free)	Tape & Reel
FPF2890MNTXG−L	Latch−Off	42W	−40°C − +85°C	FPF2890L	DFN12 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

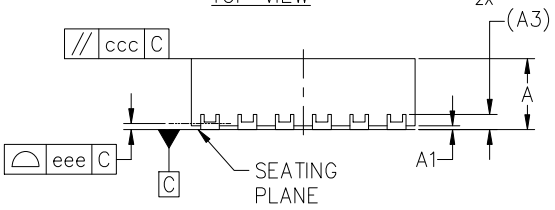


DFN12 3.00x3.00x0.95, 0.50P
CASE 506FD
ISSUE A

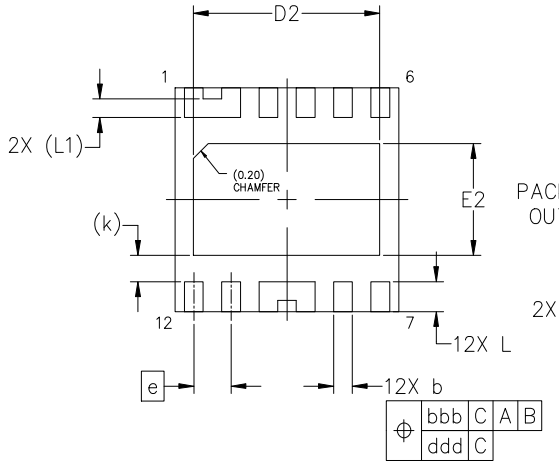
DATE 23 APRIL 2024



TOP VIEW



SIDE VIEW

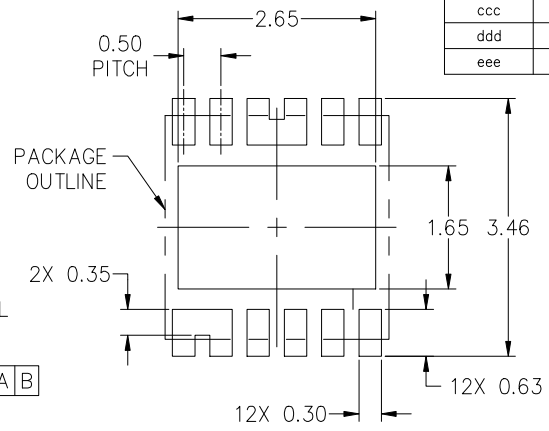


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	0.95	1.00
A1	---	---	0.05
A3		0.20 REF.	
b	0.20	0.25	0.30
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.40	1.50	1.60
e		0.50 BSC	
k		0.35 REF.	
L	0.30	0.40	0.50
L1		0.25 REF.	
TOLERANCES FOR CONTROL FEATURE FRAME			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON42269H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN12 3.00x3.00x0.95, 0.50P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales