

MOSFET – N-Channel, QFET

800 V, 3.9 A, 3.6 Ω

FQB4N80

Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. This device is suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 3.9 A, 800 V, $R_{DS(on)} = 3.6 \Omega$ (Max.) @ $V_{GS} = 10$ V, $I_D = 1.95$ A
- Low Gate Charge (Typ. 19 nC)
- Low C_{RSS} (Typ. 8.6 pF)
- 100% Avalanche Tested
- This Device is Pb-Free and Halide Free

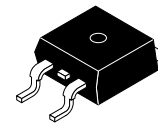
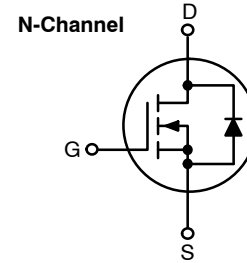
MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Rating	Value	Unit
V_{DSS}	Drain-Source Voltage	800	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	3.9	A
	– Continuous ($T_C = 100^\circ\text{C}$)	2.47	
I_{DM}	Drain Current – Pulsed (Note 1)	15.6	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	460	mJ
I_{AR}	Avalanche Current (Note 1)	3.9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)*	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	130	W
	– Derate above 25°C	1.04	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+150$	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

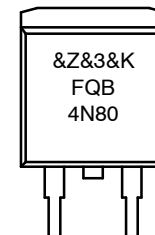
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 57$ mH, $I_{AS} = 3.9$ A, $V_{DD} = 50$ V, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 3.9$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
800 V	3.6Ω @ 10 V	3.9 A



D2PAK-3
(TO-263, 3-LEAD)
CASE 418AJ

MARKING DIAGRAMS



&Z = Assembly Plant Code
 &3 = 3-Digit Date Code Format
 &K = 2-Digits Lot Run Traceability Code
 FQB4N80 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQB4N80TM	D2PAK-3	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FQB4N80

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.96	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in ² pad of 2 oz copper), Max.	40	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to 25°C	–	0.95	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	–	–	10	μA
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	–	–	100	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
I_{GSSR}	Gate to Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.95\text{ A}$	–	2.8	3.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 1.95\text{ A}$	–	3.8	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	680	880	pF
C_{oss}	Output Capacitance		–	75	100	pF
C_{rss}	Reverse Transfer Capacitance		–	8.6	12	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 3.9\text{ A}, R_G = 25\text{ }\Omega$ (Note 4)	–	16	40	ns
t_r	Turn-On Rise Time		–	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		–	35	80	ns
t_f	Turn-Off Fall Time		–	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 3.9\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	–	19	25	nC
Q_{gs}	Gate-Source Charge		–	4.2	–	nC
Q_{gd}	Gate-Drain Charge		–	9.1	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		–	–	3.9	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	15.6	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 3.9 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 3.9 A, dI _F /dt = 100 A/μs	–	575	–	ns
Q _{rr}	Reverse Recovery Charge		–	3.65	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

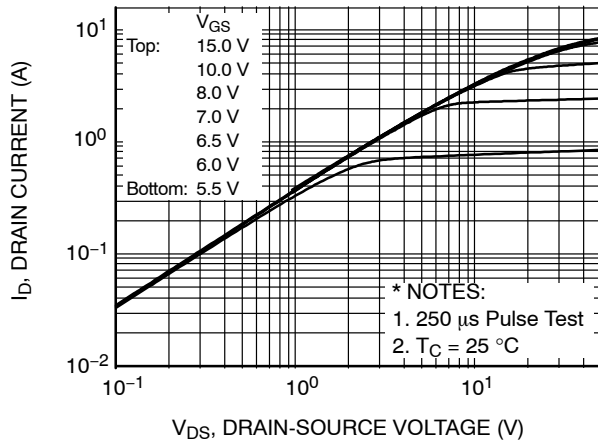


Figure 1. On-Region Characteristics

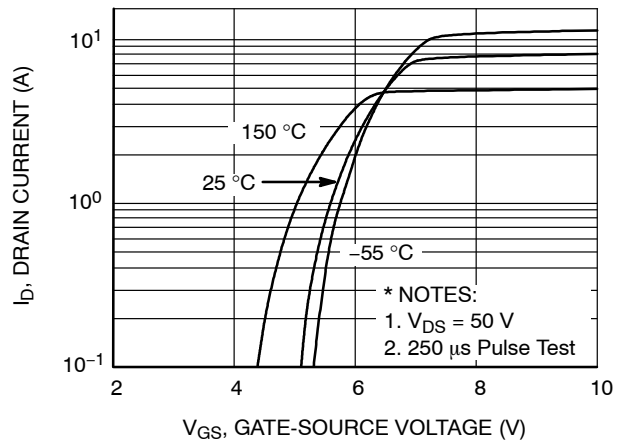


Figure 2. Transfer Characteristics

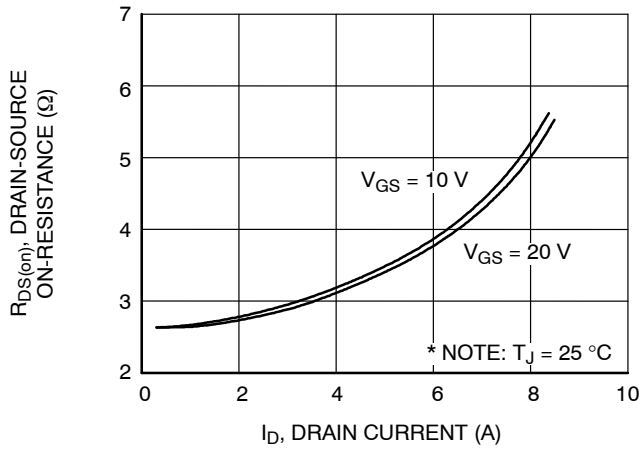


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

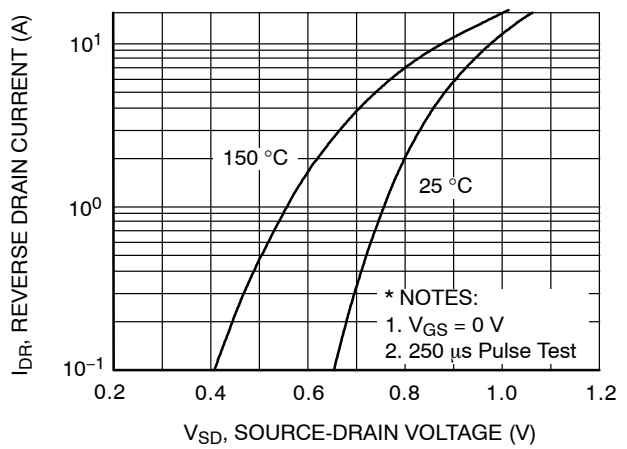


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

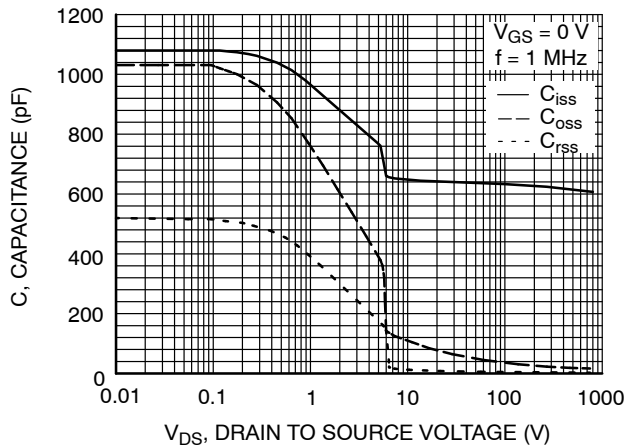


Figure 5. Capacitance Characteristics

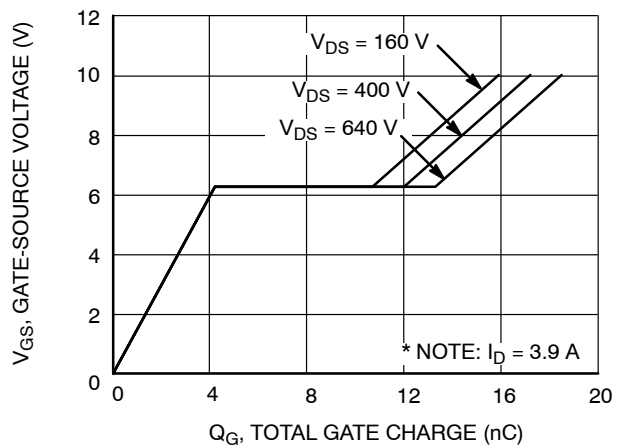


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

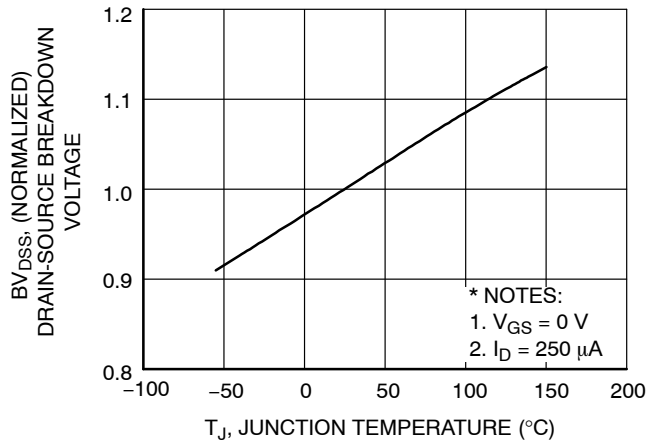


Figure 7. Breakdown Voltage Variation vs. Temperature

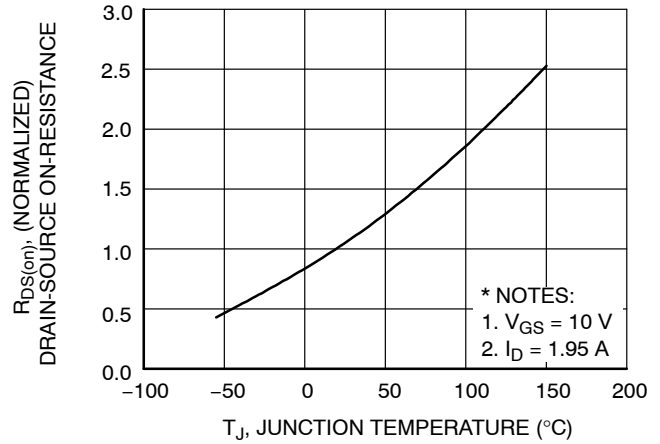


Figure 8. On-Resistance Variation vs. Temperature

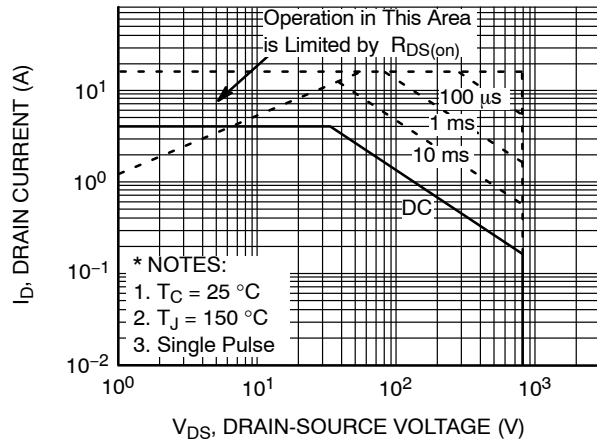


Figure 9. Maximum Safe Operating Area

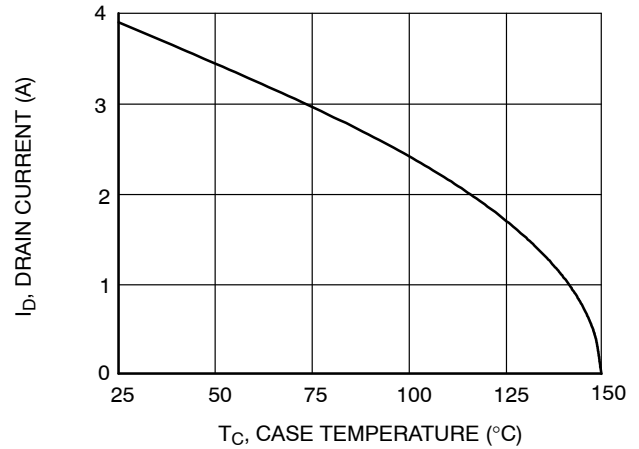


Figure 10. Maximum Drain Current vs. Case Temperature

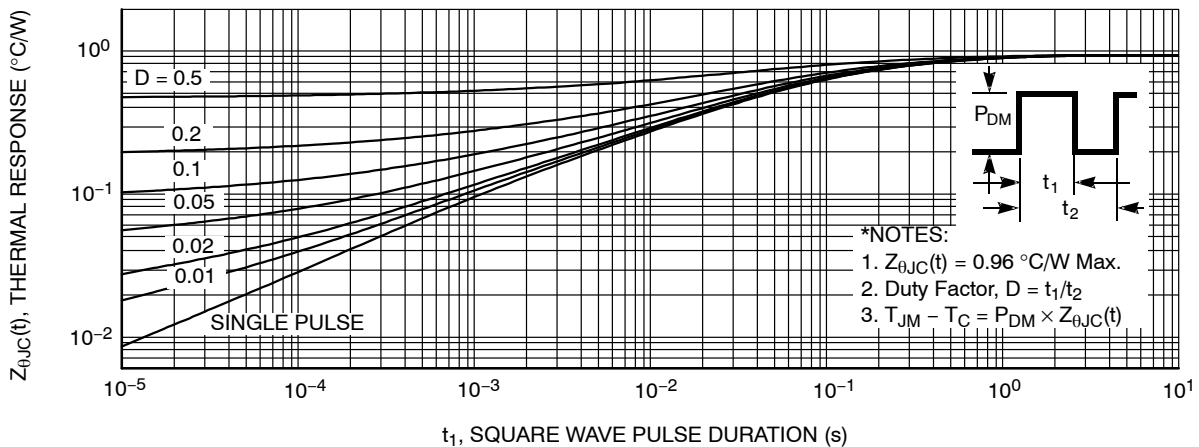


Figure 11. Transient Thermal Response Curve

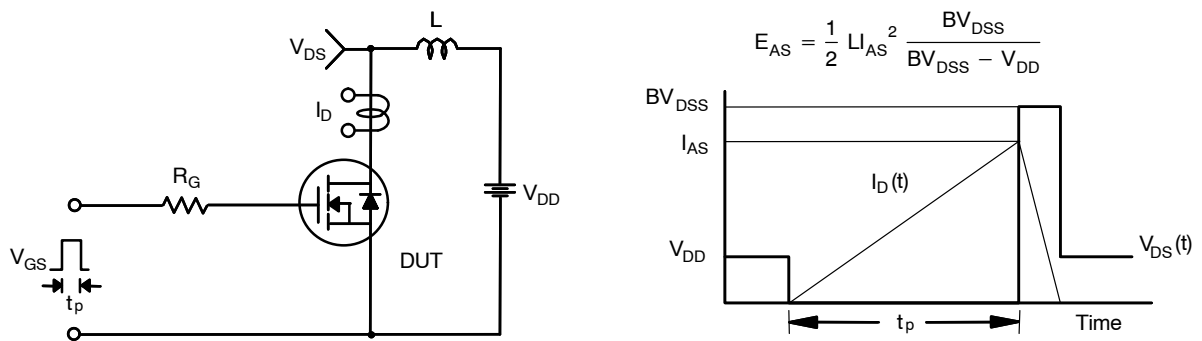
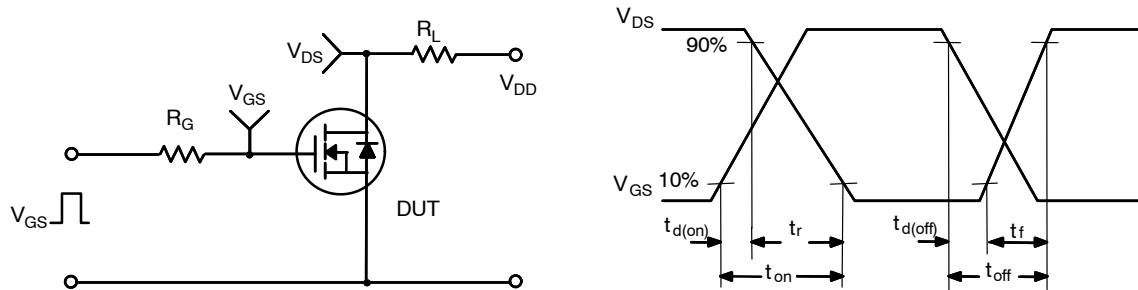
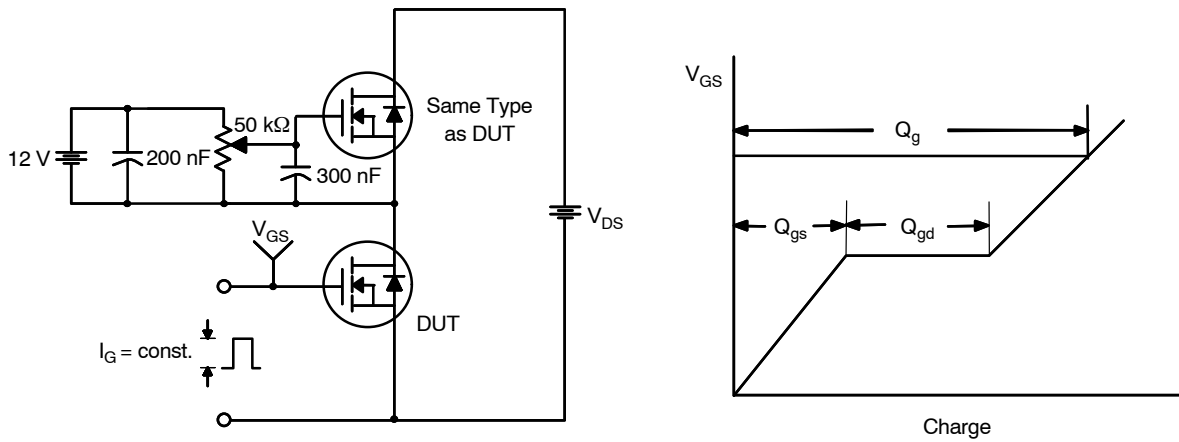


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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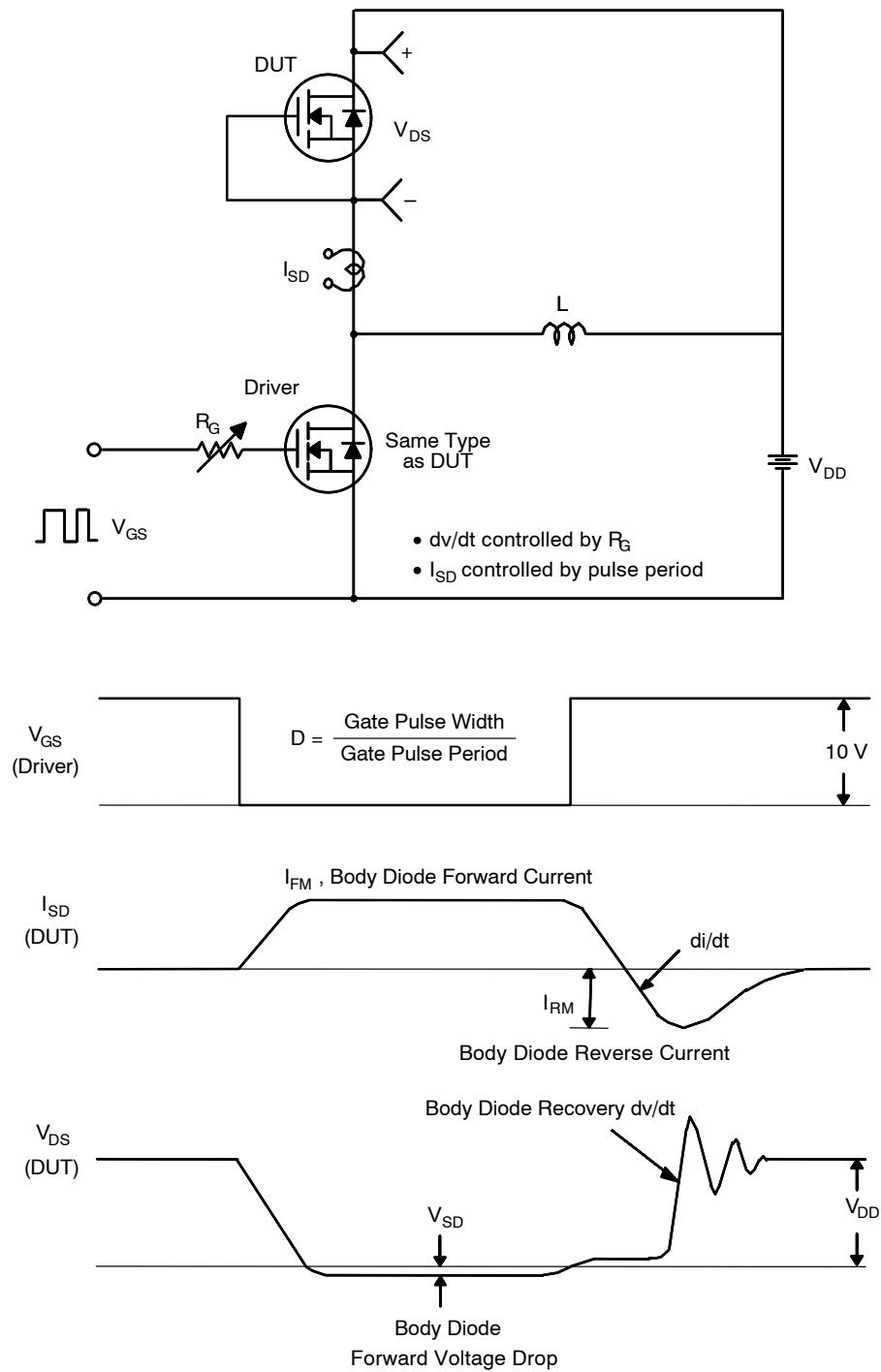
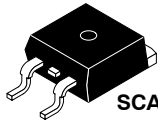


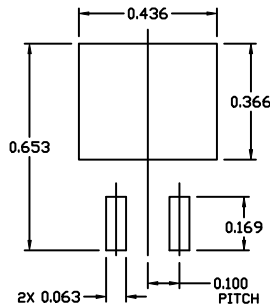
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



SCALE 1:1

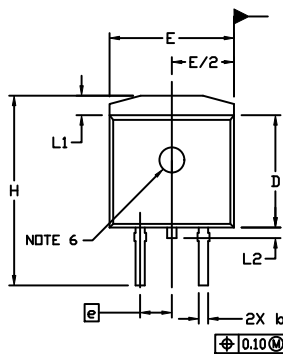
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CASE 418AJ
ISSUE F

DATE 11 MAR 2021



**RECOMMENDED
MOUNTING FOOTPRINT**

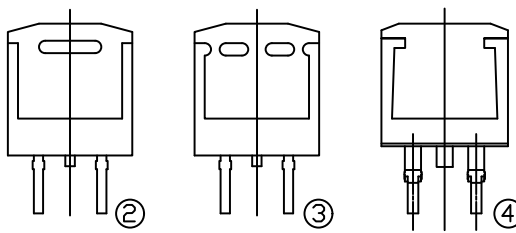
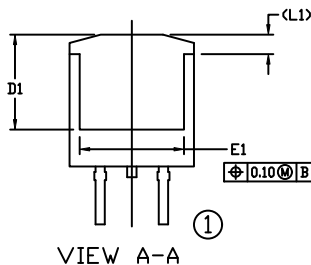
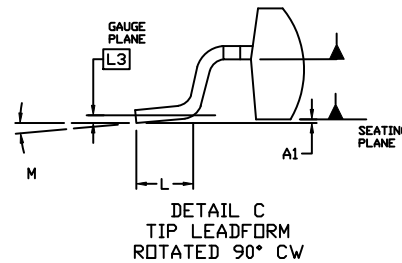
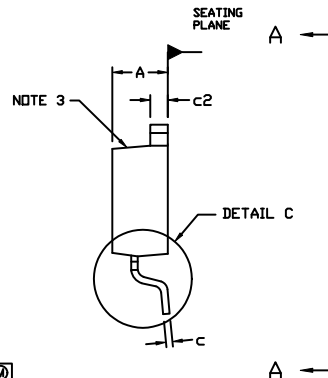
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



NOTES:

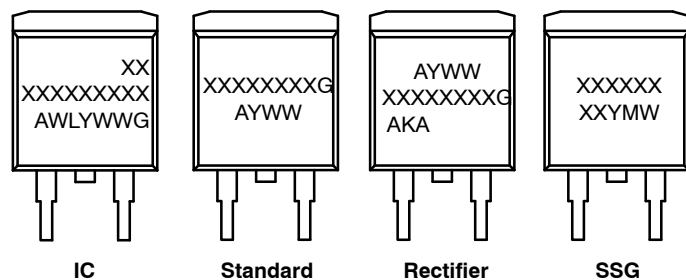
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC	---	2.54 BSC	---
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC	---	0.25 BSC	---
M	0°	8°	0°	8°



**VIEW A-A
OPTIONAL CONSTRUCTIONS**

GENERIC MARKING DIAGRAMS*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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