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# FQD13N10L / FQU13N10L

## N-Channel QFET® MOSFET

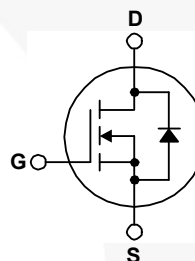
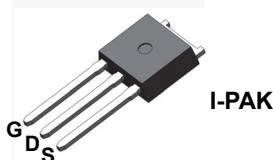
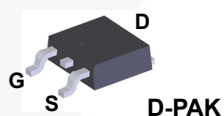
100 V, 10 A, 180 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 10 A, 100 V,  $R_{DS(on)} = 180 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 5.0 \text{ A}$
- Low Gate Charge (Typ. 8.7 nC)
- Low Crss (Typ. 20 pF)
- 100% Avalanche Tested
- Low Level Gate Drive Requirement Allowing Direct Operation Form Logic Drivers



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQD13N10LTM / FQU13N10LTU	Unit
$V_{DSS}$	Drain-Source Voltage	100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	10	A
		6.3	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	40	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	95	mJ
$I_{AR}$	Avalanche Current (Note 1)	10	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	40	W
	- Derate above $25^\circ\text{C}$	0.32	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQD13N10LTM / FQU13N10LTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.13	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD13N10LTM	FQD13N10L	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQU13N10LTU	FQU13N10L	I-PAK	Tube	N/A	N/A	70 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.09	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.0\text{ A}$	--	0.142	0.18	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 5.0\text{ A}$	--	0.158	0.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 5.0\text{ A}$	--	8.7	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	400	520	pF
$C_{oss}$	Output Capacitance		--	95	125	pF
$C_{rss}$	Reverse Transfer Capacitance		--	20	25	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 12.8\text{ A}, R_G = 25\ \Omega$	--	7.5	25	ns
$t_r$	Turn-On Rise Time		--	220	450	ns
$t_{d(off)}$	Turn-Off Delay Time		--	22	55	ns
$t_f$	Turn-Off Fall Time	(Note 4)	--	72	150	ns
$Q_g$	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 12.8\text{ A}, V_{GS} = 5\text{ V}$	--	8.7	12	nC
$Q_{gs}$	Gate-Source Charge		--	2.0	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	5.3	--

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	10	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	40	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 12.8\text{ A},$	--	75	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	0.17	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 1.43\text{ mH}, I_{AS} = 10\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 12.8\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

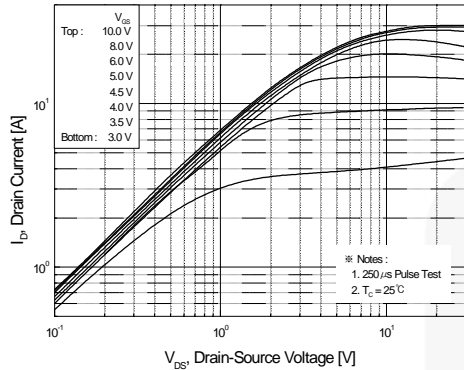


Figure 1. On-Region Characteristics

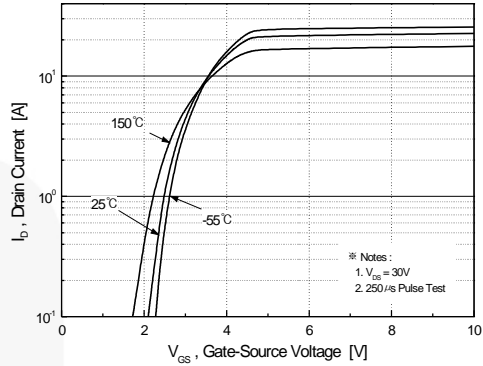


Figure 2. Transfer Characteristics

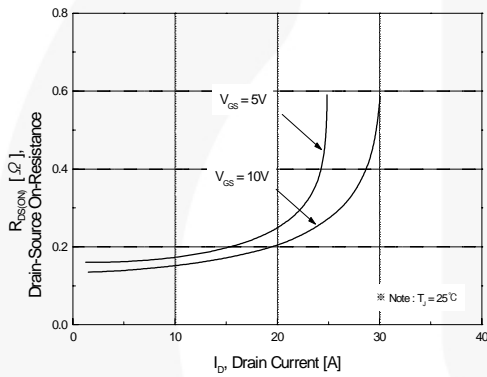


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

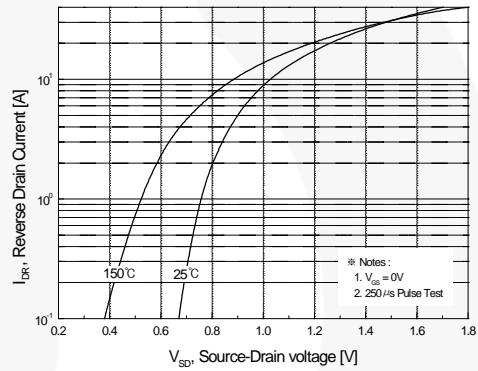


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

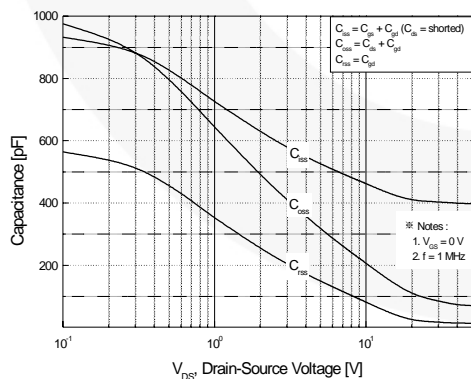


Figure 5. Capacitance Characteristics

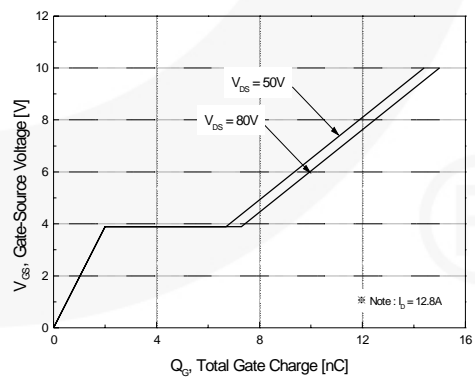
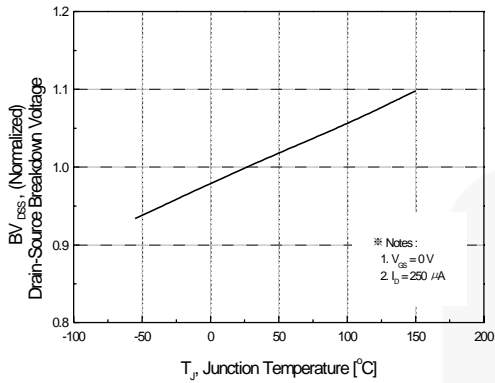
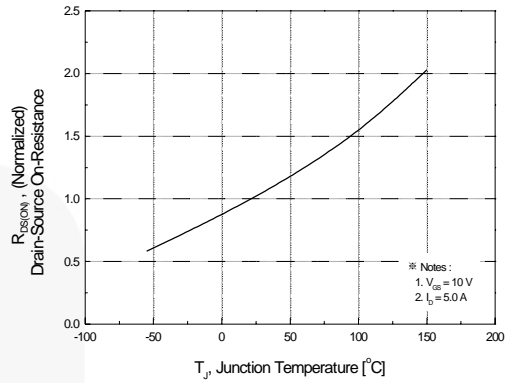


Figure 6. Gate Charge Characteristics

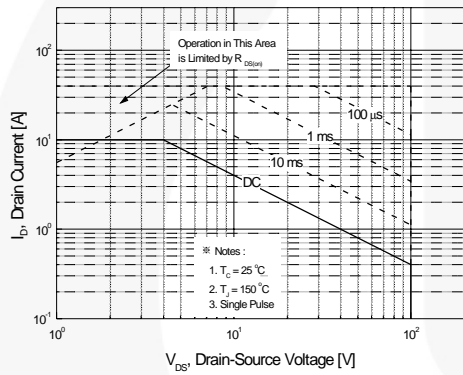
**Typical Characteristics** (Continued)



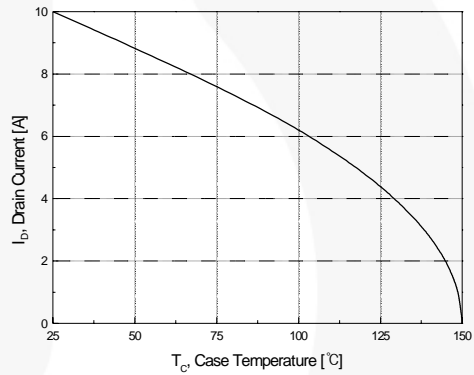
**Figure 7. Breakdown Voltage Variation vs. Temperature**



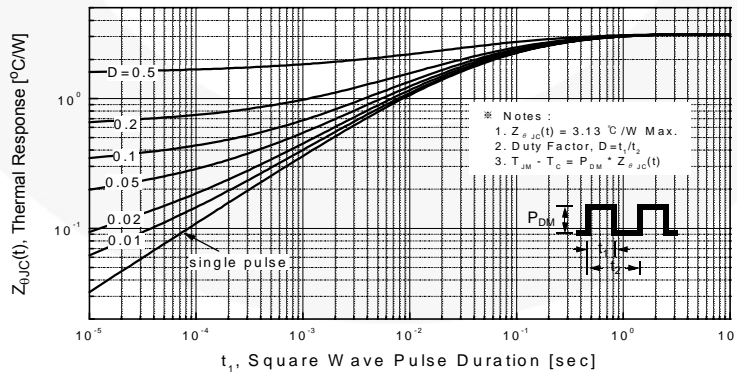
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

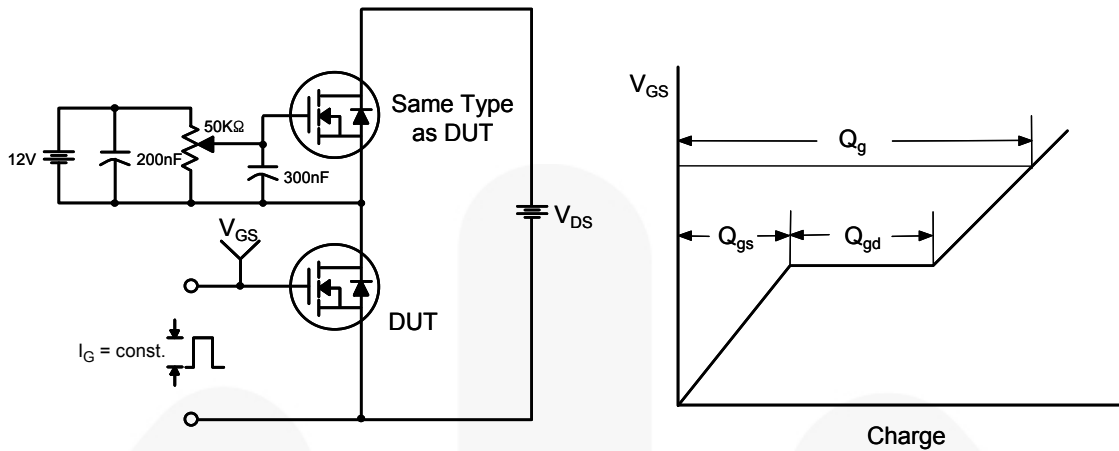


Figure 12. Gate Charge Test Circuit & Waveform

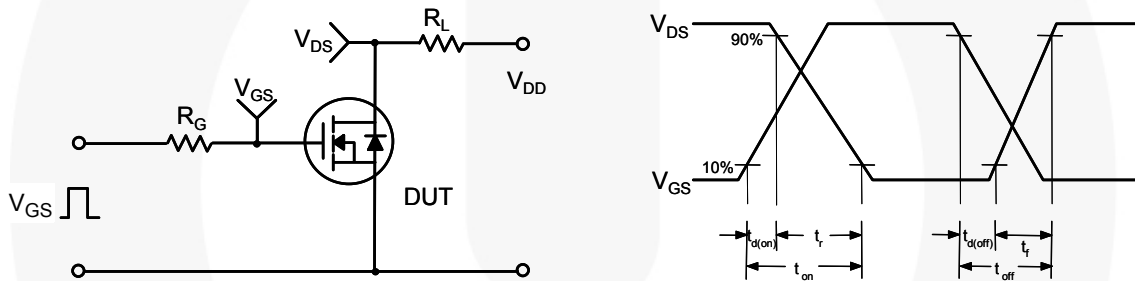


Figure 13. Resistive Switching Test Circuit & Waveforms

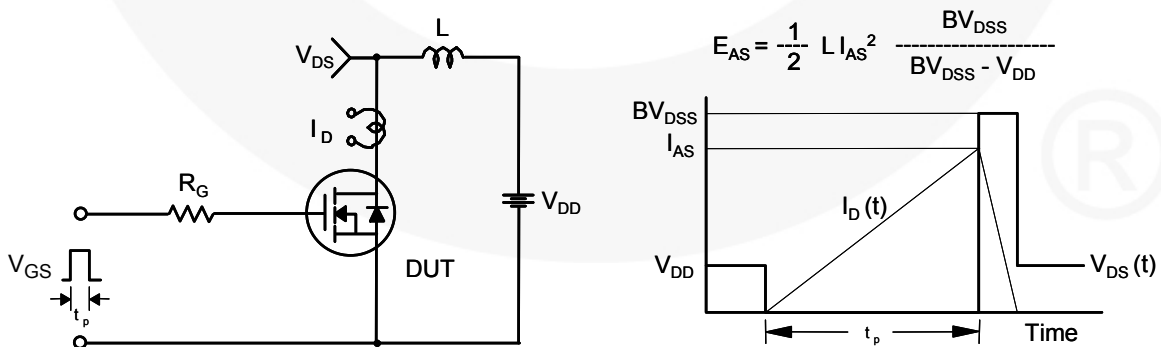
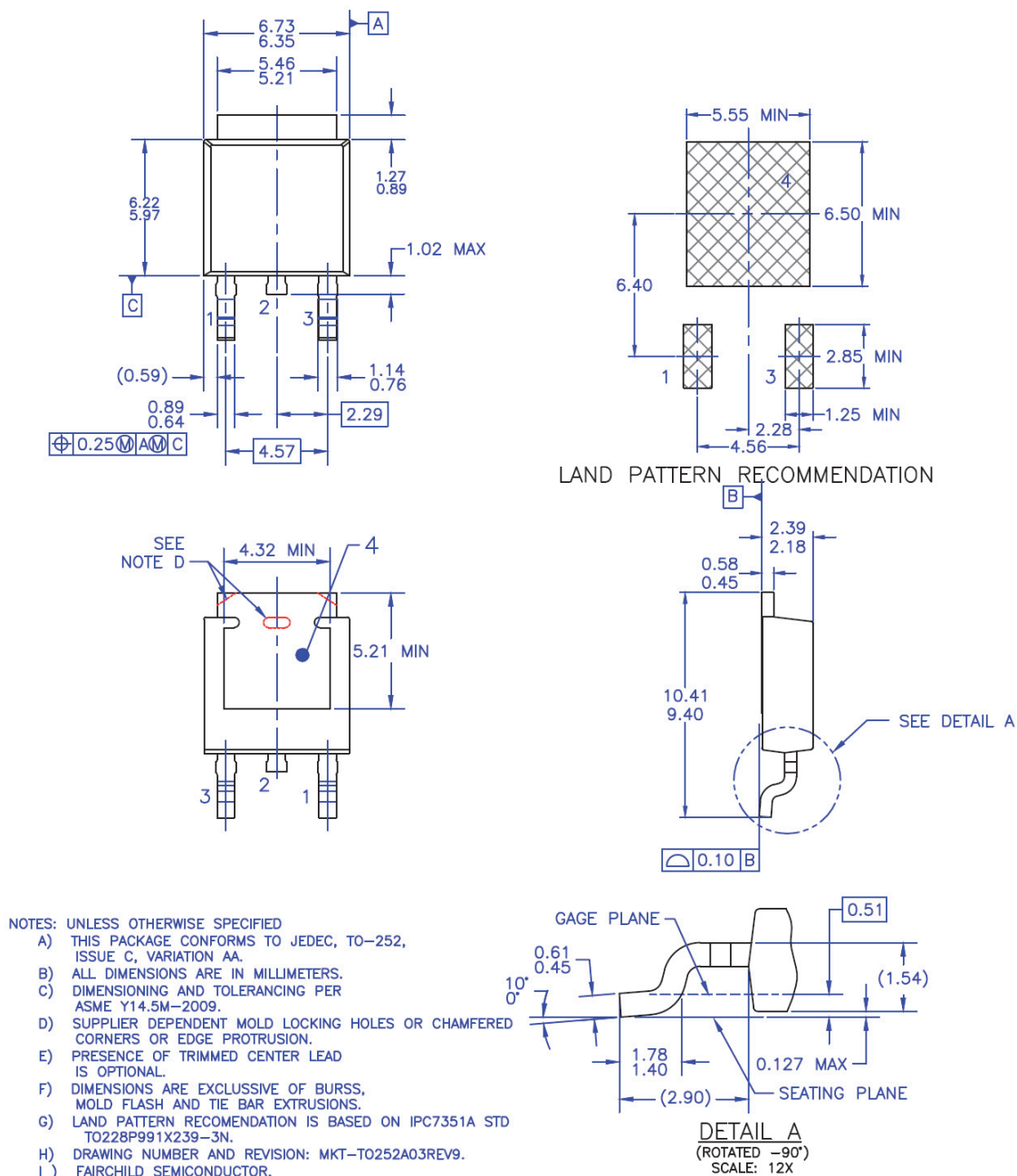


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

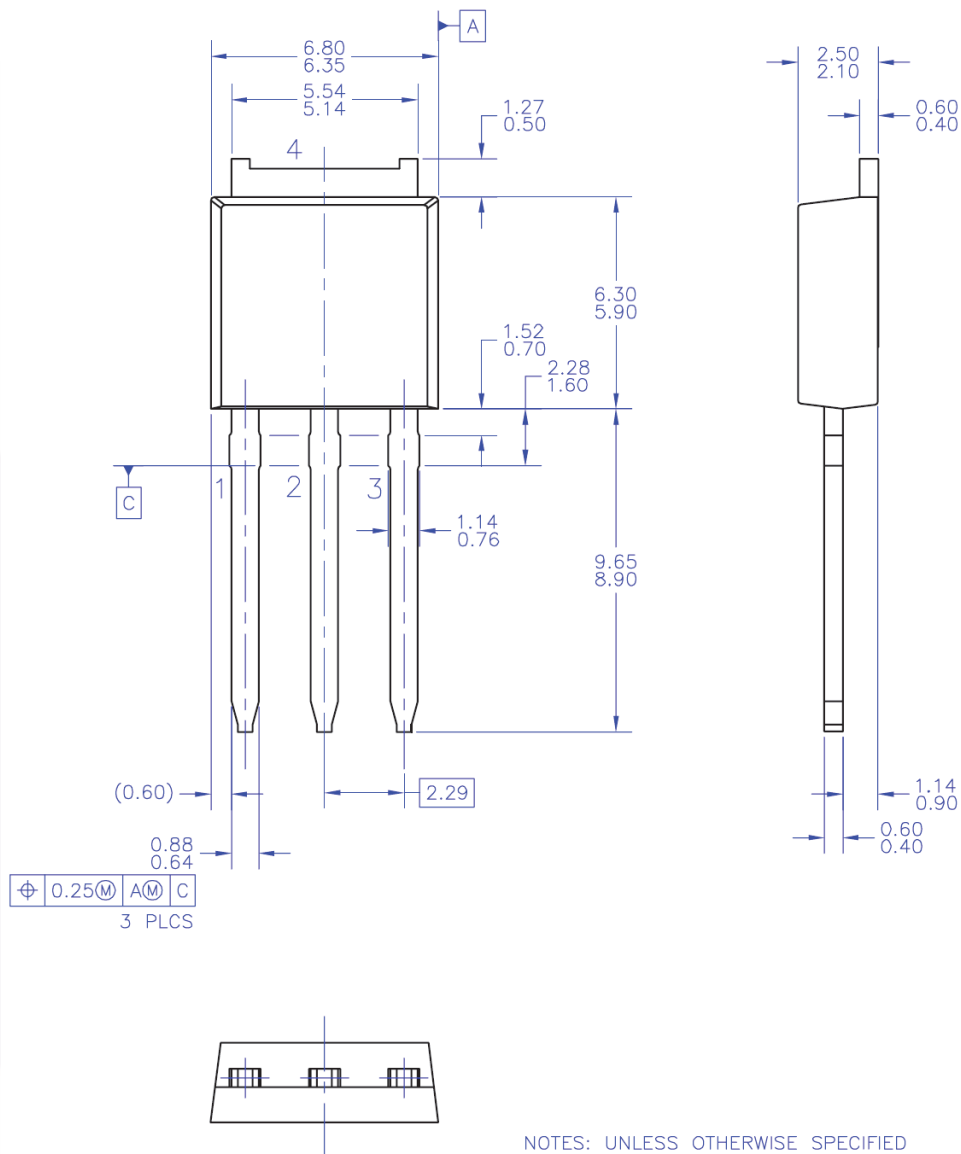
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## Mechanical Dimensions



TO251A03REVA

NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

**Figure 17. TO251 (I-PAK), Molded, 3-Lead**

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