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FSUSB46 — 带有充电器连接检测功能的高速 USB2.0 (480Mbps) 双刀单掷开关

特性

- 低导通电容: 7.0pF典型值
- 低导通电阻: 3.9Ω 典型值
- 低功耗: 1μA最大值
 - 在扩展的电压范围内($V_{IN}=1.8V$, $V_{CC}=4.3V$), 最大 I_{CC} 电流为15μA
- 宽广的 -3db带宽: > 720MHz
- 封装为无铅8-引脚MicroPak™ (1.6mm宽) 无铅8-引脚US8 (3.1mm宽), 和UMLP (1.4x1.4mm)
- 8kV的ESD, >16kV 电源对地ESD
- 当 $V_{CC}=0V$ 时所有管脚有断电保护
 - D+/D-管脚耐高压达5.25V

应用

- 手机, PDA, 数字相机, 和笔记本
- LCD显示屏, TV, 和机顶盒

描述

FSUSB46是双向低功耗双端口高速 USB2.0 开关. 结构类似于双刀单掷开关, 它对于切换一个高速源 (480Mbps) 是优化选择.

FSUSB46是兼容USB2.0要求和拥有7.0pF超低电容的特性. 元件宽广的带宽(720MHz)超过了需要通过三阶谐波的带宽, 从而可以最小化边缘和相位的失真, 超高品质的通道与通道之间的串扰特性也最小化了干扰.

FSUSB46在开关的I/O管脚包含有特殊的电路针对当 $V_{CC}=0$ 时允许元件耐过压的应用. 这个元件被设计最小化了电流消耗即使用在/OE 管脚的控制电压低于供电电压. 这种特性对手机类超便携式应用尤其重要, 通过它可以直接与基带处理器通用I/O口连接. 另外的特性是在充电器连接模式时通过对D+/D-双电平状态的有效检测从而产生一个中断信号给主芯片.

重要注解

欲知其它详情, 请联系
analogswitch@fairchildsemi.com.

订货信息

订货号码	操作温度范围	封装	 Eco Status
FSUSB46L8X	-40 至+85°C	8引脚MicroPak™ 1.6mm宽	RoHS
FSUSB46K8X	-40 至+85°C	8引脚US8, JEDEC MO187, Variation CA 3.1mm	Green
FSUSB46UMX	-40 至+85°C	8引脚 超薄模塑无脚封装(UMLP), 1.2 x 1.4mm	Green

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

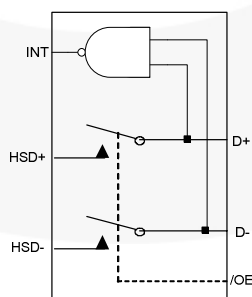


图1.模拟符号

管脚分配图

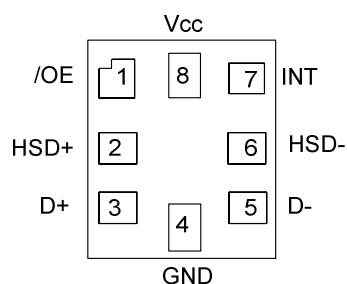


图2. MicroPak 分配图 (俯视图)

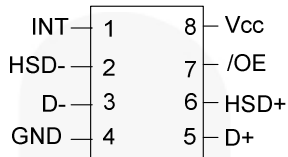


图3. US8 分配图 (俯视图)

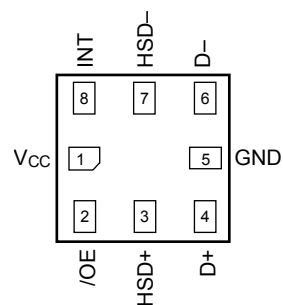


图4. UMLP (俯视图)

管脚定义

管脚名称	描述
INT	中断信号输出端
/OE	开关使能
D+, D-	USB 数据总线连接器
HSD+, HSD-	USB 源输入
GND	接地
V _{CC}	供电电源

真值表

数据通道		充电检测路径	
/OE	开关连接器	D+ D-	INT 输出
L	D+, D- = 断开	1-1	低电平
H	D+, D- = HSD+, HSD-	0X, X0	高电平

最大绝对额定值

超出绝对最大额定值会破坏设备，设备会不工作或者说不建议设备在和超过建议的工作条件下被操作。另外，过长的暴露在超过建议工作条件下会影响设备的可靠性，这种绝对最大额定值仅仅是极端额定值。

表达符号	参数	最小值	最大值	单位	
V _{CC}	供电电压	-0.5	+5.5	V	
V _{CNTRL}	DC输入电压(S) ⁽¹⁾	-0.5	V _{CC}	V	
V _{SW}	DC 开关输入/出电压 ⁽¹⁾	-0.50	5.25	V	
I _{IK}	DC输出钳位电流	-50		mA	
I _{OUT}	DC输出电流		50	mA	
T _{STG}	储存温度	-65	+150	°C	
ESD	人体电流模式, JEDEC: JESD22-A114	所有管脚		7	kV
		I/O对地		8	
		电源对地		16	
	充放电模式, JEDEC: JESD22-C101		2		

注解:

- 如输入及输出二极管电流额定值均达到时则可能会超出输入及输出负额定值。

推荐工作条件

推荐工作条件表中定义的是实际元件工作的条件，推荐工作条件指定用于保证实现数据表规范的最佳性能，Fairchild 建议不得超出以上值或设计至最大绝对额定值。

表达符号	参数	最小值	最大值	单位
V _{CC}	供电电压	3.0	4.3	V
V _{CNTRL}	控制输入电压(/OE) ⁽²⁾	0	V _{CC}	V
V _{SW}	开关 I/O电压	-0.5	V _{CC}	V
T _A	操作温度	-40	+85	°C

注解:

- 控制输入必须保持高平或低平且不得悬空。

DC 电气特性

如未说明均为25°C, 3.3V V_{CC} 下的标准值.

表达符号	参数	条件	V_{CC} (V)	$T_A = -40^{\circ}\text{C}$ 至 $+85^{\circ}\text{C}$			单位
				最小	典型	最大	
V_{IK}	钳位二极管电压	$I_{IN} = -18\text{mA}$	3.0			-1.2	V
V_{IH}	输入高电平		3.0 至 3.6	1.3			V
			4.3	1.7			V
V_{IL}	输入低电平		3.0 至 3.6			0.5	V
			4.3			0.7	V
V_{OH}	输出高电平	$I_{OH} = -2\text{mA}$	3.0 至 3.6	2.4			V
			4.3	2.4			V
V_{OL}	输出低电平	$I_{OL} = 2\text{mA}$	3.0 至 3.6			0.25	V
			4.3			0.25	V
I_{IN}	控制输入漏电流	$V_{SW} = 0$ 至 V_{CC}	4.3	-1		1	μA
I_{OZ}	断开漏电流	HSD+或 HSD=0V, 3.6V或悬浮	4.3	-2		2	μA
I_{OFF}	断电漏电流(所有I/O端口)	$V_{SW} = 0\text{V}$ 至 4.3V , $V_{CC} = 0\text{V}$ 图6	0	-2		2	μA
R_{ON}	高速开关导通电阻 ⁽³⁾	$V_{SW} = 0.4\text{V}$, $I_{ON} = -8\text{mA}$ 图5	3.0		3.9	6.5	Ω
ΔR_{ON}	高速导通电阻差 ⁽⁴⁾	$V_{SW} = 0.4\text{V}$, $I_{ON} = -8\text{mA}$	3.0		0.65		Ω
I_{CC}	静态供电电流	$V_{CNTRL} = 0$ 或 V_{CC} , $I_{OUT} = 0$	4.3			1.0	μA
I_{CCT}	控制电压和 V_{CC} 增加时 I_{CC} 相应的增加量	$V_{CNTRL} = 2.6\text{V}$, $V_{CC} = 4.3\text{V}$	4.3			10.0	μA
		$V_{CNTRL} = 1.8\text{V}$, $V_{CC} = 4.3\text{V}$	4.3			15.0	μA

注

- 在开关指定电流下通过测量管脚HSDn和Dn管脚之间的电压降获得. 导通电阻由两管脚上较低的电压决定.
- 由特性保证.

AC电气特性

如未说明均为25°C, 3.3V V_{CC}下的标准值.

表达符号	参数	条件	V _{CC} (V)	T _A =- 40°C to +85°C			单位
				最小	典型	最大	
t _{ON}	开启时间 /OE到输出	R _L =50Ω, C _L =5pF V _{SW} =0.8V 图7,8	3.0 至 3.6		13	30	ns
t _{OFF}	关断时间 /OE到输出	R _L =50Ω, C _L =5pF V _{SW} =0.8V 图7,8	3.0 至 3.6		12	25	ns
t _{PD}	传播延迟 ⁽⁵⁾	C _L =5 pF, R _L =50Ω 图7,9	3.3		0.25		ns
t _{BBM}	先断后开	R _L =50Ω, C _L =5pF V _{SW1} =V _{SW2} =0.8V 图13	3.0 至 3.6	2.0		6.5	ns
t _{PLH/HL}	INT传播延迟 ⁽⁵⁾	R _L =500Ω, C _L =5pF	3.0 至 3.6		5.0		ns
O _{IRR}	隔离度	R _L = 50Ω, f=240MHz 图15	3.0 至 3.6		-30		dB
Xtalk	非相邻通道串扰	R _L =50Ω, f=240MHz 图16	3.0 至 3.6		-45		dB
BW	-3db带宽	R _L =50Ω, C _L =0pF 图14	3.0 至 3.6		720		MHz
		R _L =50Ω, C _L =5pF 图14			550		MHz

注:

5. 由特性保证.

与USB高速相关的AC电气特性

表达符号	参数	条件	V _{CC} (V)	T _A =- 40°C至 +85°C			单位
				最小	典型	最大	
t _{SK(P)}	同一输出相反传输方向上的偏差 ⁽⁶⁾	C _L =5pF, R _L =50Ω 图10	3.0 至 3.6		20		ps
t _J	总抖动 ⁽⁶⁾	R _L =50Ω, C _L =5pf, t _R =t _F =500ps (10-90%) 在 480Mbps时 (PRBS=2 ¹⁵ - 1)	3.0 至 3.6		200		ps

注:

6. 由特性保证.

电容

表达符号	参数	条件	T _A =- 40°C至 +85°C			单位
			最小	典型	最大	
C _{IN}	控制管脚输入电容	V _{CC} =0V		1.5		pF
C _{OUT}	INT管脚输出电容	V _{CC} =0V		2.5		pF
C _{ON}	D+, D- 导通电容	V _{CC} =3.3V, f=1MHz 图12		7.0	7.9	pF
C _{OFF}	D+, D- 端开电容	V _{CC} =3.3V 图11		2.0		pF

测试图

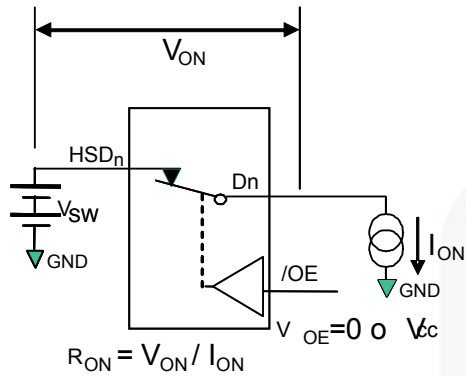


图5. 导通电阻

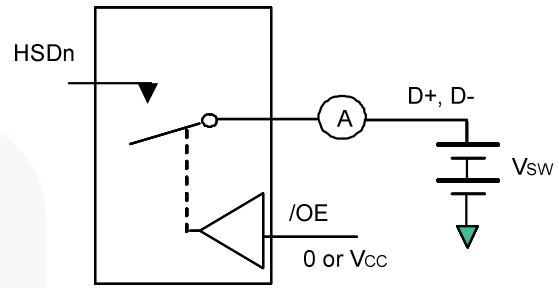


图6. 漏电流

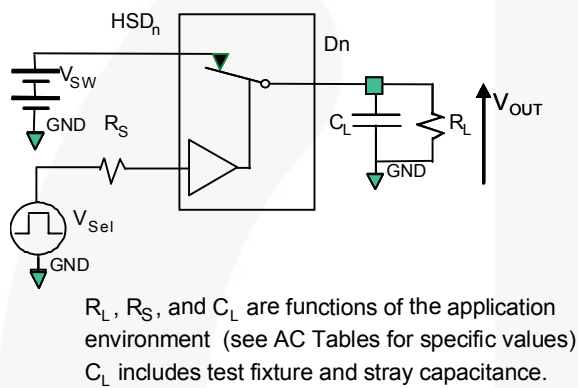


图7. AC测试电路负载

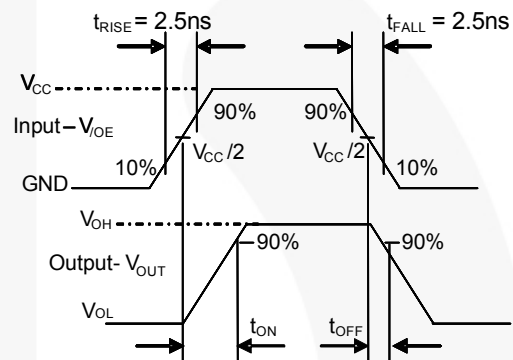


图8. 开启/关断波形

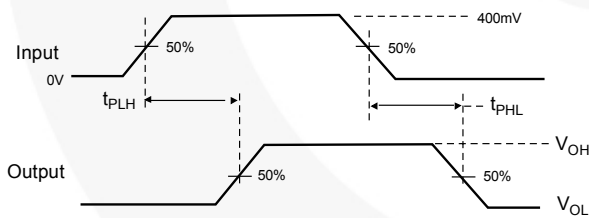


图9. 传播延迟 ($t_{rF} = 500ps$)

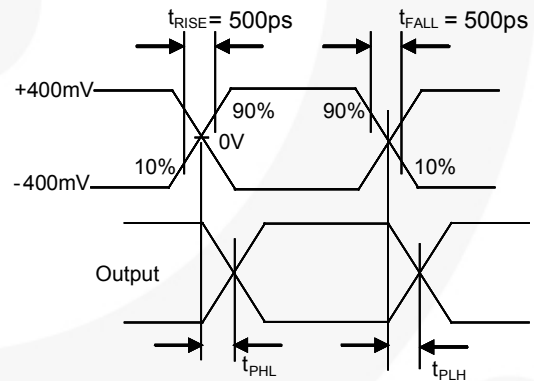


图10. 对内偏移测试 $t_{SK(P)}$

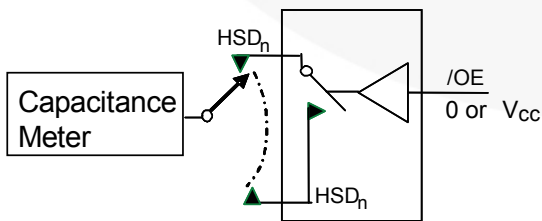


图11. 通道断开电容

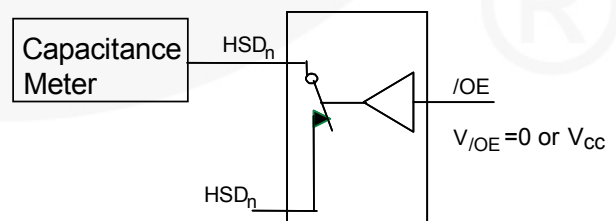
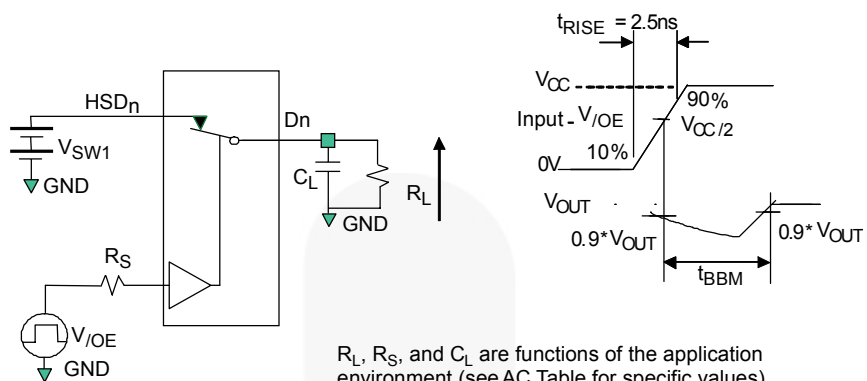


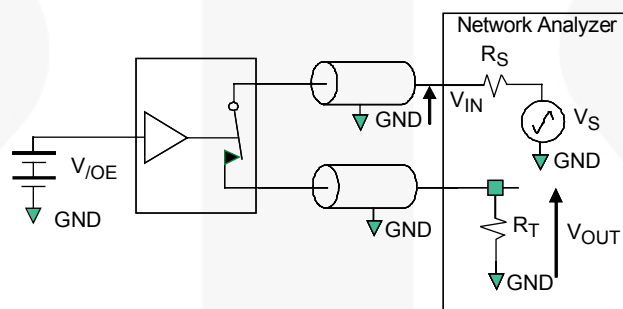
图12. 通道导通电容

测试图(续)



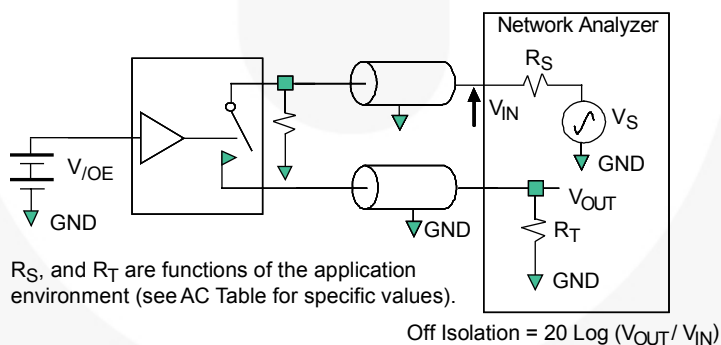
R_L , R_S , and C_L are functions of the application environment (see AC Table for specific values). C_L includes text figure and stray capacitance.

图13. 先断后开间隔时间



R_S , and R_T are functions of the application environment (see AC Table for specific values).

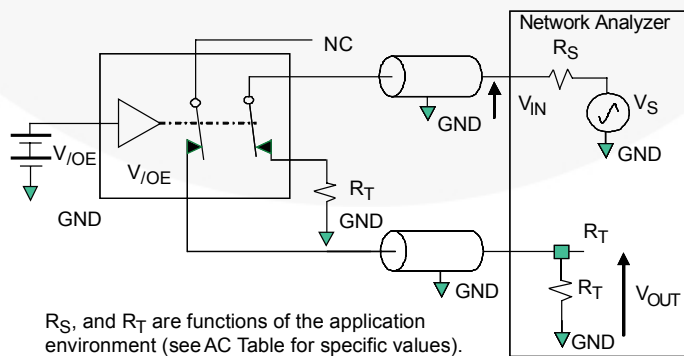
图14. 带宽



R_S , and R_T are functions of the application environment (see AC Table for specific values).

$$\text{Off Isolation} = 20 \text{ Log } (V_{OUT} / V_{IN})$$

图15. 通道隔离度

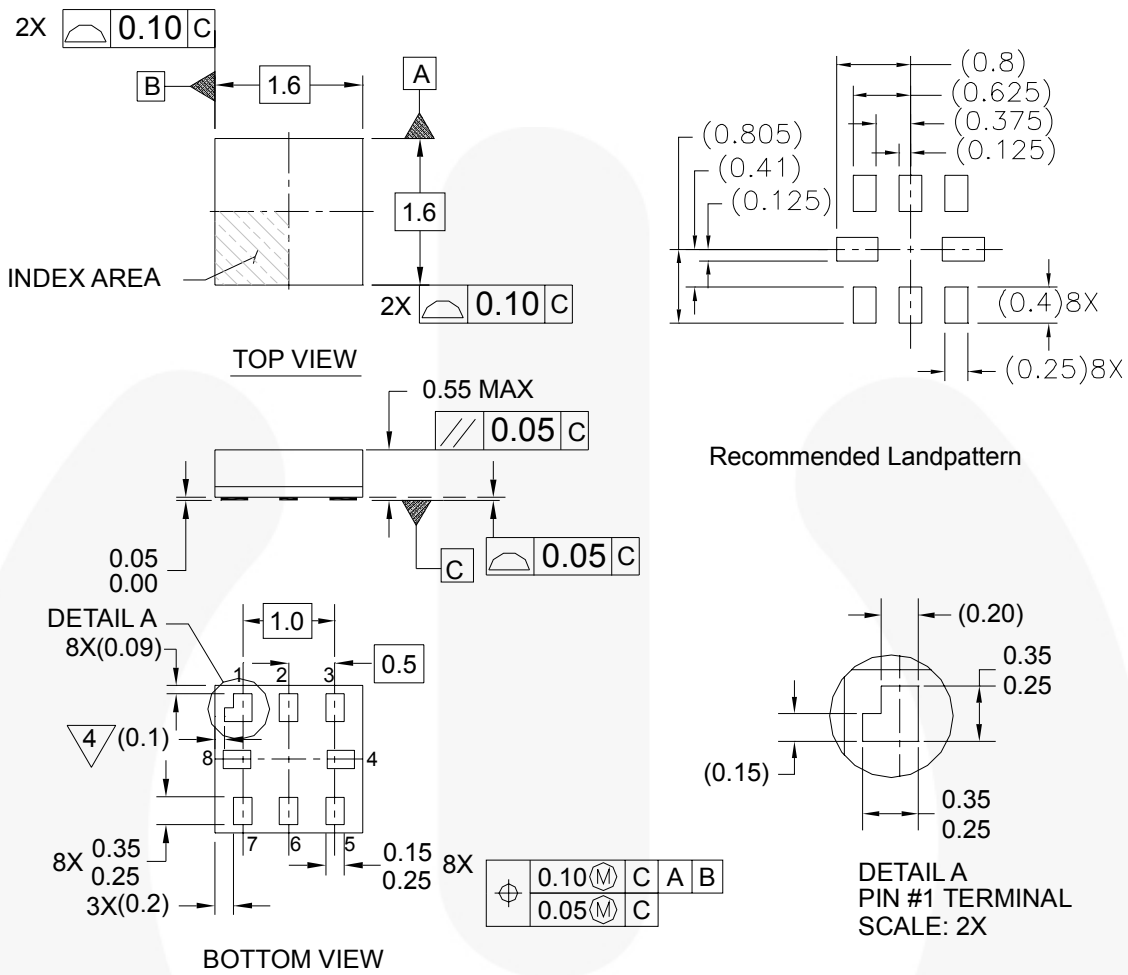


R_S , and R_T are functions of the application environment (see AC Table for specific values).

$$\text{Crosstalk} = 20 \text{ Log } (V_{OUT} / V_{IN})$$

图16. 非相邻通道串扰

物理尺寸



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

图17. 8-引脚的MicroPak™

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.

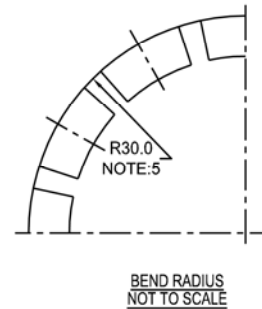
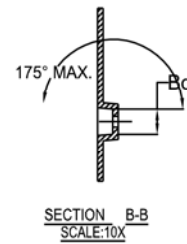
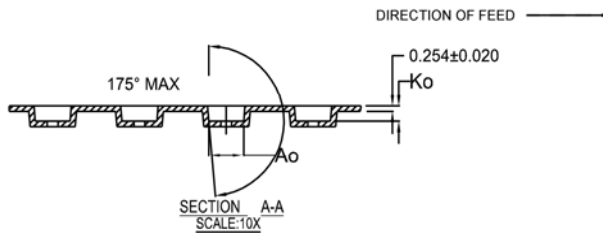
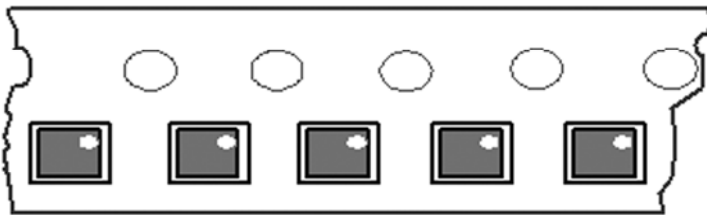
Tape and Reel Specifications

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Tape Status
L6X, L8X, L10X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Standard Tape and Reel Specifications

Standard tape and reel specifications for MicroPak are available at Fairchild Semiconductor's website:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

FSUSB46L8X_F130 Tape and Reel Specifications



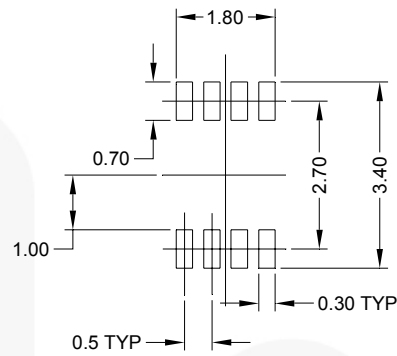
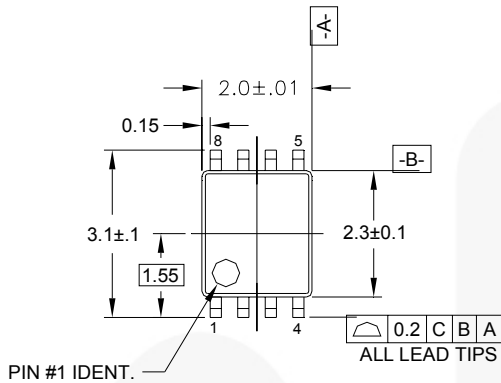
SCALE: 6X

NOTES: UNLESS OTHERWISE SPECIFIED

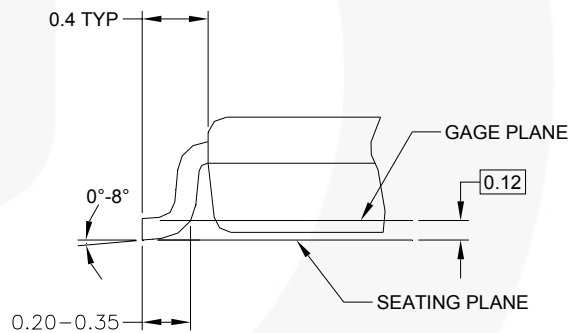
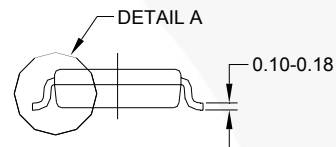
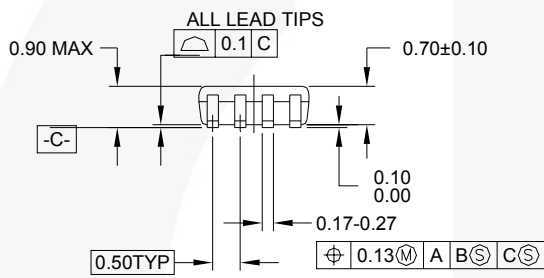
1. ACCUMULATED 50 SPROCKETS, SPROCKET HOLE PITCH IS 200.00 ±0.30MM
2. NO INDICATED CORNER RADIUS IS 0.127MM
3. CAMBER NOT TO EXCEED 1MM IN 100MM
4. SMALLEST ALLOWABLE BENDING RADIUS
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

10	30056	2.30 ± 0.1mm	1.78 ± 0.1mm	0.68 ± 0.1mm
8	30038	1.78 ± 0.1mm	1.78 ± 0.1mm	0.68 ± 0.1mm
6	30033	1.60 ± 0.1mm	1.15 ± 0.1mm	0.70 ± 0.1mm

物理尺寸



LAND PATTERN RECOMMENDATION



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

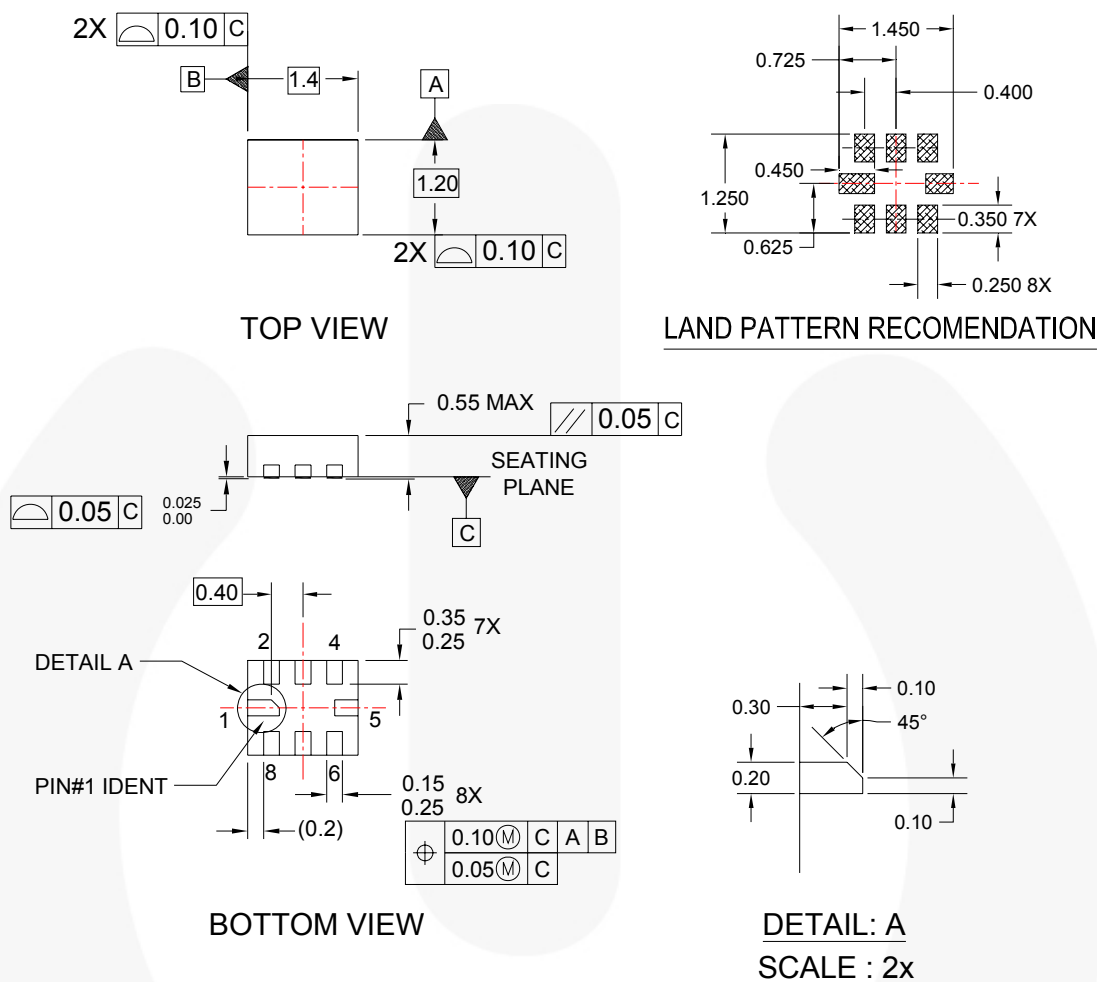
图18. 8-引脚US8, JEDEC MO-187

Tape and reel specifications are available at Fairchild Semiconductor's website:
<http://www.fairchildsemi.com/ms/MS/MS-522.pdf>.

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物理尺寸



NOTES:

- A. DOES NOT CONFORMS TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES CONFORMS TO ASME Y14.5M, 1994.
- D. DRAWING FILE NAME : UMLP08Arev1

图19. 8-引脚 超薄模塑无脚封装 (UMLP), 1.2 x 1.4mm

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