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DATA SHEET
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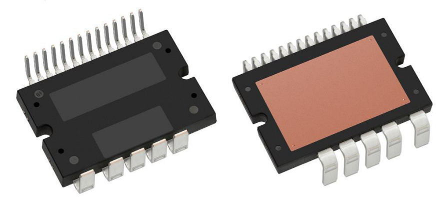
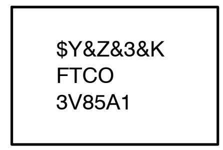
3-Phase Automotive Power Module for DC-DC Converter

FTCO3V85A1



19LD, APM, PDD STD 9
(APM19−CBC)
CASE MODCD

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FTCO3V85A1	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

General Description

The FTCO3V85A1 is an 80 V low Rds(on) automotive qualified power module, featuring a 3−phase MOSFET bridge optimized for Automotive 48 V−12 V interleaved DC−DC converter system, it includes a precision shunt resistor for current sensing, an NTC for temperature sensing, and an RC snubber circuit.

The module utilizes ON's trench MOSFET technology and it is designed to provide a very compact and high efficiency solution for DC−DC converter system. The Power module is 100% lead free, RoHS and UL compliant.

Features

- 3−Phase 1.5 kW 48 V−12 V Interleaved DC−DC Converter
- 80 V−125 A Trench MOSFET's for High−Side
  80 V−160 A Trench MOSFET for Low−Side
- Precise Shunt Current Sensing
- Temperature Sensing
- DBC Substrate
- 100% Lead Free and RoHS Compliant 2000/53/C Directive
- UL94V−0 Compliant
- Isolation Rating of 2500 Vrms/min
- Mounting Through Screws
- Automotive Qualified

Benefits

- Low Junction−Sink Thermal Resistance
- Low Power Loss for High Efficiency in DC−DC System Design
- Low Electrical Resistance
- Compact DC−DC Converter Design
- Highly Integrated Compact Design
- Better EMI and Electrical Isolation
- Easy and Reliable Installation
- High Current Handling
- Improved Overall System Reliability

Applications

- DC−DC Converter

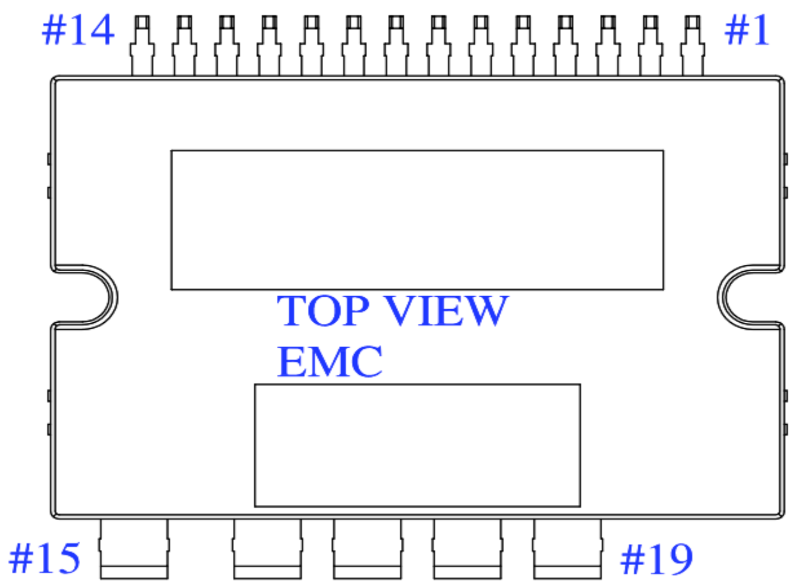


Figure 1. Pin Configuration

Table 1. PIN DESC

Pin No.	Pin Number	Pin Description
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE 3 SENSE	Source of Q3 and Drain of Q6
4	GATE 3	Gate of Q3, high side Phase 3 MOSFET
5	GATE 6	Gate of Q6, low side Phase 3 MOSFET
6	PHASE 2 SENSE	Source of Q2 and Drain of Q5
7	GATE 2	Gate of Q2, high side Phase 2 MOSFET
8	GATE 5	Gate of Q5, low side Phase 2 MOSFET
9	PHASE 1 SENSE	Source of Q1 and Drain of Q4
10	GATE 1	Gate of Q1, high side Phase 1 MOSFET
11	VBAT SENSE	Sense pin for battery voltage and Drain of high side MOSFETs
12	GATE 4	Gate of Q4, low side Phase 1 MOSFET
13	SHUNT P	Positive CSR sense pin and source connection for low side MOSFETs
14	SHUNT N	Negative CSR sense pin and sense pin for battery return
15	VBAT	Battery voltage power lead
16	GND	Battery return power lead
17	PHASE 1	Phase 1 power lead
18	PHASE 2	Phase 2 power lead
19	PHASE 3	Phase 3 power lead

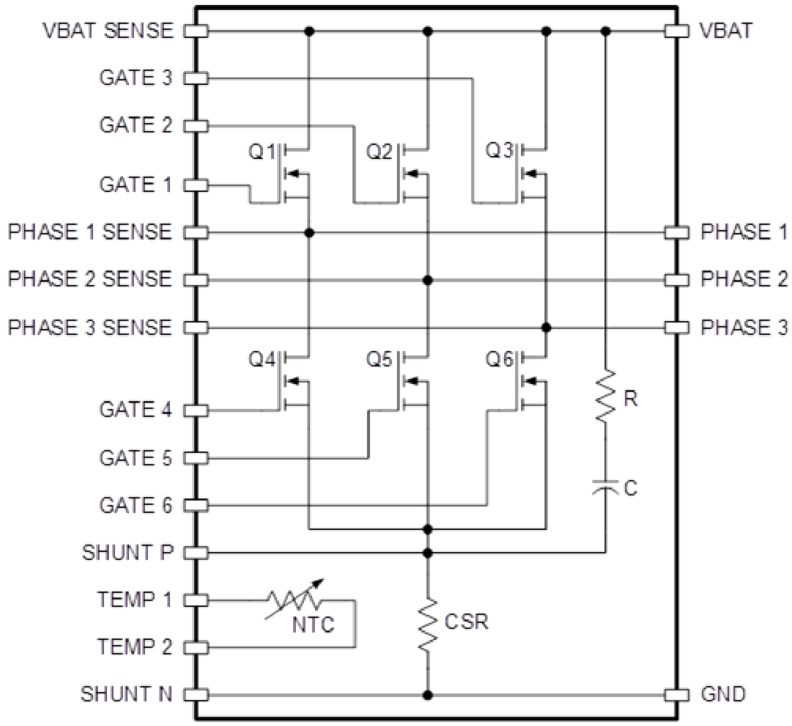


Figure 2. Internal Equivalent Circuit

Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0 or higher.

Solder

Solder used is a lead free SnAgCu alloy.

Compliance to RoHS

The Power Module is 100% lead free and RoHS compliant with the 2000/53/C directive.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	FTCO3V85A1	Unit
V_{DS}(Q1~Q6)	Drain to Source Voltage	80	V
V_{GS}(Q1~Q6)	Gate to Source Voltage	±20	V
I_D(high−side)	Drain Current Continuous (T_C = 25°C, T_J = 175°C, V_{GS} = 10 V) (Note 1)	125	A
I_D(low−side)	Drain Current Continuous (T_C = 25°C, T_J = 175°C, V_{GS} = 10 V) (Note 1)	160	A
E_{AS}(Q1~Q3)	Single Pulse Avalanche Energy (Note 2)	190	mJ
E_{AS}(Q4~Q6)	Single Pulse Avalanche Energy (Note 2)	324	mJ
P_D(high−side)	Power dissipation (T_C = 25°C, T_J = 175°C)	115	W
P_D(low−side)	Power dissipation (T_C = 25°C, T_J = 175°C)	135	W
T_J	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature	125	°C

THERMAL RESISTANCE

Symbol	Parameter	Min.	Typ.	Max.	Unit
Rthjc Thermal Resistance Junction to case, Single FET, (Note 3)	Q1 Thermal Resistance J −C	–	1.0	1.3	°C/W
	Q2 Thermal Resistance J −C	–	1.0	1.3	°C/W
	Q3 Thermal Resistance J −C	–	1.0	1.3	°C/W
	Q4 Thermal Resistance J −C	–	0.8	1.1	°C/W
	Q5 Thermal Resistance J −C	–	0.8	1.1	°C/W
	Q6 Thermal Resistance J −C	–	0.8	1.1	°C/W
T_J	Maximum Junction Temperature	–		175	°C
T_S	Operating Sink Temperature	−40		120	°C
TSTG	Storage Temperature	−40		125	°C

1. Max value not to exceed Tj=175°C based on max limitation of Rthjc thermal limitation and Rdson. Defined by design, not subject production testing.
2. For Q1−Q3: Starting TJ = 25°C, L = 0.08mH, IAS = 69 A, VDD = 80 V during inductor charging and VDD = 0 V during time in avalanche. For Q4−Q6: Starting TJ = 25°C, L = 0.08 mH, IAS = 90 A, VDD = 80 V during inductor charging and VDD = 0 V during time in avalanche.
3. Test method compliant with MIL STD 883−1012.1.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	D–S Breakdown Voltage (Inverter MOSFETs)	V_{GS} = 0V, I_D = 250 μA	80	–	–	V
V_{GS}	Gate to Source Voltage (Inverter MOSFETs)	Gate–to–Source Voltage	−20	–	20	V
V_{TH}	Threshold Voltage (Q1–Q6)	$V_{GS} = V_{DS}$, I_D = 250 μA, T_J = 25°C	2	3	4	V
V_{SD}	MOSFET Body Diode Forward Voltage	V_{GS} = 0 V, I_S = 80 A, T_J = 25°C	–	–	1	V
$R_{DS(ON)Q1}$	Inverter High Side MOSFETs Q1 (See Note 4)	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	2.4	3.5	mΩ
$R_{DS(ON)Q2}$	Inverter High Side MOSFETs Q2 (See Note 4)	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	2.4	3.5	mΩ
$R_{DS(ON)Q3}$	Inverter High Side MOSFETs Q3 (See Note 4)	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	2.5	3.7	mΩ
$R_{DS(ON)Q4}$	Inverter Low Side MOSFETs Q4 (See Note 4)	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	1.9	2.6	mΩ
$R_{DS(ON)Q5}$	Inverter Low Side MOSFETs Q5 (See Note 4)	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	2.1	2.8	mΩ
$R_{DS(ON)Q6}$	Inverter Low Side MOSFETs Q6 (See Note 4)	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	2.4	3.1	mΩ
I_{GSS}	Inverter MOSFETs (UH,UL,VH,VL,WH,WL)	V_{GS} = ±20 V, V_{DS} = 0 V, T_J = 25°C	–	–	±100	nA
I_{DSS}	Inverter MOSFETs Drain to Source Leakage Current	V_{GS} = 0 V, V_{DS} = 80 V, T_J = 25°C	–	–	2	μA
Total loop resistance VLINK(+) – V0 (–)		V_{GS} = 10 V, I_D = 80 A, T_J = 25°C	–	5.9	7.5	mΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. High side Q1,Q2,Q3 have same die size and Rdson, Low side Q4,Q5,Q6 have same die size and Rdson. For lowest power loss, High and Low side MOSFETs have different die size and Rdson. The different Rdson values listed in the datasheet are due to the different access points available inside the module for Rdson measurement. While the high side MOSFETs (Q1, Q2, Q3) have source sense wire bonds, the low side MOSFETs (Q4, Q5, Q6) do not have source sense wire bonds, thus resulting in higher Rdson values.

TEMPERATURE SENSE (NTC THERMISTOR)

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Voltage	Current = 1 mA, Temperature = 25°C	7.5	–	12	V

CURRENT SENSE RESISTOR

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Voltage	Current sense resistor current = 80 A (Note 5)	0.47	–	0.51	mΩ

	Components	Spec	Quantity	Size
1	MOSFET	PT7 80 V,bare die Rdson 2.25 mΩ typical	3ea (Q1–Q3)	195 mil x 95 mil
2	MOSFET	PT7 80 V,bare die Rdson 1.35 mΩ typical	3ea (Q4–Q6)	200 mil x 145 mil
3	Resistor	1 Ω 0.5 W	1ea	142 mil x 55 mil
4	Capacitor	0.022 μF 100 V	1ea	79 mil x 49 mil
5	CSR	1% tolerance, 0.5 mΩ	1ea	250 mil x 120 mil
6	NTC	1% tolerance, 10 kΩ	1ea	63 mil x 32 mil

DYNAMIC CHARACTERISTIC

Symbol	Parameter	Min	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MH_Z for Q1–Q3 (High side MOSFET)		–	6320	–	pF
C_{oss}	Output Capacitance			–	1030	–	pF
C_{rss}	Reverse Transfer Capacitance			–	32	–	pF
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MH_Z for Q4–Q6 (Low side MOSFET)		–	10000	–	pF
C_{oss}	Output Capacitance			–	1400	–	pF
C_{rss}	Reverse Transfer Capacitance			–	95	–	pF
R_G	Gate Resistance	V_{GS} = 0V, f = 1MH_Z for Q1–Q3 (High side MOSFET)		–	2.1	–	Ω
R_G	Gate Resistance	V_{GS} = 0V, f = 1MH_Z for Q4–Q6 (Low side MOSFET)		–	3.3	–	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10 V	VGS = 0 to 10 V	V_{DD} = 64 V I_D = 80 A I_g = 1 mA	–	86	112	nC
$Q_{g(TH)}$	Threshold Gate Charge	VGS = 0 to 2 V		–	12	18	nC
Q_{gs}	Gate to Source Gate Charge	For Q1–Q3 (High side MOSFET)		–	30	–	nC
Q_{gd}	Gate to Drain “Miller” Charge			–	18	–	nC
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V	V_{DD} = 64 V I_D = 80 A I_g = 1 mA	–	131	150	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V		–	18	21	nC
Q_{gs}	Gate to Source Gate Charge	For Q4–Q6 (Low side MOSFET)		–	47	–	nC
Q_{gd}	Gate to Drain “Miller” Charge			–	24	–	nC

TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86366_F085 (TOLL) Datasheet (High side MOSFET)

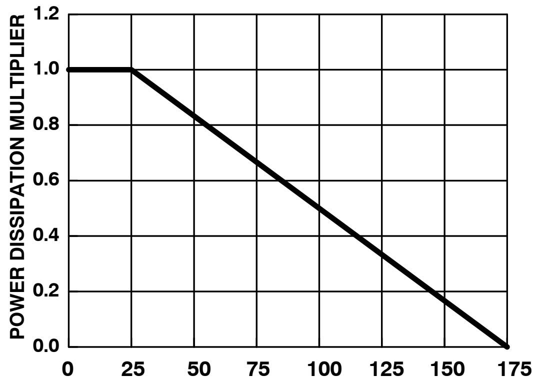


Figure 3. Normalized Power Dissipation vs. Case Temperature

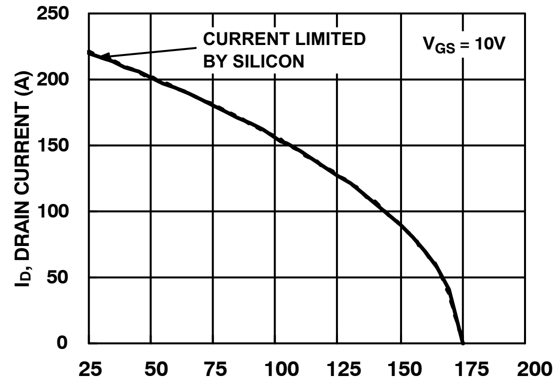


Figure 4. Maximum Continuous Drain Current vs. Case Temperature

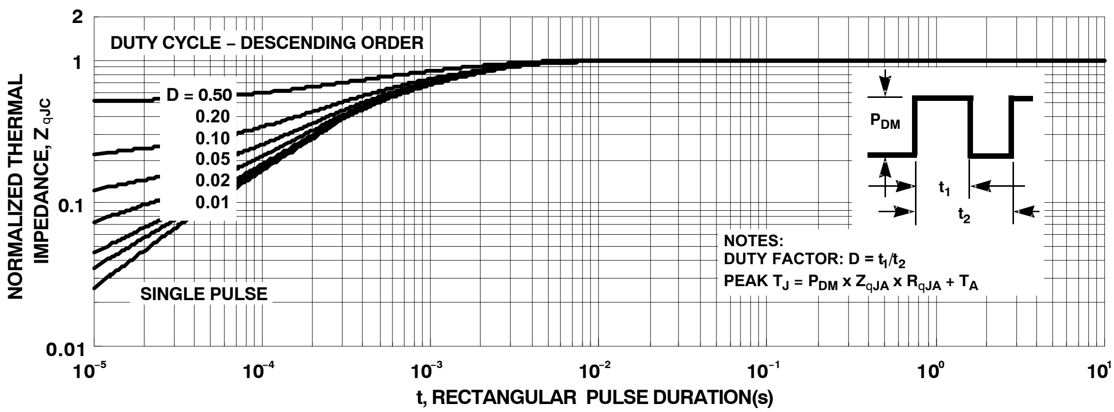


Figure 5. Normalized Maximum Transient Thermal Impedance

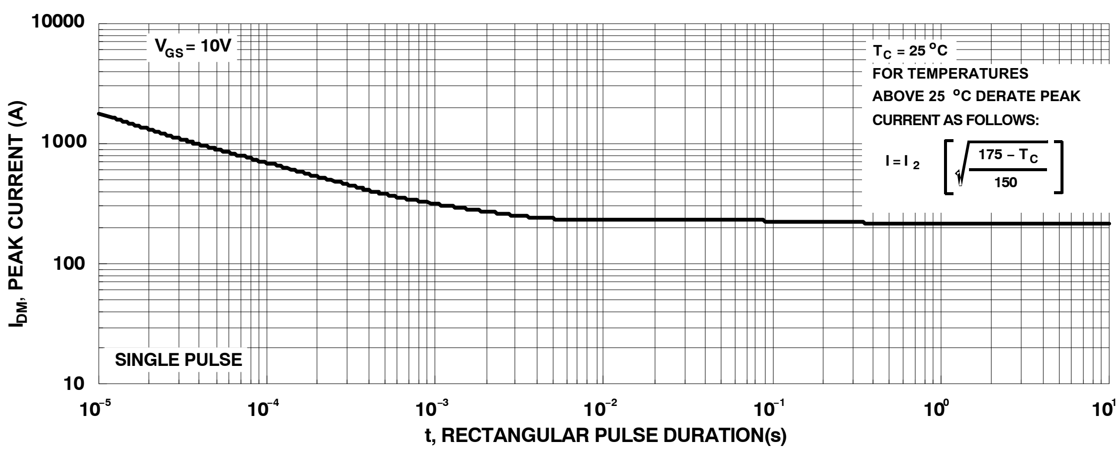


Figure 6. Peak Current Capability

TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86366_F085 (TOLL) Datasheet (High side MOSFET) (Continued)

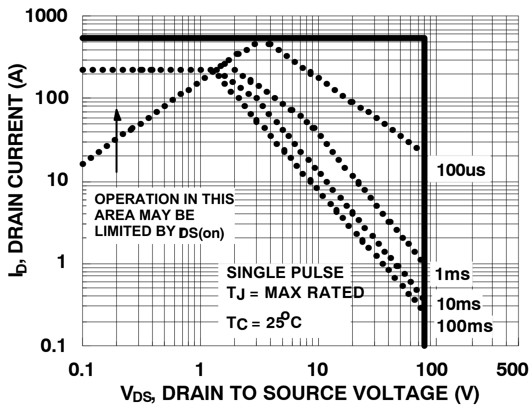


Figure 7. Forward Bias Safe Operating Area

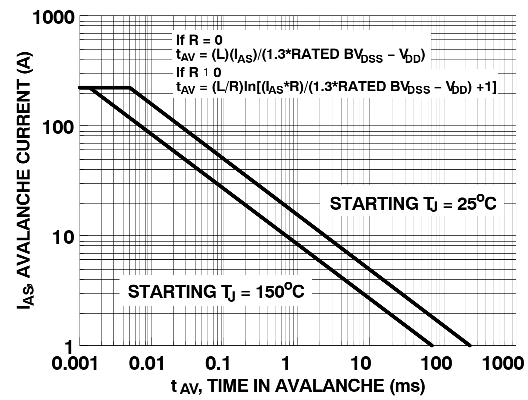


Figure 8. Unclamped Inductive Switching Capability

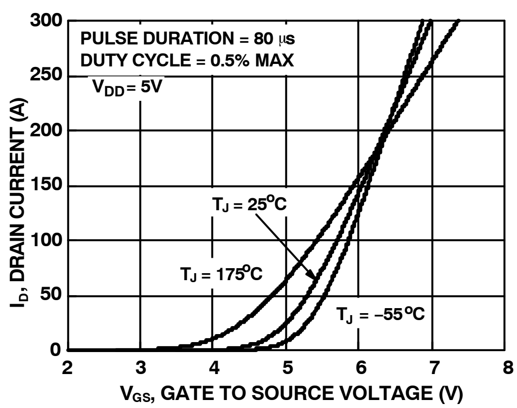


Figure 9. Transfer Characteristics

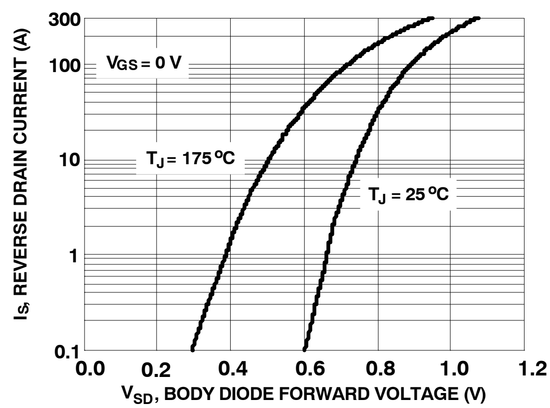


Figure 10. Forward Diode Characteristics

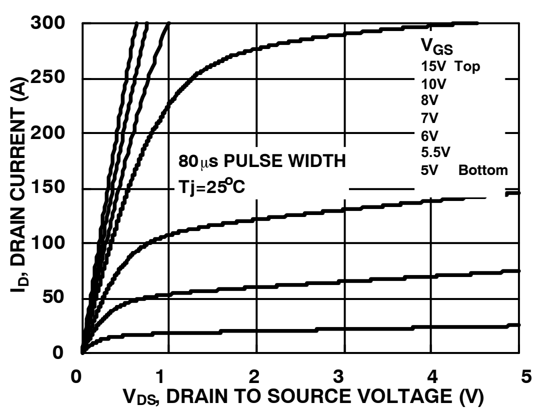


Figure 11. Saturation Characteristics

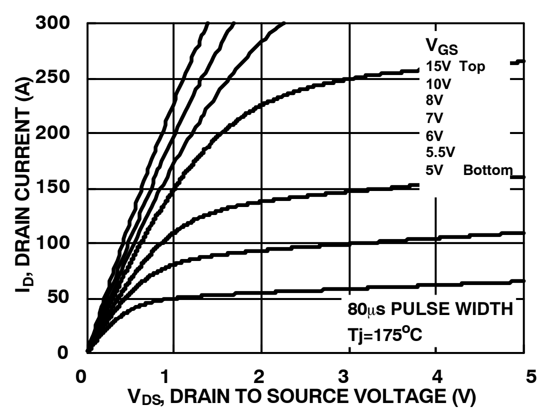


Figure 12. Saturation Characteristics

TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86366_F085 (TOLL) Datasheet (High side MOSFET)

(Continued)

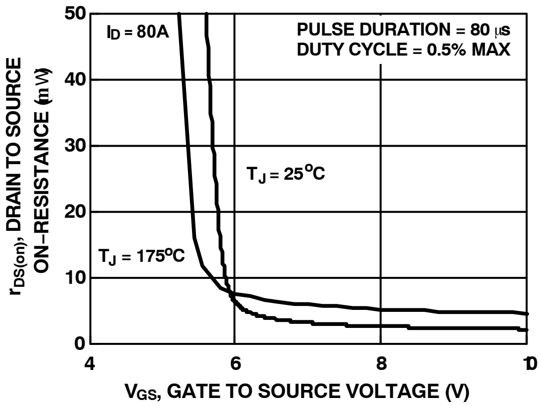


Figure 13. R_{DSON} vs. Gate Voltage

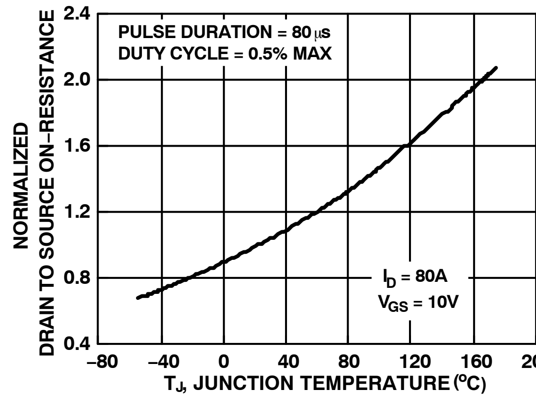


Figure 14. Normalized R_{DSON} vs. Junction Temperature

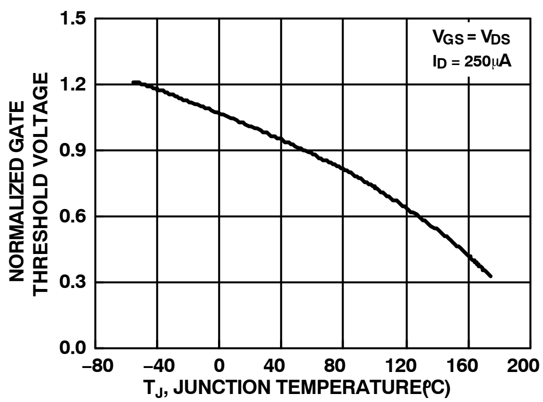


Figure 15. Normalized Gate Threshold Voltage vs. Temperature

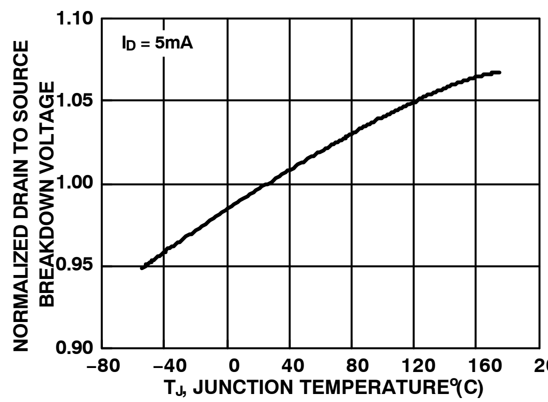


Figure 16. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

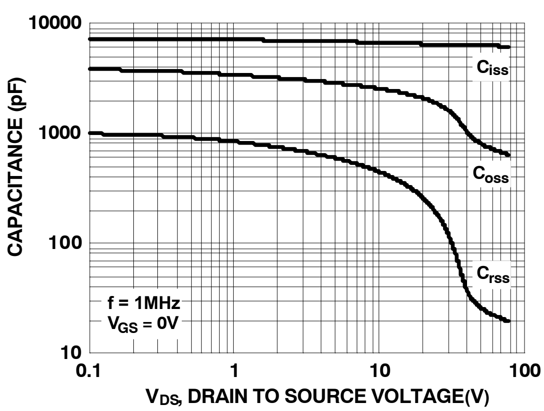


Figure 17. Capacitance vs. Drain to Source Voltage

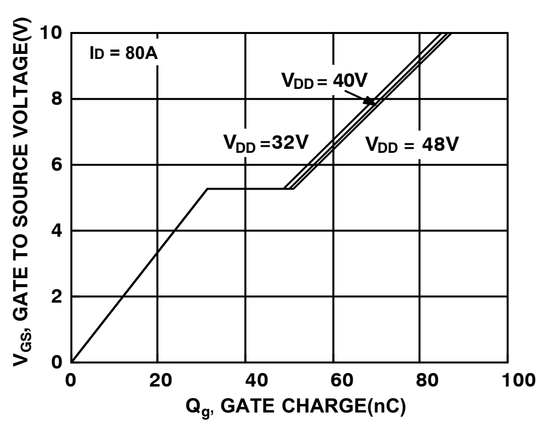


Figure 18. Gate Charge vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86363_F085 (TOLL) Datasheet (Low side MOSFET) (Continued)

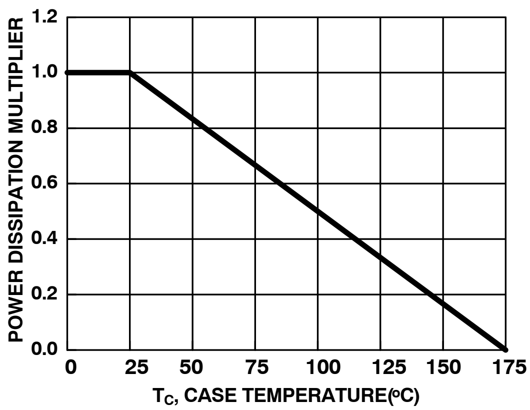


Figure 19. Normalized Power Dissipation vs. Case Temperature

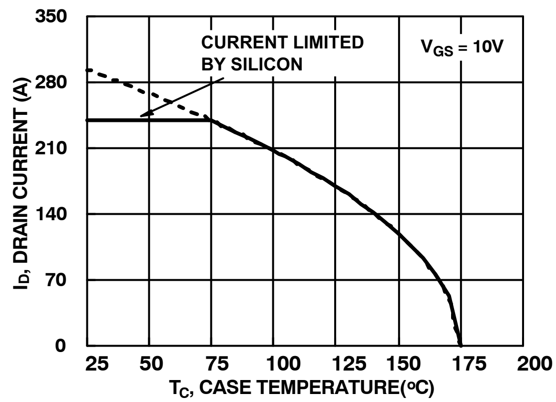


Figure 20. Maximum Continuous Drain Current vs. Case Temperature

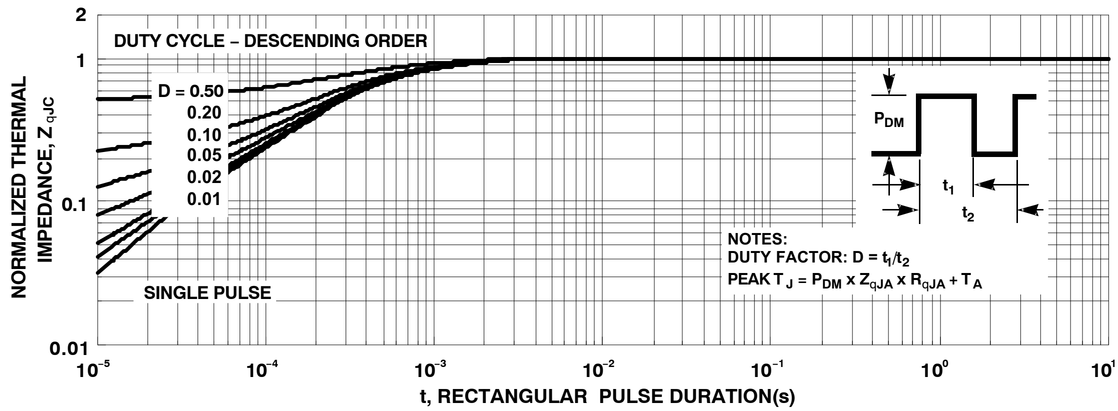


Figure 21. Normalized Maximum Transient Thermal Impedance

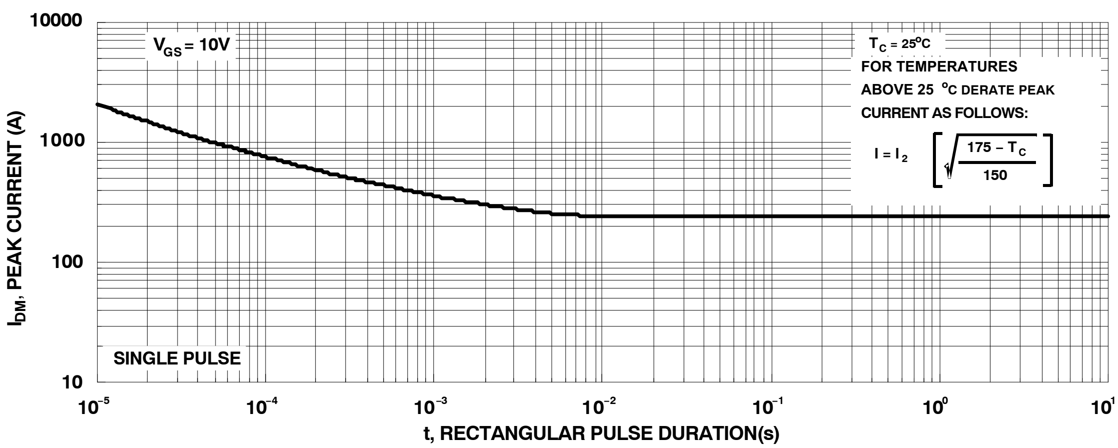


Figure 22. Peak Current Capability

TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86363_F085 (TOLL) Datasheet (Low side MOSFET) (Continued)

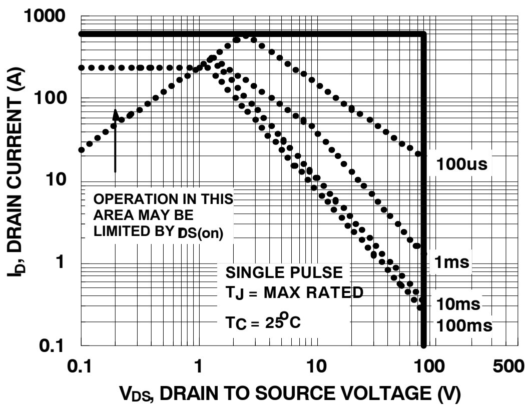


Figure 23. Forward Bias Safe Operating Area

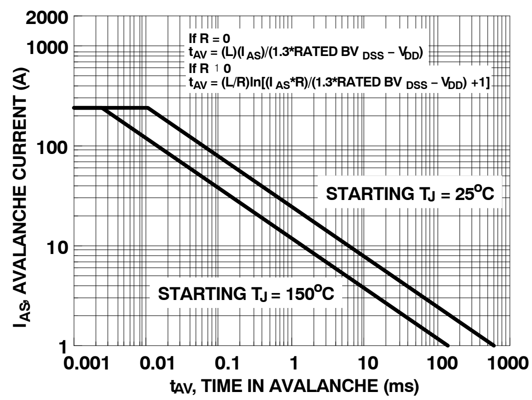


Figure 24. Unclamped Inductive Switching Capability

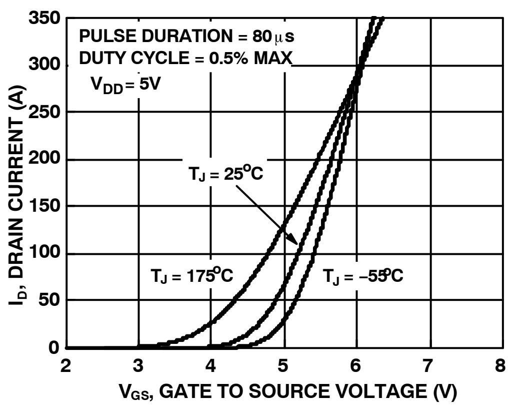


Figure 25. Transfer Characteristics

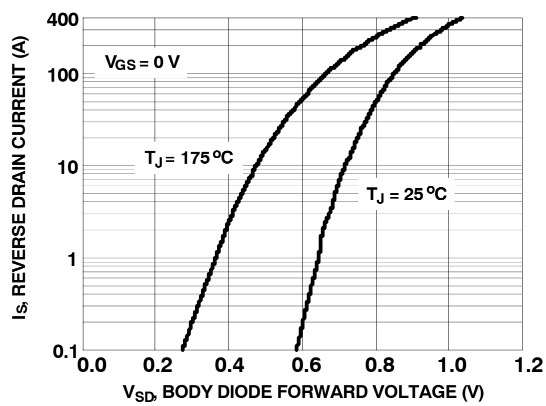


Figure 26. Forward Diode Characteristics

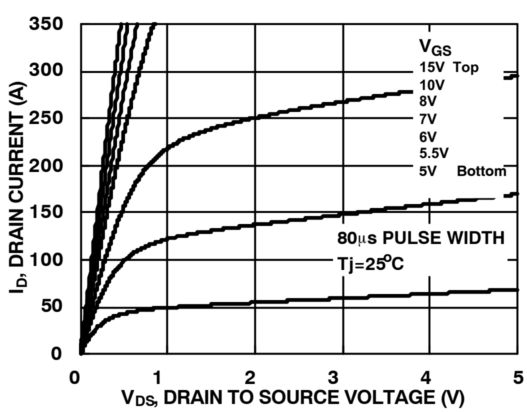


Figure 27. Saturation Characteristics

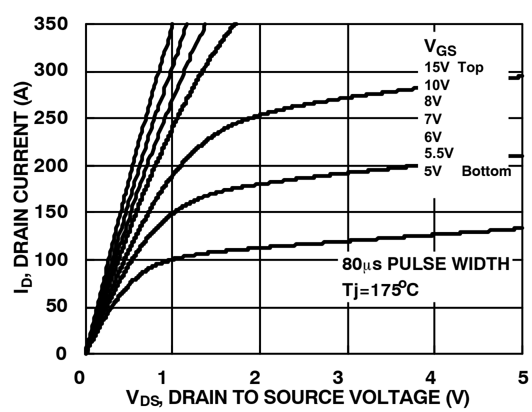


Figure 28. Saturation Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86363_F085 (TOLL) Datasheet (Low side MOSFET) (Continued)

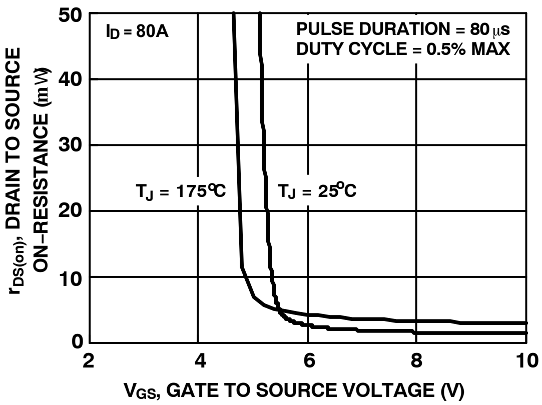


Figure 29. R_{DSON} vs. Gate Voltage

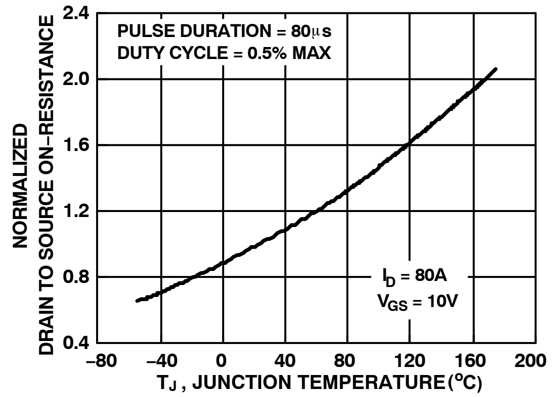


Figure 30. Normalized R_{DSON} vs. Junction Temperature

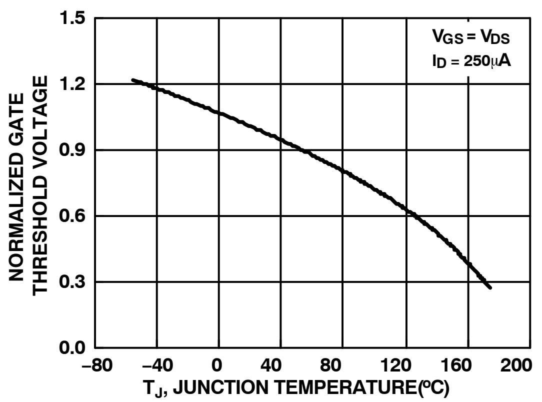


Figure 31. Normalized Gate Threshold Voltage vs. Temperature

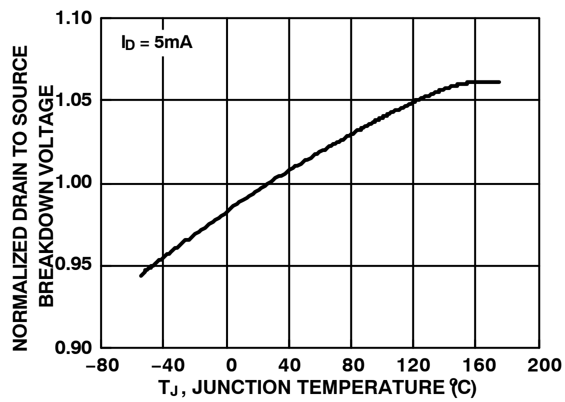


Figure 32. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

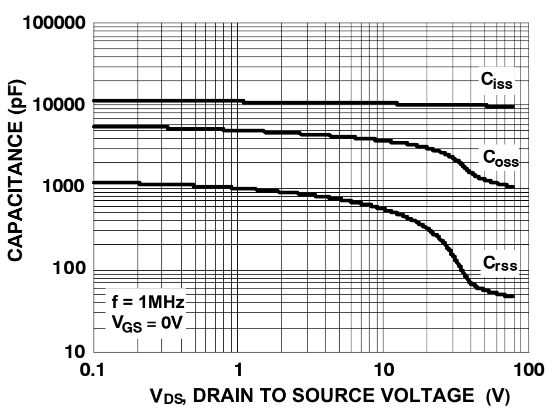


Figure 33. Capacitance vs. Drain to Source Voltage

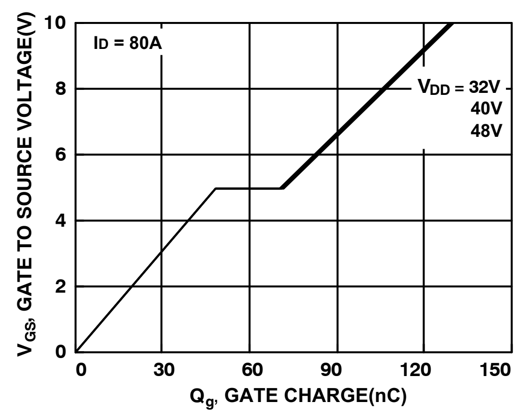
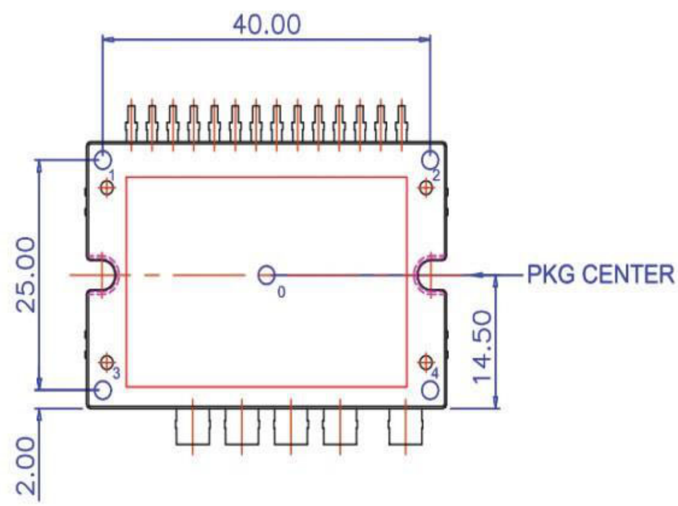


Figure 34. Gate Charge vs. Gate to Source Voltage

Table 2. MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Units
		Min.	Typ.	Max.	
Device Flatness	Note Fig. 15	0	–	+150	μm
Mounting Torque	Mounting Screw: −M3, Recommended 0.7N.m	0.4	–	0.8	N.m
Weight		–	20	–	g



FLATNESS : MAX. 150um

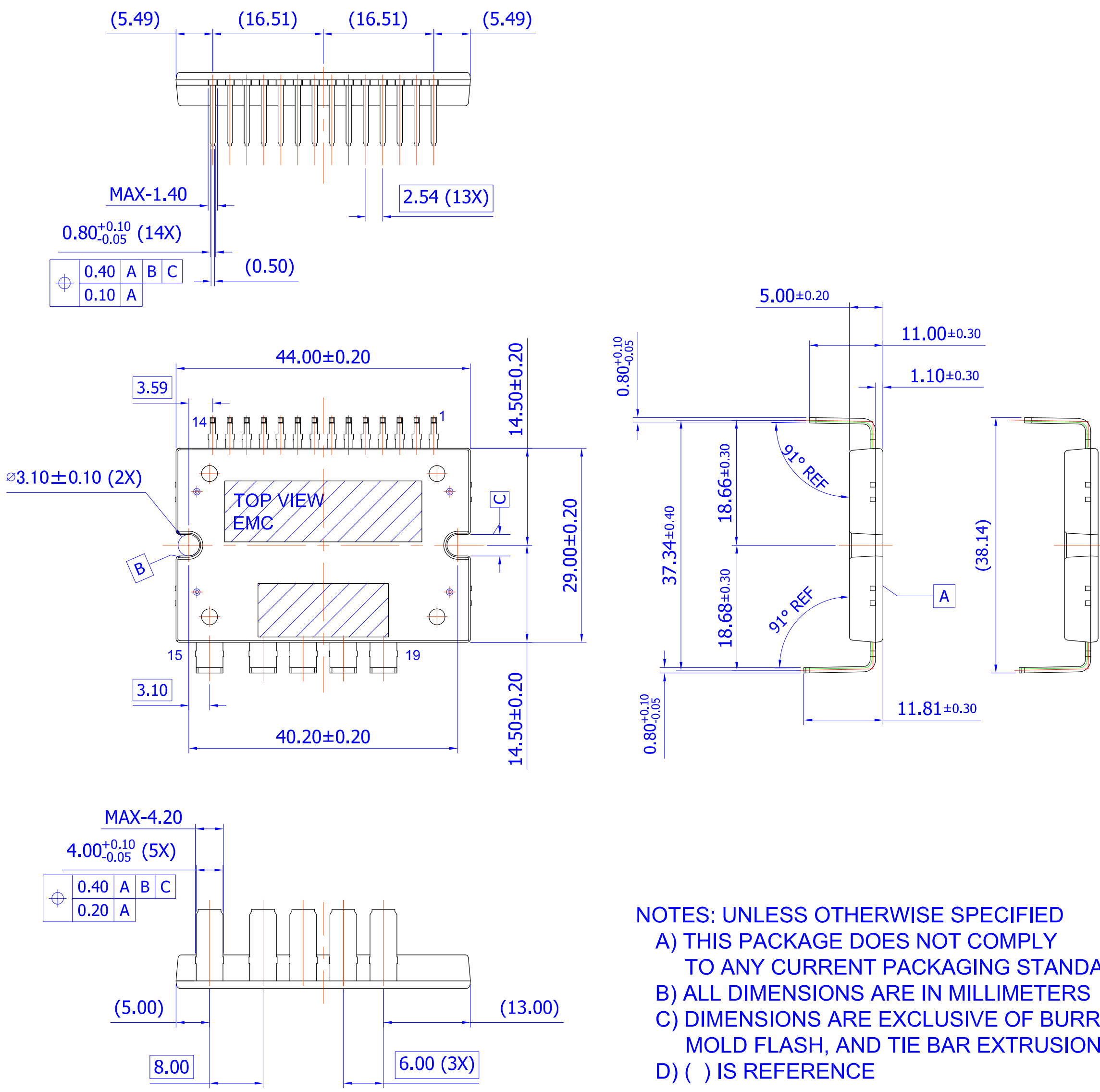
–. MEASURING AT INDICATING POINTS
1, 2, 3, AND 4 (BASED ON "0")

Table 3. PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Packing Type	Quantity
FTCO3V85A1	Tube	11

19LD, APM, PDD STD (APM19−CBC)
CASE MODCD
ISSUE O

DATE 30 NOV 2016



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

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