Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High level output voltage	V_{OH}(1)	Ports 0, 1, 32 to 35	I_{OH}=−0.4mA	2.5 to 3.6	V_{DD}−0.4			V
	V_{OH}(2)	Ports 30, 31	I_{OH}=−1.6mA	2.5 to 3.6	V_{DD}−0.4			
	V_{OH}(3)	Ports 71 to 73	I_{OH}=−0.4mA	2.5 to 3.6	V_{DD}−0.4			
	V_{OH}(4)	Ports A, B, C Ports D, E, F	I_{OH}=−0.4mA	2.5 to 3.6	V_{DD}−0.4			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 32 to 35 Ports 30, 31 (PWM function output mode)	I_{OL}=1.6mA	2.5 to 3.6			0.4	
	V_{OL}(2)	Ports 30, 31 (Port function output mode)	I_{OL}=5mA	2.5 to 3.6			0.4	
	V_{OL}(3)	Ports 7, 8 XT2	I_{OL}=1.6mA	2.5 to 3.6			0.4	
	V_{OL}(4)	Ports A, B, C Ports D, E, F	I_{OL}=1.6mA	2.5 to 3.6			0.4	
LCD output voltage regulation	VODLS	S0 to S53	• I_O=0mA • VLCD, 2/3VLCD, 1/3VLCD level output • See Fig. 8.	2.5 to 3.6	0		±0.2	
	VODLC	COM0 to COM3	• IO=0mA • VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD level output • See Fig. 8.	2.5 to 3.6	0		±0.2	
LCD bias resistor	RLCD(1)	Resistance per one bias resister	See Fig. 8.	2.5 to 3.6		60		kΩ
	RLCD(2)	Resistance per one bias resister 1/2R mode	See Fig. 8.	2.5 to 3.6		30		
Resistance of pull-up MOS Tr.	Rpu(1)	Ports 0, 1, 3, 7 Ports A, B, C, D, E, F	V_{OH}=0.9V_{DD}	2.5 to 3.6	18	50	50	
Hysterisis voltage	VHYS(1)	Ports 1, 7 RES		2.5 to 3.6		0.1V_{DD}		V
	VHYS(2)	P87 small signal input side		2.5 to 3.6		0.1V_{DD}		
Pin capacitance	CP	All pins	• For pins other than that under test: V_{IN}=V_{SS} • f=1MHz • Ta=25°C	2.5 to 3.6		10		pF
Input sensitivity	Vsen	P87 small signal input side		2.5 to 3.6	0.12V_{DD}			Vpp

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Serial I/O Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3$ = 0V, 0.190µs ≤ tCYC ≤ 200µs

SIO0 Serial I/O Characteristics (Note 4-1-1) at V_{DD} = 2.7 V to 3.6V 0.190µs ≤ tCYC ≤ 200µs

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 3.6	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-3)	2.5 to 3.6			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.5 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.		2			
		Low level pulse width	tSCKL(4)			2.5 to 3.6	1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03			µs
	Data hold time		thDI(2)			2.5 to 3.6	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.5 to 3.6			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P30 to P33), INT5(P34 to P35), INT6(P30), INT7(P34)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	256			
	tPIH(5) tPIL(5)	MICIN(P87)	Condition that signal is accepted to small signal detection counter.	2.5 to 3.6	1			
	tPIH(6) tPIL(6)	RMIN(P73)	Condition that signal is accepted to remote control receiver circuit.	2.5 to 3.6	4			RMCK (Note 5-1)
	tPIL(7)	$\overline{RES}$	Resetting is enabled.	2.5 to 3.6	200			µs

Note 5-1: RMCK is an unit for the base clock (40tCYC/50tCYC/Sub-Clock) of remote control receiver circuit.

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12bits AD Converter Mode at Ta =–30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		12		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±16	LSB
Conversion time	tCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	64		115	µs
				2.7 to 3.6	128		230	
				2.5 to 3.6	256		460	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.5 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.5 to 3.6	–1			

<8bits AD Converter Mode at Ta =–30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		8		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±1.5	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	39		71	µs
				2.7 to 3.6	79		140	
				2.5 to 3.6	157		280	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.5 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.5 to 3.6	–1			

<Conversion time calculation formulas>

12bits AD Converter Mode: tCAD (Conversion time)=((52/(division ratio)) + 2) × (1/3) ×tCYC
8bits AD Converter Mode: tCAD(Conversion time)=((32/(division ratio)) + 2) × (1/3) ×tCYC

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.
The conversion time is 2 times the normal-time conversion time when:
- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• FmCF=18MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		6.1	15.6	mA
	IDDOP(2)		• FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.5 to 3.6		3.9	8.8	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		0.4	1.7	
	IDDOP(4)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		4.3	12.0	
	IDDOP(5)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		2.1	6.6	
	IDDOP(6)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		19.3	73	μA

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=18MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		2.7	6.8	mA
	IDDHALT(2)		• HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.5 to 3.6		1.4	3.1	
	IDDHALT(3)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		0.2	0.75	
	IDDHALT(4)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		1.6	4.5	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		0.7	1.75	
	IDDHALT(6)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		12.4	54.9	μA
HOLD mode consumption current	IDDHOLD(1)	V_{DD}	• HOLD mode • CF1=V_{DD} or open (External clock mode)	2.5 to 3.6		0.08	18.4	
Timer HOLD mode consumption current	IDDHOLD(2)		• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FmX'tal=32.768kHz crystal oscillation mode	2.5 to 3.6		10.14	34.4	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Write Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

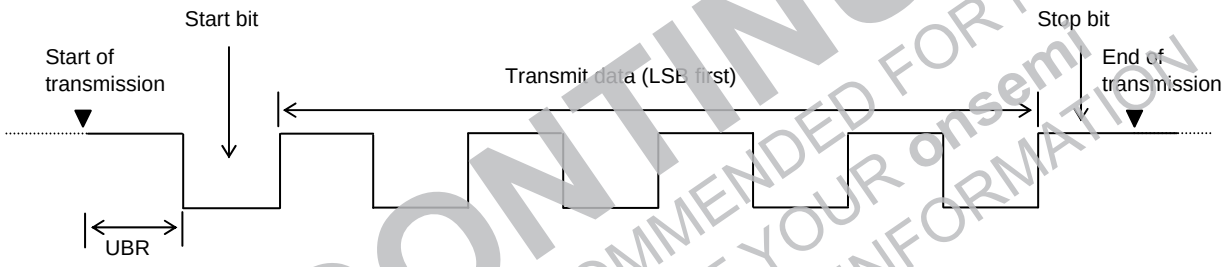
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Without CPU current	3.0 to 3.6		7	11	mA
Programming time	tFW(1)		• 2K-byte erase operation	3.0 to 3.6		12	15	ms
	tFW(2)		• 2K-byte writing operation	3.0 to 3.6		35	45	µs

UART (Full Duplex) Operating Conditions at Ta = +40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

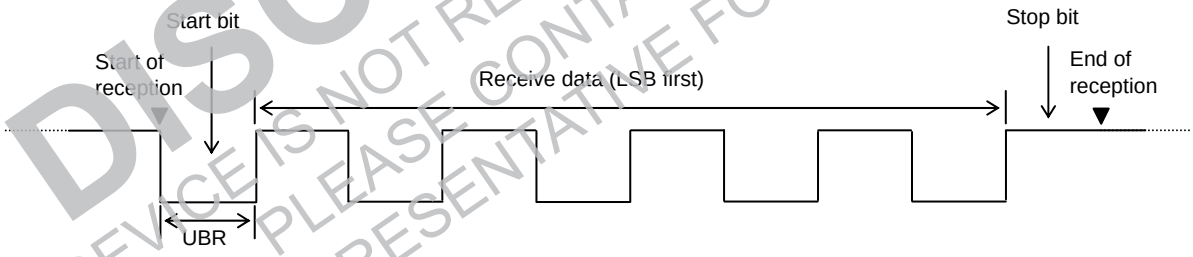
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR	UTX(S32), URX(S33)		2.5 to 3.6	16/3		8192/3	tCYC

Data length : 7/8/9 bits (LSB first)
Stop bits : 1 bit (2-bit in continuous data transmission)
Parity bits : None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
18MHz	MURATA	CSTCE18M0V51-R0	(5)	(5)	OPEN	150	2.7 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS18M0X51-B0	(5)	(5)	OPEN	0	2.7 to 3.6	0.11	0.33	
10MHz	MURATA	CSTCE10M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS10M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS8M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillation Circuit with a Crystal Oscillation

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	9	9	Open	330k	2.5 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Fig. 4).

Caution: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

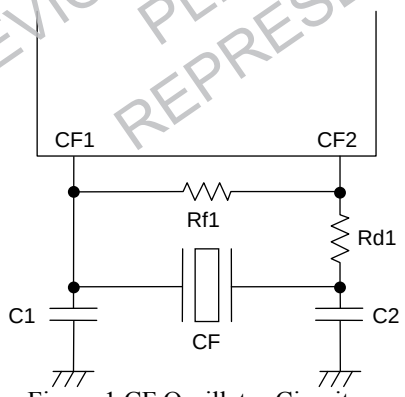


Figure 1 CF Oscillator Circuit

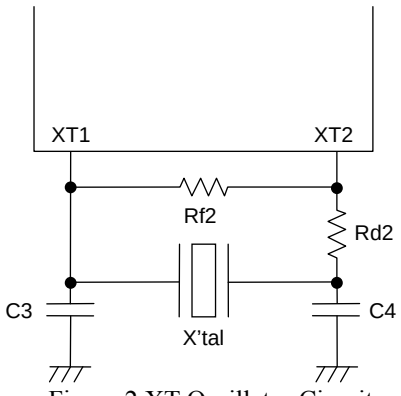


Figure 2 XT Oscillator Circuit

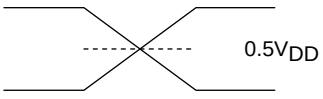
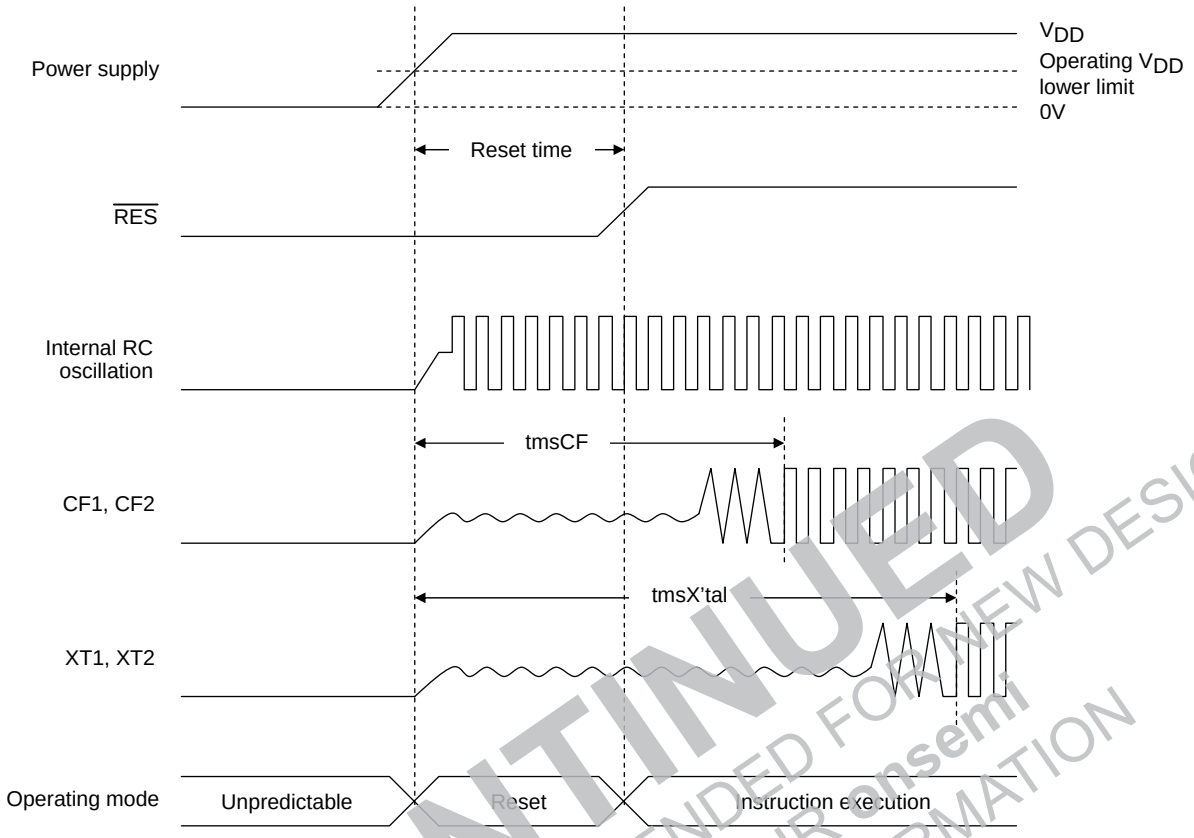
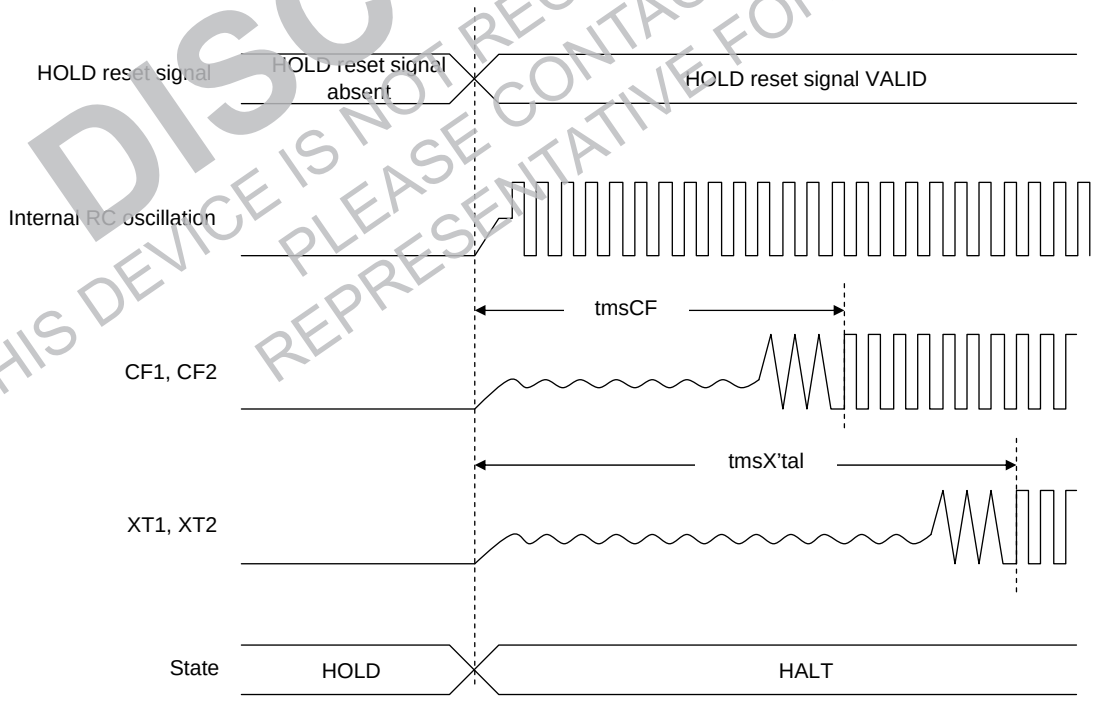


Figure 3 AC Timing Measurement Point

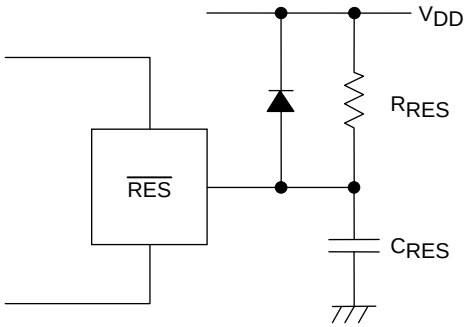


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note :
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200μs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

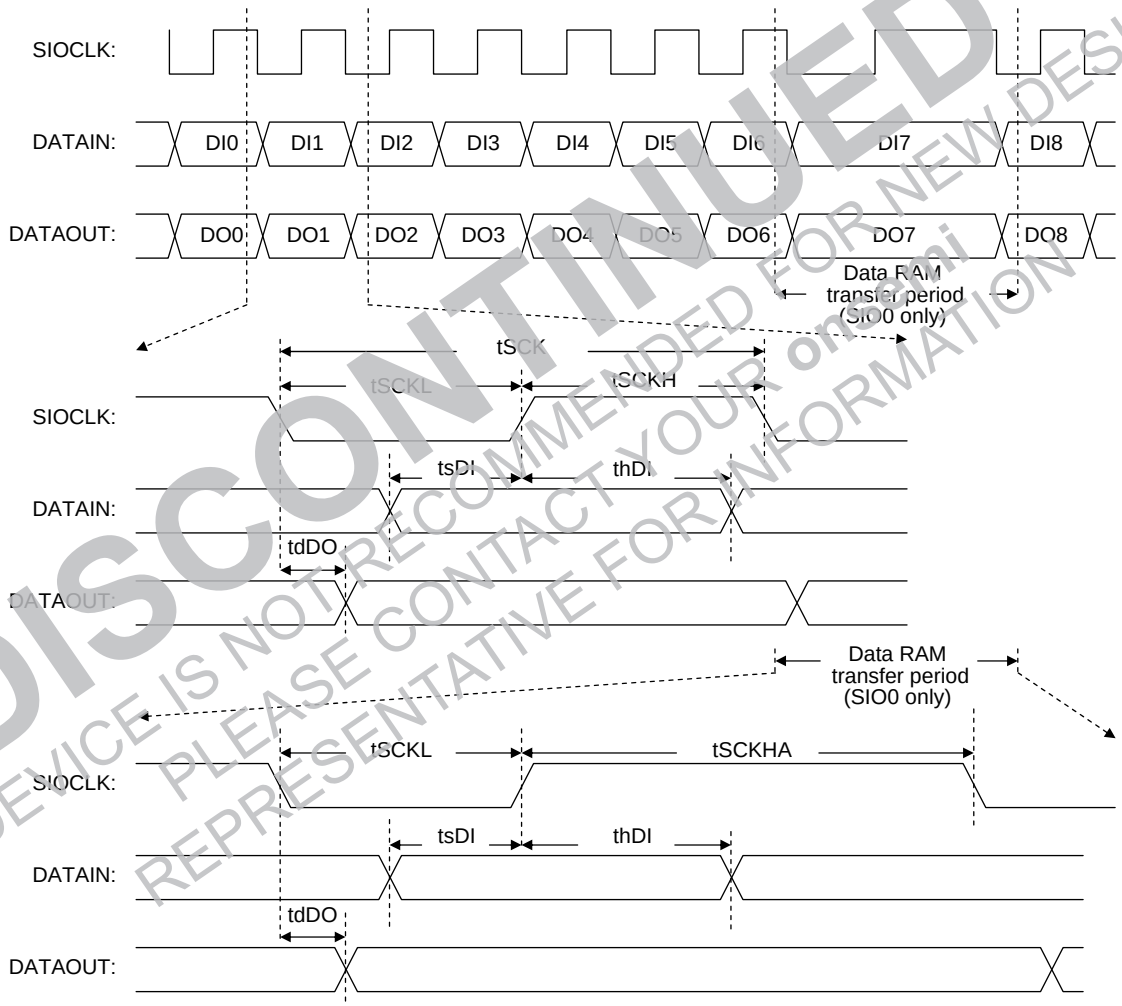


Figure 6 Serial I/O Waveforms

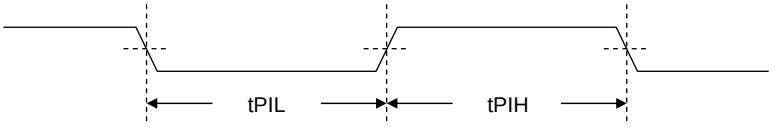


Figure 7 Pulse Input Timing Signal Waveform

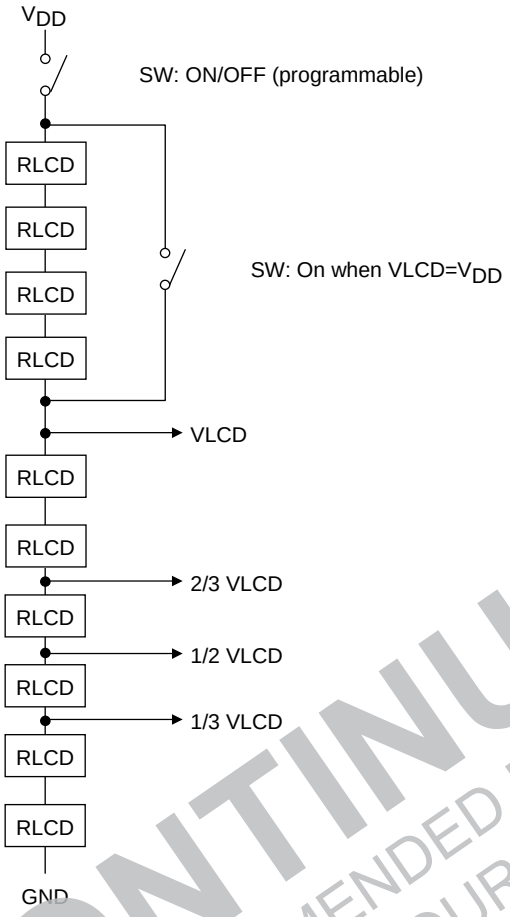


Figure 8 LCD bias resistor

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F7NC8AUEJ-2H	QIP100E(14×20) (Pb-Free / Halogen Free)	50 / Tray Foam
LC87F7NC8AVUEJ-2H	QIP100E(14×20) (Pb-Free / Halogen Free)	50 / Tray Foam