16-bit Microcontroller 384K-byte Flash ROM / 24Kbyte RAM / 100-pin



ON Semiconductor

www.onsemi.com

Features

- 16-channel 12-bit resolution AD converter
- Infrared remote controller receiver circuit
- CRC operating circuit
- Internal Reset Function

Performance

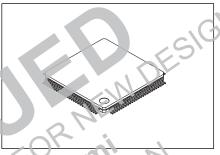
- 83.3ns (12.0MHz), $V_{DD} = 3.0$ to 3.6V, $T_a = -40$ to +85°C
- 100ns (10.0MHz), $V_{DD} = 2.7$ to 3.6V, $T_a = -40$ to +85°C

Function Descriptions

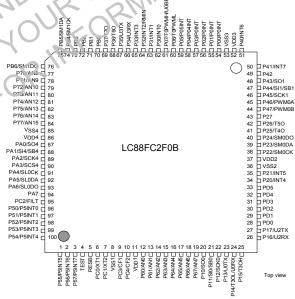
- Xstromy16 CPU
 - 4G-byte address space
 - General-purpose registers : 16 bits × 16 registers
- Ports
 - I/O Ports 86
 - Power supply pins 8 (VSS1 to VSS4, VDD1 to VDD4)
- Timer
 - 16-bit timers \times 8
 - Base timer serving as a time-of-day clock
- Serial interfaces
- Synchronous SIO interfaces × 3 (with automatic transmission capability)
 - Single master I²C/synchronous SiO interface × 2
 Slave I²C/synchronous SIO interface
 - Asynchronous SIO (UART) interfaces × 3
- Multifrequency 12-ut PWM modules
- 16-channel 12-bit resolution AD converted
- Watchdog timer
- Infra ed remote controller receiver circuit
- CRC operating circuit
- Real time clock
- System clock frequency divider
- CF oscillator circuit, Crystal oscillator circuit, RC oscillator circuit
- 61-source 14-vector interrupt feature
- On-chip debugger function

Application

• Home audio, White goods



TQFP 100.14x14



Pin Assignment (Top view)

ORDERING INFORMATION

See detailed ordering and shipping information on page 47 of this data sheet.

^{*} This product is licensed from Silicon Storage Technology, Inc. (USA).

Function Details

- Xstromy16 CPU
 - 4G-byte address space
 - General-purpose registers: 16 bits × 16 registers

■ Flash ROM

- Programming voltage level: 2.7 to 3.6V.
- Block-erasable in 2K byte units.
- Data written in 2-byte units.
- 393216×8 bits

■ RAM

- 24576×8 bits
- Minimum instruction cycle time (tCYC)
 - 83.3 ns (12 MHz), $V_{DD} = 3.0 \text{ to } 3.6 \text{V}$
 - 100 ns (10 MHz), $V_{DD} = 2.7 \text{ to } 3.6 \text{V}$

■ Ports

• Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1 bit units : 86 (P0n P n, P2n, P3n, P4n, P5n, P6n, P7n,

PAn PB0 to PB6, PC2, PD0 to PD5)

DESIGN

• Oscillation/normal withstand voltage I/O ports

• Reset pins

• TEST pins

• Power pins

. 4 (PC0, PC1, PC3, PC4) : 1 (RESB)

1 (TEST)

: 8 (V_S31 to 4, V_{DD} 1 to 4)

■ Timers

- Timer 0: 16-bit timer that supports PWM/toggle outputs
 - <1> 5-bit prescaler
 - <2> 8-bit PWM \times 2, 8-bit timer + 8-bit PWM mode selectable
 - <3> Clock source selectable from system clock, OSCO OSC1, and internal RC oscillator.
- Timer 1: 16-bit timer with capture registers
 - 1>5-bit prescaler
 - <2> May be divided into 2 channels of 8-bit timer
 - 3> Clock source relectable from system clock, OSC0, OSC1, and internal RC oscillator
 - Timer 2: 16-bit timer with capture registers
 - <1> 4-bit prescaler
 - <2> May be divided into 2 channels of 8-bit timer
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3: 16-bit timer that shpports PWM/toggle outputs
 - <1> 8-bit prescaler
 - <2> 8-bit timer× 2ch or 8-bit timer+8-bit PWM mode selectable
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle outputs
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle output
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 6: 16-bit timer that supports toggle outputs
 - <1> Clock source selectable from system clock and prescaler 1
- Timer 7: 16-bit timer that supports toggle output
 - <1> Clock source selectable from system clock and prescaler 1
 - *Prescaler 0 and 1 are consisted of 4bits and can choose their clock source from OSC0 or OSC1.
- · Base timer
 - <1> Clock may be selected from OSC0 (32.768 kHz crystal oscillator) and frequency-divided output of system clock.
 - <2> Interrupts can be generated in 7 timing schemes.

■ Real time clock

- <1> Calender with Jan. 1, 2000 to Dec. 31, 2799 including automatic leapyear calculation function.
- <2> Consisted of Indipendent second-minuit-hour-day-month-yeare-century counters.

■ Serial interfaces

- SIO0: 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
- SIO1: 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - NDESIGN <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
- SIO4: 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9 to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
- SMIIC0: Single master I²C/8-bit synchronous SIO

Mode 0: Single-master mode communication

Mode 1: Synchronous 8-bit serial I/O (MSB first)

• SMIIC1: Single master I²C/8-bit synchronous SIO

Mode 0: Single-master mode communication

Mode 1: Sync ronous 8-bit serial I/O (MSB first)

• SLIICO: Slave 1²C/8-bit synchronous SIO

Mode 0: I²C slave mode communication

Mode 1. Synchronous 8-bit serial I/O (MSB first)

Note: usable only with the external clock source

• UARTO

- 1> Data length : 8 bits (LSB first)
- <2> Start bits : 1 bit <3> Stop bits . 1 bit
- <4> Parity bits · None/even parity/odd parity
- <5> Transfer rate · 4/8 cycle
- <6> Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer4 cycle.
- <7> Full duplex communication

Note: The "cycle" refers to one period of the baudrate clock source.

• UART2

: 8 bits (LSB first) <1> Data length

<2> Start bits : 1 bit <3> Stop bits : 1/2 bit

: None/even parity/odd parity <4> Parity bits

<5> Transfer rate : 8 to 4096 cycle

<6> Baudrate source clock : System clock/OSC0/OSC1/P26 input signal

<7> Wakeup function

<8> Full duplex communication

Note: The "cycle" refers to one period of the baudrate clock source.

• UART3

<1> Data length : 8 bits (LSB first)

<2> Start bits : 1 bit <3> Stop bits : 1/2 bit

<4> Parity bits : None/even parity/odd parity

<5> Transfer rate : 8 to 4096 cycle

<6> Baudrate source clock : System clock/OSC0/OSC1/P36 input signal

<7> Wakeup function

<8> Full duplex communication

Note: The "cycle" refers to one period of the baudrate clock source.

■ AD converter

- <1> 12/8 bits resolution selectable
- <2> Analog input: 16 channels
- <3> Comparator mode

■ PWM

- PWM0: Multifrequency 12-bit PWM × 2 channels (PWM0A and PWM0B)
 - <1> 2-channel pairs controlled independently of one another
 - <2> Clock source selectable from system clock or OSC1
 - <3> 8-bit prescaler: TPWMR0= (prescaler value + 1) × clock period
 - <4> 8-bit fundamental wave PWM generator circuit + 4-bit addit onal rulse generator circuit

DESIGN

<5> Fundamental wave PWM mode

Fundamental wave period: 16 TPWMR0 to 256 TPWMR0

High pulse width : 0 to (Fundamental wave period - TPW MR0)

<6> Fundamental wave + additional pulse mode

Fundamental wave period: 16 TPWMR0 to 256 TPWMR0 Overall period: Fundamental wave period × 16

High pulse width 0 to (Fundamental wave period - TPWMR0)

■ CRC operating circuit

- Watchdog timer
 - 1> Driven by the base timer + internal vatchdog timer dedicated counter
 - Interrupt or reset mode selectable
- Infrared Remote Controller Receiver Circuit
 - 1) Noise reject on turction (noise tilter time constant: Approx. 120μs when the 32.768kHz crystal oscillator is selected as the reference clock source)
 - 2) Supports data encording systems such as PPM (Pulse Position Modulation) and Manchester encording
 - 3) X tal HOLD mode release function

■ Internal Reset Function

- •Power-on reset (POR) function
 - 1) POR reset is generated only at power-on time.
 - 2) The POR release level can be selected through option configuration.
- •Low-voltage detection reset (LVD) function
 - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
 - 2) The use/disuse of the LVD function and the low voltage threshold level can be selected by option configuration.
- Interrupts (peripheral function))
 - 61 sources (33 modules). 14 vector addresses
 - <1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - <2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Interrupt Module |
|-----|----------------|---|
| 1 | 08000Н | Watchdog timer (1) |
| 2 | 08004H | Base timer (2) |
| 3 | 08008H | Timer 0 (2) |
| 4 | 0800CH | INT0 (1) |
| 5 | 08014H | INT1 (1) |
| 6 | 08018H | INT2 (1)/timer 1 (2)/UART2 (4) |
| 7 | 0801CH | INT3 (1)/timer 2 (4)/SMIIC0 (1)/SLIIC1 (1) |
| 8 | 08020Н | INT4 (1)/timer 3 (2)/Infared remote control receiver(4) |
| 9 | 08024Н | INT5 (1)/timer 4 (1)/SIO1 (2) |
| 10 | 0802CH | PWM0 (1)/SMIIC1(1) |
| 11 | 08030Н | ADC (1)/timer 5 (1)/SIO4(2) |
| 12 | 08034Н | INT6 (1)/timer 6 (1)/UART 3 (4) |
| 13 | 08038H | INT7 (1)/SIO0 (2)/SIO0(2) |
| 14 | 0803CH | Port 0 (3)/Port 5 (8)/RTC (1)/CRC (1) |

- 3 priority levels selectable
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

■ Subroutine stack: RAM area

- Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
- Subroutine calls that do not automatically save PSW 4 bytes
- Multiplication/division instructions
 - 16 bits × 16 bits (4 tCYC execution time)
 - 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
 - 32 bits ÷ 16 bits (18 to 19 tCYC execution time)
- Oscillator circuits
 - RC oscillator circuit (internal)
- For system clock
- CF oscillator circuit (built-in Rf circuit)
- : For system clock(OSC1)
- Crystal oscillator circuit (built in Rf circuit)
- For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal)
- : For system clock (In the case of exception processing)
- VC oscillator circuit
- : For timer3, 4, 5, 6, 7 clock
- System clock divider function
 - Can run on low current.
 - 1/1 to 1/128 of the system clock frequency can be set.
- Standby function
 - HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - <1> Oscillation is not stopped automatically.
 - <2> Released by a system reset or occurrence of an interrupt.
 - HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - <1>OSC1, RC, and OSC0 oscillations automatically stop.
 - <2> There are six ways of releasing the HOLD mode:
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established at port 5
 - (5) Having an interrupt established at SIO0, SIO1 or SIO4
 - (6) Having an interrupt established at UART2 or UART3

- HOLDX mode: Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
 - <1>OSC1 and RC oscillations automatically stop.
 - <2> OSC0 maintains the state that is established when the HOLDX mode is entered.
 - <3> There are nine ways of releasing the HOLDX mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established at port 5
 - (5) Having an interrupt source established at the base timer circuit
 - (6) Having an interrupt established at SIO0, SIO1 or SIO4
 - (7) Having an interrupt established at UART2 or UATR3
 - (8) Having an interrupt established at Infared remote control receiver.
 - (9) Having an interrupt source established at the real time clock circuit

■ On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
 Supports source line debugging and tracing functions, and breakpoint setting and real time display
 Single-wire communication

 Package form
- Package form
 - TQFP100, 14 × 14 : Pb-Free and Halogen Free type
- Development tools
 - On-chip debugger: EOCUIF1 or EOCUIF2 + LC88 FC2F0B

■ Programming board

| Package | Programming Board |
|-----------------|-------------------|
| TQFP100,14 × 14 | W88F52TQ |

■ Flash ROM Programmer

| Make | er | Model | Supported Version | Device |
|---------------|------------|---------------------------|----------------------|-----------|
| Flash Support | On-board | AF9101/AF9103 (Main budy) | (Note 2) | LC88FC2H0 |
| Group | Single / | (FSG models) | | |
| Company | Gang | SIB88 Type A | | |
| (FSG) | programmer | (Interface driver) | | |
| + | 0/ | (ON Semiconductor model) | | |
| ON | 125 | | | |
| Semiconductor | 101 | | | |
| (Note 1) | | | | |
| ON | Single / | SKK Type C | Application Version | LC88FC2H0 |
| Semiconductor | Gang | (SanyoFWS) | After 1.08 | |
| | programmer | | Chip Data Version | |
| | | | After 2.46 | |
| | On-board | FWS-X16DI Type 2 | Application Version | LC88FC2H0 |
| | Single | | After 1.08 | |
| | programmer | | Chip Data Version | |
| | | | After 2.45 | |

For information about AF-Series:

Flash Support Group Company. (TOA ELECTRONICS, Inc.)

TEL: +81-53-459-1050 E-mail: sales@j-fsg.co.jp

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from our company (SIB88-TypeA) together can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

Package Dimensions

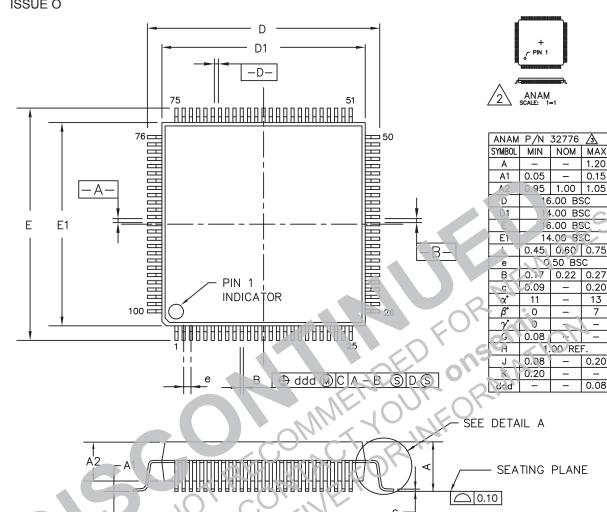
unit: mm

G RADIUS-

DETAIL

Α

TQFP 100, 14x14 CASE 932AN-01 ISSUE O



2. PACKAGE OUTSIDE FEATURES AND PIN 1 INDICATOR VARY FROM VENDOR TO VENDOR.

THIS PART CONFORMS TO JEDEC 95, MS-026, VARIATION "AED".

MAX 1.20

0.15

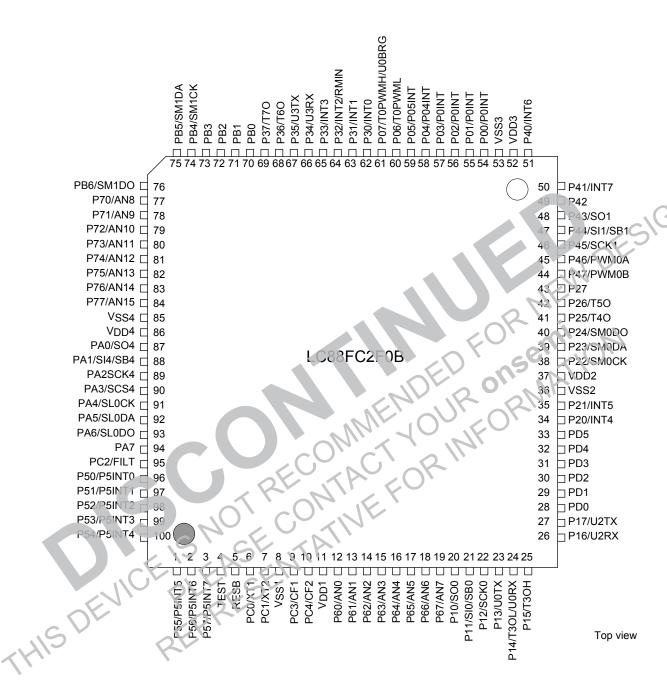
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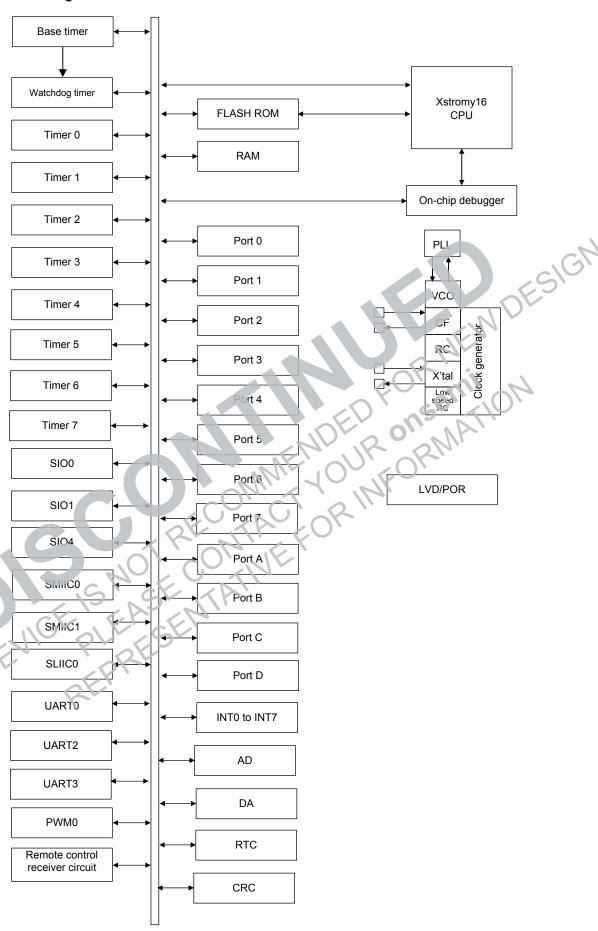
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Pin Assignment



TQFP100,14x14 (Pb-Free and Halogen Free type)

System Block Diagram



Pin Description

| Pin Name | I/O | Description |
|-------------|-----|---|
| VSS1, VSS2, | - | – power sources |
| VSS3, VSS4 | | |
| VDD1, VDD2, | _ | +power sources |
| VDD3, VDD4 | | |
| Port 0 | I/O | • 8-bit I/O port |
| P00 to P07 | | • I/O specifiable in 1-bit units |
| 100 to 107 | | • Pull-up resistors can be turned on and off in 1 bit units |
| | | • HOLD release input (P00 to P03, P04, P05) |
| | | • Port 0 interrupt input (P00 to P03, P04, P05) |
| | | • Pin functions |
| | | P06: Timer 0L output |
| | | P07: Timer 0L output/UART0 clock input |
| Port 1 | I/O | • 8-bit I/O port |
| P10 to P17 | | • I/O specifiable in 1-bit units |
| 110 10117 | | • Pull-up resistors can be turned on and off in 1 bit units |
| | | • Pin functions |
| | | P10: SIO0 data output |
| | | P11: SIO0 data input/pulse input/output |
| | | P12: SIO0 clock input/output |
| | | P13: UART0 transmit |
| | | P14: Timer 3L output/UART0 receive |
| | | P15: Timer 3H output |
| | | P16: UART2 receive |
| | | P17: UART2 transmit |
| Port 2 | I/O | • 8-bit I/O port |
| P20 to P27 | | • I/O specifiable in 1-bit units |
| F20 t0 F27 | | • Pull-up resistors can be turned on and of in 1 bit units |
| | | • Pin functions |
| | | P20: IN [4 input/HOLD release input/timer 3 event input/ |
| | | timer 2L capture input/timer 2H capture input |
| | | P21: INT5 input/HOLD release input/timer 3 event input/ |
| | | timer 2L capture input/timer 2H capture input |
| | | P22. SMIICo clock input/output |
| | | P23: SMIIC) bus input/output/data input |
| | | P24: SMIICO data output (used in 3-wire SIO mode) |
| | | P25: Timer 4 output |
| | | P26: Timer 5 output |
| | CV | Interrupt acknowledge type |
| | | INT4, INT5: H level, L level, H edge, L edge, both edges |

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Continued from preceding page.

| Pin Name | I/O | Description |
|------------|-----|--|
| Port 3 | I/O | • 8-bit I/O port |
| P30 to P37 | 1 | • I/O specifiable in 1-bit units |
| 130 10 137 | | • Pull-up resistors can be turned on and off in 1 bit units |
| | | • Pin functions |
| | | P30: INT0 input/HOLD release/timer 2L capture input |
| | | P31: INT1 input/HOLD release/timer 2H capture input |
| | | P32: INT2 input/HOLD release/timer 2 event input/timer 2L capture input/ |
| | | Infrared Remote Controller Receiver input P33: INT3 input/HOLD release/timer 2 event input/timer 2H capture input |
| | | P34: UART3 receive |
| | | P35: UART3 transmit |
| | | P36: Timer 6 output |
| | | P37: Timer 7 output |
| | | Interrupt acknowledge type |
| | | INT0 to INT3: H level, L level, H edge, L edge, both edges |
| Port 4 | I/O | • 8-bit I/O port |
| P40 to P47 | | • I/O specifiable in 1-bit units |
| | | Pull-up resistors can be turned on and off in 1 bit units |
| | | • Pin functions |
| | | P40: INT6 input/HOLD release input |
| | | Pin functions P40: INT6 input/HOLD release input P41: INT7 input/HOLD release input P43: SIO1 data output P44: SIO1 data input/but input/output |
| | | P43: SIO1 data output P44: SIO1 data input/bus input/output |
| | | P45: SIO1 clock input/output |
| | | P46: PWM0A output |
| | | P47: PWM0Boutput |
| | | Interrupt acknowledge type |
| | | P41: INT7 input/HOLD release input P43: SIO1 data output P44: SIO1 data input/bus input/output P45: SIO1 clock input/output P46: PWM0A output P47: PWM0Boutput Interrupt acknowledge type INT6, INT7: H level. L level. H edge. L edge, both edges |
| Port 5 | I/O | • 8-bit I/O port |
| P50 to P57 | | • I/O specifiable in 1-bit units |
| | | • Pull-up resistors can be turned on and off in 1 b t units |
| | | HOLD release input |
| | | Port 0 interrupt input |
| Port 6 | I/O | 8-bit I/O port |
| P60 to P67 | | • I/O specifiable in 1-bit units |
| 100 to 10 | | Pull-up resistors can be turned on and off in 1 bit units |
| | | • Pin functions |
| | | ANO (P60) to AN/ (P67): AD converter input port |
| Port 7 | I/O | • 8-bit I/O port |
| P70 to P77 | C | • I/O specifiable in (-bit units |
| 170 60 177 | | Puli-up resistors can be turned on and off in 1 bit units |
| OF. | | • Pin functions |
| $\sim V$ | | ANĈ (P70) to AN15 (P77): AD converter input port |

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| | I/O | Description |
|--------------|-----|--|
| Port A | I/O | • 8-bit I/O port |
| PA0 to PA7 | † | • I/O specifiable in 1-bit units |
| 1710 to 1717 | | • Pull-up resistors can be turned on and off in 1 bit units |
| | | Multiplexed pin functions |
| | | PA0: SIO4 data output |
| | | PA1: SIO4 data input/pulse input/output |
| | | PA2: SIO4 clock input/output |
| | | PA3: SIO4 chip select input |
| | | PA4: SLIIC0 clock input |
| | | PA5: SLIIC0 bus input/output/data input PA6: SLIIC0 data output (yead in 2 wire SIO mode) |
| Port B | I/o | PA6: SLIIC0 data output (used in 3-wire SIO mode) |
| POR B | 1/0 | 7-bit I/O portI/O specifiable in 1-bit units |
| PB0 to PB6 | | Pull-up resistors can be turned on and off in 1 bit units |
| | | Multiplexed pin functions |
| | | PB4: SMIIC1 clock input/output |
| | | PB5: SMIIC1 bus input/output/data input |
| | | PB6: SMIIC1 data output (used in 3-wire SIO mode) |
| Port C | I/O | • 5-bit I/O port |
| PC0 to PC4 | + | • I/O specifiable in 1-bit units |
| FC0 10 FC4 | | • Pull-up resistors can be turned on and off in 1 bit units (PC2) |
| | | • Pin functions |
| | | PC0: 32.768 kHz crystal oscillator input |
| | | PC1: 32.768 kHz crystal oscillator output |
| | | PC2: FILT of VCO |
| | | PC3: Ceramic oscillator input |
| | | I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1 bit units (PC2) Pin functions PC0: 32.768 kHz crystal oscillator input PC1: 32.768 kHz crystal oscillator output PC2: FILT of VCO PC3: Ceramic oscillator input PC4: Ceramic oscillator output/VCO output I/O specifiable in 1-bit units |
| Port D | I/O | • 6-bit I/O port |
| PD0 to PD5 | 1 | • 1/O specifiable in 1-bit units |
| | | Pull-up resistors can be turned on and off in 1 bit units |
| TEST | I/O | TEST pin |
| RESB | | Used to communicate with on-chip debugger. |
| | | • Connects an external 100 kQ pull-down resistor. Reset pin |
| | | |

Port Output Types

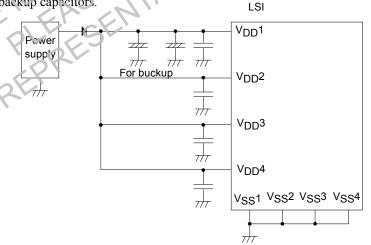
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The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

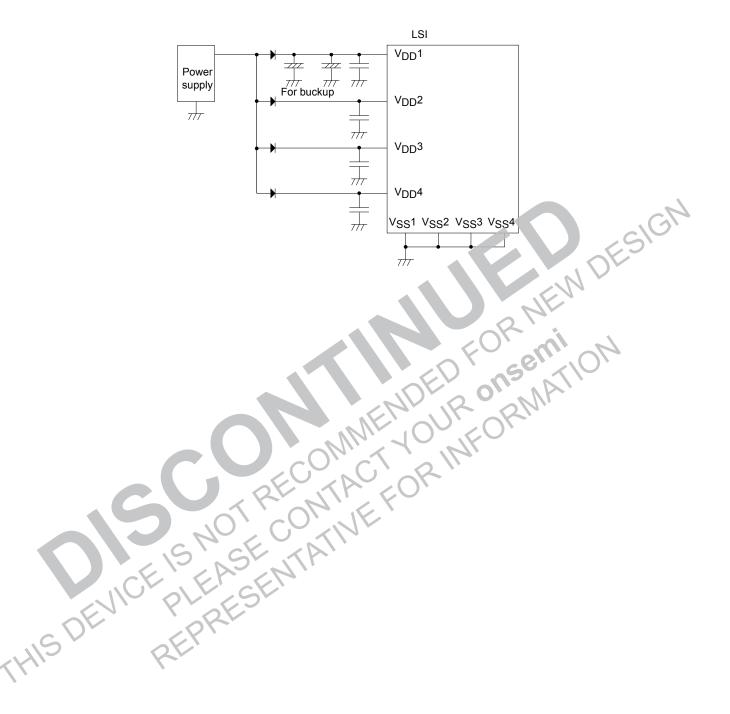
| Port Name | Option Selected in Units of | Output Type | Pull-up Resistor |
|------------|-----------------------------------|---------------------------------|------------------|
| P00 to P07 | 1 bit | CMOS | Programmable |
| | | | |
| P10 to P17 | | Able to program special | |
| P20 to P27 | | functions'output type from | |
| P30 to P37 | | CMOS output or Nch-opendrain | |
| P40 to P47 | | | |
| P50 to P57 | | | |
| P60 to P67 | | | |
| P70 to P77 | | | |
| PA0 to PA7 | | | |
| PB0 to PB6 | | | |
| P60 to P67 | | CMOS | |
| P70 to p77 | | | |
| PD0 to PD5 | | | |
| PC2 | | | |
| PC0 | _ | N-channel open drain | None |
| | | (32.768 kHz crystal oscillator | |
| | | input) | - CO. W |
| PC1 | _ | Nch-open drain | None |
| | | (32.768k kHz crystal oscillator | EV NO N |
| | | output) |) O, VI |
| PC3 | _ | CMOS | None |
| | | (ceramic oscillator input) | 0 |
| PC4 | - | CMOS | None |
| | | (ceranic oscillator output) | |

^{*} Make the following connection to minimize the noise input to the $V_{DD}1$ pin and prolong the backup time. Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, $V_{SS}3$ and $V_{SS}4$ pins.

Example 1: When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2: When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



■ Absolute Maximum Ratings at Ta=25°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

| | D | 0 1 1 | Applicable Pin | G IV | | | Specific | eation | |
|---------------------------|---|------------|---|--|---------------------|-------|----------|----------------------|------|
| | Parameter | Symbol | /Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Max volt | kimum supply age | VDD max | VDD1, VDD2, VDD3, VDD4 | VDD1=VDD2=VDD3 = VDD4 | | -0.3 | | +4.6 | |
| Inpu | ıt voltage | VI (1) | RESB | | | -0.3 | | V _{DD} +0.3 | |
| Inpu | nt/output voltage | VIO(1) | Ports 0, 1, 2 Ports 3, 4,5 Ports 6, 7 Ports A, B, C, D | | | -0.3 | | V _{DD} +0.3 | V |
| High level output current | Peak output current | IOPH (1) | Ports 0, 1, 2, 3 P40 to P45 Ports 7, A, D PB2 to PB6 | CMOS output selected Per applicable pin | | -7.5 | | | |
| tput cur | | IOPH (2) | P46, P47 PB0, PB1 | Per applicable pin | | -12.5 | | | |
| rent | | IOPH (3) | Port 5, 6 PC0 to PC4 | Per applicable pin | | -4.5 | | | (5) |
| | Average output current (Note 1-1) | IOMH (1) | Ports 0, 1, 2, 3 P40 to P45 Ports 5, 6, 7, A PB2 to PB6 Ports D | CMOS output selected Per applicable pin | | -5 | NE | 10 | |
| | | IOMH (2) | P46, P47 PB0, PB1 | Per applicable pin | CO | -10 | en | 10/ | 1 |
| | | IOMH (3) | Port 5, 6 PC0 to PC4 | Per applicable pin | S | -3 | Wh | | |
| | Total output current | ΣΙΟΑΗ (1) | Ports 5 PC0 to PC4 | Total of currents at applicable pins | 00, | -10 | | | |
| | | ΣΙΟΑΉ (2) | Port 6 | Total of currents at applicable pins | R | -10 | | | mA |
| | | ΣΙΟΑΗ (3) | Port 5, 6 PC0 to PC4 | Total of currents at applicable pins |)` | -20 | | | |
| | | ΣΙΟΑΗ (4) | Ports 1,D1 1 20 to P21 | Total of currents at applicable pins | | -20 | | | |
| K | | ΣΙΟΑΉ (5) | P22 (o P27 | Total of currents at applicable pins | | -20 | | | |
| | 110 | ΣΙΟΑΗ (6) | Ports 1 2, D | Total of currents at applicable pins | | -40 | | | |
| | OF. | ΣΙΟΑΗ (7) | Ports 4 | Total of currents at applicable pins | | -20 | | | |
| P | | ΣΙΟΑΉ (8) | Ports 0, 3 | Total of currents at applicable pins | | -20 | | | |
| | | ΣΙΟΑΗ (9) | Ports 0, 3, 4 | Total of currents at applicable pins | | -40 | | | |
| | | ΣΙΟΑΗ (10) | Ports B, 7 | Total of currents at applicable pins | | -20 | | | |
| | | ΣΙΟΑΗ (11) | Ports A | Total of currents at applicable pins | | -20 | | | |
| | ota 1 1. Ave | ΣΙΟΑΗ (12) | Ports 7, A, B | Total of currents at applicable pins | | -40 | | | |

Note 1-1: Average output current refers to the average of output currents measured for a period of 100 ms.

Continued on next page.

Continued from preceding page.

| | Parameter | Symbol | Applicable Pin | Conditions | | | Specific | ation | T |
|--------------------------|-----------------|------------------|-------------------------|--------------------------------------|---------------------|-----|----------|-----------------|------|
| | 1 arameter | Symbol | /Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Lc | Peak output | IOPL (1) | Ports 0, 1, 3, 4 | Per applicable pin | | | | | |
| Low level output current | current | | Ports 7, D | | | | | | |
| evel | | | P20, P21, P24 to P27 | | | | | 15 | |
| 011 | | | PA0 to PA4, PA6, PA7 | | | | | | |
| but | | | PB0 to PB4, PB6, | | | | | | |
| cun | | IOPL (2) | P22, P23 | Per applicable pin | | | | | |
| rent | | , , | PA4, PA5 | | | | | 20 | |
| | | | PB4, PB5 | | | | | | |
| | | IOPL (3) | Ports 5, 6 | Per applicable pin | | | | | |
| | | . , | PC0 to PC4 | | | | | 7.5 | |
| | Average output | IOML (1) | Ports 0, 1, 3, 4 | Per applicable pin | | | | | |
| | current | | Ports 7, D | 11 1 | | | | | |
| | (Note 1-1) | | P20, P21, P24 to P27 | | | | | 12.5 | |
| | , | | PA0 to PA4, PA6, PA7 | | | | | 12.3 | |
| | | | PB0 to PB4, PB6, PB7 | | | | | | |
| | | IOML (2) | P22, P23 | Per applicable pin | | | | | |
| | | 101112 (2) | PA4, PA5 | | | | | 15 | |
| | | | PB4, PB5 | | | | | 11/2 | |
| | | IOML (3) | Ports 5, 6 | Per applicable pin | | | | | |
| | | IOME (3) | PC0 to PC4 | Ter appricable pin | | | | 5 | |
| | Total output | ΣIOAL (1) | Ports 5 | Total of currents at | | | à | | |
| | _ | ZIOAL (1) | PC0 to PC2 | applicable pins | | | | 10 | 1 |
| | current | EIOAI (2) | Port 6 | Total of currents at | 70 | , | 20. | , 10 | m/ |
| | | ΣIOAL (2) | | applicable pins | | | 1 | 10 | |
| | | FIGAL (2) | PC3 to PC4 | | V 2 | 0 | 1/// | | |
| | | ΣIOAL (3) | Port 5, 6 PC0 to PC4 | Total of currents at applicable pins | 21)/ | | | 20 | |
| | | SIOAI (4) | | Total of currents at | Θ | CO. | | | |
| | | ΣIOAL (4) | Ports 1, D | applicable pins | | | | 35 | |
| | | | P20, P21 | | (2) | | | | |
| | | $\Sigma IOAL(5)$ | P22 to P27 | Total of currents at applicable pins | | | | 35 | |
| | | -FIGAL (O | Ports 1 2, D | Total of currents at | | | | | |
| | | ΣΙΟΑL (6) | Ports 1 2, D | applicable pins | | | | 70 | |
| | | ΣΙΟΑL (7) | Port 4 | Total of currents at | | | | | |
| ø | | 210AL (7) | F011 4 | at plicable pins | | | | 35 | |
| | | ΣΙΟΑL (8) | Port 0, 3 | Total of currents at | | | | | |
| | | 210710 (0) | | applicable pins | | | | 35 | |
| | 111 | ΣΙΟΑΙ (2) | Port 0, 3, 4 | Total of currents at | | | | | |
| | EVIL | | | applicable pins | | | | 70 | |
| | OF | ΣΙΟΑL (10) | Port 7, B | Total of currents at | | | | | |
| 3 | | | | applicable pins | | | | 35 | |
| | | ΣlOAL (11) | Port A | Total of currents at | | | | 25 | |
| | | | | applicable pins | | | | 35 | |
| | | ΣΙΟΑL (12) | Port 7, A, B | Total of currents at | | | | 70 | |
| | | | | applicable pins | | | | 70 | |
| | owable power | Pd max | TQFP100 | Ta=-40 to +85°C | | | | | |
| diss | ipation | | | Package with thermal | | | | 460 | m۱ |
| | | | | resistance bord (Note | | | | 400 | "" |
| | | | | 1-2) | | | | | |
| Оре | erating ambient | Topr | | | | 40 | | o <i>e</i> | |
| tem | perature | | | | | -40 | | +85 | |
| Sto | rage ambient | Tstg | | | | | | .125 | °C |
| tem | perature | | | | | -55 | | +125 | |
| | | | | | | | | | |

Note 1-1: Average output current refers to the average of output currents measured for a period of 100 ms. Note 1-2: SEMI standerds thermal resistance board (size: 76.1×114.3×1.6 tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ Allowable Operating Conditions at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

| Parameter | Symbol | Symbol Applicable Pin/Remarks Conditions | | | Specific | ation | | |
|--|----------|--|--|---------------------|----------------------------|-------|---------------------|------|
| Turumeter | Symbol | rppheasie i m/remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Operating supply | VDD (1) | $V_{DD}1 = V_{DD}2 = V_{DD}3$ | 0.081μs≤tCYC≤66μs | | 3.0 | | 3.6 | |
| voltage (Note 2-1) | | | 0.098µs≤tCYC≤66µs | | 2.7 | | 3.6 | |
| Memory sustaining supply voltage | VHD | $V_{DD}1=V_{DD}2=V_{DD}3$ | RAM and register contents sustained in HOLD mode | | 2.0 | | 3.6 | |
| High level input voltage | VIH (1) | Ports 0, 1, 2, 3, 4 Port 5, A, B | | 2.7 to 3.6 | 0.3V _{DD} +0.7 | | v _{DD} | |
| | VIH (2) | Ports 6, 7, D,PC2 | | 2.7 to 3.6 | 0.3V _{DD} +0.7 | | v_{DD} | |
| | VIH (3) | RESB PC0, PC1, PC3, PC4 | | 2.7 to 3.6 | 0.75V _{DD} | | v_{DD} | |
| | VIH (4) | P22, P23, PA4, PA5, PB4, PB5 I2C side | | 2.7 to 3.6 | 0.7V _{DD} | | V _{DD} | |
| Low level input voltage | VIL (1) | When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=0 Ports 0, 6, 7, D, PC2 | | 2.7 to 3.6 | V _{SS} | NE | 0.2V _{DD} | |
| | VIL (2) | When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=1 | | 2.7 to 3.6 | V _{SS} | SW | 0.2V _{DD} | |
| | VIL (3) | CF1, RESB PC0, PC1,PC3, PC4 | M | 2.7 to 3.6 | C _{VSS} | NA | 0.25V _{DD} | |
| | VIL (4) | P22, P23, PA4, PA5, PB4, PB5 I2C side | MME | 2 7 to 3.6 | Vss | | 0.3V _{DD} | |
| Instruction cycle time | tCYC | | 00000 | 3.0 to 3.6 | 0.081 | | 66 | μs |
| (Note 2-2) | | OX | - <u>1220</u> | 2.7 to 3.6 | 0.098 | | 66 | Ċ |
| External system clock frequency | FEXCF(1) | 10°C | • CF2 pin open • System clock frequency division ratio = 1/1 | 3.0 to 3.6 | 0.1 | | 12 | |
| O_{I} | | ASEN | • External system clock DUTY50±5% | 2.7 to 3.6 | 0.1 | | 10 | МН |
| | 00 | LE'SE' | CF2 pin open System clock frequency | 3.0 to 3.6 | 0.2 | | 24 | |
| | | | division ratio = 1/2 | 2.7 to 3.6 | 0.2 | | 20 | |

Continued from preceding page.

| D (| 0 1 1 | Applicable Pin | C I'v' | | | Specific | cation | |
|-----------------|----------|----------------|-------------------------------|---------------------|-----|----------|--------|------|
| Parameter | Symbol | /Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Oscillation | FmCF (1) | PC3 (CF1), | 12 MHz ceramic oscillator | | | | | |
| frequency range | | PC4 (CF2) | mode | 3.0 to 3.6 | | 12 | | |
| (Note 2-3) | | | See Fig. 1. | | | | | |
| | FmCF (2) | PC3(CF1), | 10 MHz ceramic oscillator | | | | | |
| | | PC4(CF2) | mode | 2.7 to 3.6 | | 10 | | MHz |
| | | | See Fig. 1. | | | | | |
| | FmRC | | Internal RC oscillation | | | | | |
| | | | | 2.7 to 3.6 | 0.5 | 1.0 | 2.0 | |
| | FmSLRC | | Internal low-speed RC | 271 26 | 10 | 20 | 4.5 | |
| | | | oscillation | 2.7 to 3.6 | 18 | 30 | 45 | |
| | FsX'tal | XT1, XT2 | 32.768 kHz crystal oscillator | | | | | kHz |
| | | | mode | 2.7 to 3.6 | | 32.768 | | |
| | | | See Fig. 2. | | | | | |
| | FmVCO(1) | | VCO oscillator | | | | | -1 |
| | | | When setting FRQSEL=0 | 2.7 to 3.6 | 12 | | 28 | 19 |
| | | | See Fig. 9. | | | | | |
| | FmVCO(2) | | VCO oscillator | | | | \cup | |
| | | | When setting FRQSEL=1 | 2.7 to 3.6 | 38 | | 70 | MHz |
| | | | See Fig. 9. | | | | 4 | |
| | FmVCO(5) | | VCO oscillator | | | Min | | |
| | | | | 2.7 to 3.6 | OR | Note 2-3 | , | |

Note 2-2: See Tables 1 and 2 for oscillator constant values.

Note 2-3: VCO oscillation frequency = Ceramic oscillator frequency × Setting point of SFLREF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

■ Electrical Characteristics at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

| Doromatar | Symbol | Applicable Pin | Conditions | | | Specific | ation | |
|---------------------------|---------|--|--|---------------------|----------------------|--------------------|-------|------|
| Parameter | Symbol | /Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| High level input current | IIH (1) | Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B,C, D RESB | Output disabled Pull-up resistor off VIN=VDD (including output Tr. off leakage current) | 2.7 to 3.6 | | | 1 | |
| Low level input current | IIL (1) | Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB | Output disabled Pull-up resistor off VIN=VSS (including output Tr. off leakage current) | 2.7 to 3.6 | -1 | | | μΑ |
| High level output voltage | VOH (1) | Ports 0, 1, 2, 3 Ports 5, 6 | IOH=-0.4mA | 3.0 to 3.6 | V _{DD} -0.4 | | | |
| | VOH (2) | Ports A, D, PC2 P40 to P45 PB2 to PB6 | IOH=-0.2mA | 2.7 to 3.6 | V _{DD} -0.4 | | | ,5 |
| | VOH (3) | P46, P47 | IOH=-1.6mA | 3.0 to 3.6 | V _{DD} -0.4 | | 10 | |
| | VOH (4) | PB0, PB1 | IOH=-1.0mA | 2.7 to 3.6 | V _{DD} -0.4 | | N | |
| | VOH (5) | PC0, PC1, | IOH=-1.0mA | 3.0 to 3.6 | V _{DD} -0.4 | NE | | |
| | VOH (6) | PC3, PC4, | IOH=-0.4mA | 2.7 to 3.6 | V _{DD} -0.4 | | | |
| Low level output voltage | VOL(1) | Ports 0, 1, 3, 4 Ports 5, 6, 7, D PC2 | IOL=1.6mA | 3.0 to 3.6 | OU. | SW | 0:4 | V |
| | VOL (2) | P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to PB3, PB6 | 101 = 1.0mA | 2.7 to 3.6 | FOR | Mir | 0.4 | |
| | VOL (3) | P22, P23, | IOL=3.0mA | 3 0 to 3.6 | | | 0.4 | |
| | VOL (4) | PA4, PA5, PB4, PB5 | IOL=1.3mA | 2.7 to 3.6 | | | 0.4 | |
| | VOL (5) | PC0, PC1 | IOL=1.0mA | 3.0 to 3.6 | | | 0.4 | |
| | VOL (6) | PC3, PC4, | IOL=0.4mA | 2.7 to 3.6 | | | 0.4 | |
| Pull-up resistor | Rpu (1) | Ports 0, 1, 2, 3 Ports 4, 5, 6, 7 | VOH=0.9V _{DD} | 3.0 to 3.6 | 15 | 35 | 80 | kΩ |
| | Rpu (2) | Ports A B, D, PC2 | | 2.7 to 3.6 | 15 | 35 | 100 | Kaz |
| Hysteres is voltage | VHYS | RUSB When ports 1, 2, 3, 4, A, B PnFSAn=1 | | 2.7 to 3.6 | | 0.1V _{DD} | | V |
| Pin capacitance | СР | All pins | Pins other than that under test V _{IN} =V _{SS} f=1 MHz Ta=25°C | 2.7 to 3.6 | | 10 | | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

 \blacksquare Serial I/O Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

1-1. Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

| | | Parameter | Symbol | Applicable | Conditions | (11000 1 1 | -, | Specif | ication | |
|---------------|--------------|------------------------|------------------|--------------------------|---|---------------------|------|--------|----------------|--------|
| | Г | arameter | Symbol | Pin/Remarks | | V _{DD} [V] | min | typ | max | unit |
| Seri | Inpu | Period | tSCK (1) | SCK0 (P12) | • See Fig. 6. | | 4 | | | |
| Serial clock | Input clock | Low level | tSCKL (1) | | | | 2 | | | |
| ock | ck | pulse width | (CCKH (1) | | | | | | | |
| | | High level pulse width | tSCKH (1) | | | | 2 | | | |
| | | puise width | tSCKHA (1) | | Automatic communication mode | 2.7 to 3.6 | 6 | | | |
| | | | tSCKHBSY | | • See Fig. 6. • Automatic communication | | | | | tCYC |
| | | | (1a) | | mode | | 23 | | | |
| | | | -COMITMON | | • See Fig. 6. • Mode other than automatic | | | | | |
| | | | tSCKHBSY (1b) | | communication mode | | 4 | | | |
| | | | (10) | | • See Fig. 6. | | | | | |
| | Outpu | Period | tSCK (2) | SCK0 (P12) | • CMOS output selected • See Fig. 6. | | 4 | | | 15 |
| | Output clock | Low level pulse width | tSCKL (2) | | | | | 1/2 | N | - G GY |
| | | High level pulse width | tSCKH (2) | | | | 2 | 1/2 | | tSCK |
| | | | tSCKHA (2) | | Automatic communication mode CMOS output selected | 2.7 to 3.6 | 6 6 | ew | 1017 | |
| | | | tSCKHBSY (2a) | | • See Fig. 6. Automatic communication mode CMOS output selected • see Fig. 6. | OUR | 4 | Wh | 23 | tCYC |
| | | | tSCKHBSY (2b) | | • Mode other than automatic communication mode • See Fig. 6. | RIT | 4 | | | |
| Serial inp | Dat | ta setup time | tsDI (1) | SI0 (P11), SB0 (P11) | • Specified with respect to rising edge of SIOCLK | | 0.03 | | | |
| input | Dai | ta hold time | thDI (1) | SE | • See Fig. 6. | 2.7 to 3.6 | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdD0(1) | SO0 (P10), . B0 (P11) | • (Note 4-1-2) | | | | 1tCYC +0.05 | μs |
| | Output clock | | tdDO (2) | | • (Note 4-1-2) | 2.7 to 3.6 | | | 1tCYC +0.05 | |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

1-2. SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

| | | | | Applicable | | | | Specif | ication | |
|---------------|-------------|-----------------------|--------------------------------|-----------------------------|---|-----------------------------|-----------|--------|----------------|-------|
| | P | arameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Seria | Inpu | Period | tSCK (3) | SCK0 (P12) | • See Fig. 6. | | 2 | | | |
| Serial clock | Input clock | Low level pulse width | tSCKL (3) | | | | 1 | | | |
| k | , | High level | tSCKH (3) | | | 2.7 to 3.6 | 1 | | | tCYC |
| | | pulse width | tSCKHBSY (3) | | | | 2 | | | |
| Serial input | Dat | a setup time | tsDI (2) | SI0 (P11), SB0 (P11) | • Specified with respect to rising edge of SIOCLK | | 0.03 | | | |
| 1 innut | Dat | a hold time | thDI (2) | SB0 (F11) | • See Fig. 6. | 2.7 to 3.6 | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdD0 (3) | SO0 (P10), SB0 (P11) | • (Note 4-2-2) | 2.7 to 3.6 | | (| 11CYC +0.05 | μs |
| N N | ote | 4-2-2: Specia | fied with resp | pect to the fa | etical values. Add marginalling edge of SIOCLK. sen drain output mode S | Specified as see Fig. 6. | the inter | | to the tim | ne an |
| N | ote | 4-2-2: Specia | fied with resp t change beg | pect to the fains in the op | alling edge of SIOCLK. Den drain output mode S | Specified as see Fig. 6. | the inter | | to the time | e an |

2-1. SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

| | | | - | Applicable | eristics (Wakeup Fund | | | | ication | |
|---------------|--------------|------------------------|---------------|-------------------------|---|---------------------|------|-----|----------------|------|
| | ŀ | Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Seri | Inpu | Period | tSCK (4) | SCK1 (P45) | • See Fig. 6. | | 4 | | | |
| Serial clock | Input clock | Low level pulse width | tSCKL (4) | | | | 2 | | | |
| ĺ, | | High level | tSCKH (4) | | | | 2 | | | |
| | | pulse width | tSCKHA (4) | | Automatic communication mode See Fig. 6. | 2.7 to 3.6 | 6 | | | |
| | | | tSCKHBSY (4a) | | Automatic communication modeSee Fig. 6. | | 23 | | | tCYC |
| | | | tSCKHBSY (4b) | | Mode other than automatic communication modeSee Fig. 6. | | 4 | | | |
| | Output clock | Period | tSCK (5) | SCK1 (P45) | • CMOS output selected • See Fig. 6. | | 4 | | | ,5 |
| | t clock | Low level pulse width | tSCKL (5) | | | | | 1/2 | ND | tSCK |
| | | High level pulse width | tSCKH (5) | | | | | 1/2 | | tsck |
| | | | tSCKHA (5) | | Automatic communication mode CMOS output selected See Fig. 6. | 27 to 36 | 6 | ew | 101 | 7 |
| | | | tSCKHBSY (5a) | | * Automatic communication mode CMOS output selected * See Fig. 6. | OUR | 4 | W | 23 | tCYC |
| | | | tSCKHBSY (5b) | R | • Mode other than automatic communication mode • See Fig. 6. | R | 4 | | | |
| Serial in | Dat | ta setup time | tsDI (3) | SU1 (P44), SB1 (P44) | • Spenfied with respect to rising edge of SIOCLK | | 0.03 | | | |
| input | Dai | ta hold time | thDI (3) | SE | • See Fig. 6 | 2.7 to 3.6 | 0.03 | | | |
| Serial output | input clock | Output delay | tdDv(4) | SO1 (F43), SB1 (P44) | • (Note 4-3-2) | | | | 1tCYC +0.05 | μs |
| | Output clock | | tdDO (5) | | • (Note 4-3-2) | 2.7 to 3.6 | | | 1tCYC +0.05 | |

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

2-2. SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

| Prin/Remarks VDD [V] min typ max unit | Pin/Remarks VDD [V] min typ max unit graph and typ max unit graph an | Parameter | | Parameter Symbol Applicable Conditions | | | | | Specification | | | |
|---|--|-----------|---------|--|----------------|---|---|---------------------|---------------------|--------------|-------|-------|
| Low level pulse width High level pulse width Pulse width | Low level pulse width High level pulse width | | ř | 'arameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| High level pulse width tSCKHBSY (6) tSCKHBSY (6) tSCKHBSY | High level pulse width tSCKHBSY (6) | Seri | Inpu | Period | tSCK (6) | SCK1 (P45) | • See Fig. 6. | | 2 | | | |
| The little Dulse width SCKHBSY 1 2 2 2 2 2 2 2 2 2 | The little Dulse width SCKHBSY 1 2 2 2 2 2 2 2 2 2 | al clock | t clock | | tSCKL (6) | | | | 1 | | | |
| Data setup time tsDI (4) SBI (P44), SBI (P44) *See Fig. 6. See Fig. 6. Solution of the specifications are theoretical values. Add margin depending on its use. Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | Data setup time tsDI (4) SBI (P44), SBI (P44) *See Fig. 6. See Fig. 6. Solution of the specifications are theoretical values. Add margin depending on its use. Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | | | _ | tSCKH (6) | | | 2.7 to 3.6 | 1 | | | tCYC |
| Data hold time thDI (4) SB1 (P44) rising edge of SIOCLK See Fig. 6. 2.7 to 3.6 Output delay time time thDI (6) SO1 (P43), SB1 (P44) Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | Data hold time thDI (4) SB1 (P44) rising edge of SIOCLK See Fig. 6. 2.7 to 3.6 Output delay time time thDI (6) SO1 (P43), SB1 (P44) Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | | | pulse width | | | | | 2 | | | |
| Serial of time SO1 (P43), SB1 (P44) S | Serial of time SO1 (P43), SB1 (P44) S | Serial i | | | | | rising edge of SIOCLK | | 0.03 | | | |
| Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. o. | Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | nput | Dat | ta hold time | thDI (4) | | • See Fig. 6. | 2.7 to 3.6 | 0.03 | | | |
| Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | Serial | Input | | tdD0 (6) | | • (Note 4-4-2) | | | | | μs |
| Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. | Note 4-4-1: These specifications are theoretical values. Add margin depending on its use. Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. o. | output | clock | | | | | | | | | |
| | IS NOT CONVE | | | 4-4-2: Spec | ified with res | ns are theore pect to the fi gins in the op | etical values. Add marginalling edge of SIOCLK. Den drain output mode. S | | on its us the inter | e. vai up | +0.05 | ne an |
| EVICEPLEESER | | N | lote | 4-4-2: Specoutpu | ified with res | ns are theore pect to the facins in the op | etical values. Add marginalling edge of SIOCLK. Seen drain output mode. S | | on its us the inter | e. Vai up | +0.05 | ne an |

3-1. SIO4 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-5-1)

| | | | | Applicable | eristics (Wakeup Fund | | | | ication | |
|---------------|--------------|------------------------|--------------|-------------|---|---------------------|----------------|------|---------|------|
| | F | Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Seri | Inpu | Period | tSCK (7) | SCK4 (PA2) | • See Fig. 6. | | 4 | | | |
| Serial clock | Input clock | Low level | tSCKL (7) | | | | 2 | | | |
| ock | ck | pulse width | -G GYYYY (5) | | | | | | | |
| | | High level pulse width | tSCKH (7) | | | | 2 | | | |
| | | puise width | tSCKHA (7) | | • Automatic communication mode | 2.7 to 3.6 | 6 | | | |
| | | | tSCKHBSY | | See Fig. 6.Automatic communication | 2.7 10 3.0 | | | | tCYC |
| | | | (7a) | | mode | | 23 | | | |
| | | | (74) | | • See Fig. 6. | | 23 | | | |
| | | | tSCKHBSY | | • Mode other than automatic | | | | | |
| | | | (7b) | | communication mode | | 4 | | | |
| | | | | | • See Fig. 6. | | | | | , G |
| | Output clock | Period | tSCK (8) | SCK4 (PA2) | • CMOS output selected • See Fig. 6. | | 4 | | .0 | |
| | cloc | Low level | tSCKL (8) | | | | | 1/2 | 11. | |
| | × | pulse width | | | | |) | | | tSCK |
| | | High level pulse width | tSCKH (8) | | | | 2 | 1/2 | | |
| | | puise widin | tSCKHA (8) | | * Automatic communication | | .0) | -60 | - | |
| | | | tockina (6) | | mode | .0 | C | S/,, | ~(O) | |
| | | | | | * CMOS output selected | 2.7 to 3.6 | 6 | | | |
| | | | | | • See Fig. 6. |) 2 | 0, | WL | | |
| | | | tSCKHBSY | | * Automatic communication | | OR | | | |
| | | | (8a) | | mode | 0,4 | 4 | | 23 | tCYC |
| | | | | | * CMOS oup it selected | 11/1 | | | 23 | |
| | | | tSCKHBSY | | • See Fig. 6. • Mode other than automatic | 6, | | | | |
| | | | (8b) | (2) | communication mode |) ` | 4 | | | |
| | | | (00) | \sim | See Fig. 6. | | 7 | | | |
| Seri | Da | ta setup time | tsDI (5) | S14 (PA1), | • Specified with respect to | | 0.02 | | | |
| nali | | | G | SB4 (PA1) | rising edge of SIOCLK | | 0.03 | | | |
| nput | Da | ta hold time | thDI (5) | 20, " | • See Fig. 6. | 2.7 to 3.6 | | | | |
| | 1 | I/C | OLE | SE | | | 0.03 | | | |
| Seri | Inp | Output delay | tdD0 (7) | SO4 (PA0), | (Note 4-5-2) | | | | | |
| Serial output | Input clock | time | 201 | SB14(PA1) | | | | | 1tCYC | |
| tg u | č | | 0V. | | | | | | +0.05 | μs |
| | | | | | | | | | | |
| | 0 | | tdDO (8) | | • (Note 4-5-2) | 2.7 to 3.6 | | | | |
| | Output clock | | | | , | | | | 1,6776 | |
| | t clo | | | | | | | | 1tCYC | |
| | ck | | | | | | | | +0.05 | |
| | | | | | | | | | | |

Note 4-5-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-5-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

3-2. SIO4 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-6-1)

| Parameter Symbol Pin/Remarks Conditions VDD [V] min typ max un pin |
|--|
| Comparison Com |
| High level pulse width tSCKH (9) tSCKHBSY (9) 2 1 2 |
| Data setup time tsDI (6) SI4 (P44), Specified with respect to rising edge of SIOCLK Data hold time thDI (6) SO4 (P43), See Fig. 6. South of the pulse width South of the pulse width of the pulse width South of the pulse width of the pulse width South of the pulse width South of the pulse width of the pulse width South of the pulse width of the pulse width of the pulse width of the pulse width South of the pulse width of the pulse |
| SCKHBSY (9) 2 2 |
| SB4 (P44) rising edge of SIOCLK 0.03 0.03 |
| Output delay time SO4 (P43), SB4(P44) SO4 (P44) SO5 (Note 4-6-2) SO5 (P43), SB4(P44) SO5 (P43), SB5 (P43), S |
| Output delay time SO4 (P43), SB4(P44) S |
| Note 4-6-1: These specifications are theoretical values. Add margin depending on its use. Note 4-6-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6. |
| |

4-1. SMIICO Simple SIO Mode Input/Output Characteristics

| | Parameter | Symbol | Applicable | Conditions | | | Specif | fication | 1 |
|---------------|-------------------------------|------------|-----------------------------------|--|---------------------|------|--------|----------------|------|
| | | ~, | Pin/Remarks | | V _{DD} [V] | min | typ | max | unit |
| Serial clock | Period Low level | tSCK (10) | SM0CK (P22) | See Fig. 6. | | 4 | | | |
| clock | Low level pulse width | tSCKL (10) | | | 2.7 to 3.6 | 2 | | | |
| | High level pulse width | tSCKH (10) | | | | 2 | | | tCY |
| oles O | Period | tSCK (11) | SM0CK (P22) | • CMOS output selected • See Fig. 6. | | 4 | | | |
| | Period Low level pulse width | tSCKL (11) | , | | 2.7 to 3.6 | | 1/2 | | |
| | High level pulse width | tSCKH (11) | | | | | 1/2 | | tSC |
| Serial input | Data setup time | tsDI (7) | SM0DA (P23), | • Specified with respect to rising edge of SIOCLK | 27. 26 | 0.03 | | | |
| input | Data hold time | thDI (7) | | • See Fig. 6. | 2.7 to 3.6 | 0.03 | | N C | |
| Serial output | Output delay time | tdD0 (10) | SM0DO (P24), SM0DA (P23) | Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts | 2.7 to 3.6 | OP | NF | 1tCYC +0.05 | μs |
| | | | | changing. • See Fig. 6. | 20 | 7 | e, | (O) | |
| | | | | retical values. Add margin | OUR | FOR | Mil | | |

4-2. SMIIC0 I²C Mode Input/Output Characteristics

| | P. | arameter | | Symbol | Applicable | Conditions | | | Specif | ication | 1 |
|-------|-----------------|---------------------------------------|--------|----------|----------------------------|--|---------------------|-----|--------|---------|-------|
| | | | | - | Pin/Remarks | | V _{DD} [V] | min | typ | max | unit |
| Clock | Input clock | Period | | tSCL | SM0CK (P22) | • See Fig. 8. | | 5 | | | |
| | lock | Low level pulse widt | h | tSCLL | | | 2.7 to 3.6 | 2.5 | | | TCL |
| | | High level pulse widt | | tSCLH | | | | 2 | | | Tfilt |
| | Outpu | Period | | tSCLx | SM0CK (P22) | • Specified as interval up to time when output state starts | | 10 | | | |
| | Output clock | Low level | h | tSCLLx | | changing. | 2.7 to 3.6 | | 1/2 | | |
| | | High level | | tSCLHx | | | | | 1/2 | | tSCL |
| pin | ıs inp | X and SM0E out spike ssion time | | tsp | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | 2.7 to 3.6 | | | ı | Tfilt |
| | | | Input | tBUF | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | | 2.5 | | N | Tfilt |
| | weer | ease time n start and | Output | tBUFx | SM0CK (P22) SM0DA (P23) | Standard clock mode Specified as interval up to time when output state starts changing High-speed clock mode Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 5.5 | erc | | μѕ |
| | | | Inpu | tHD;STA | SMOCK (P22) SMODA (P23) | • when SM/IC register control br., I2CS/HDS=0 • See Fig. 8. | RIN | 2.0 | | | Tfilt |
| | ırt/re: | start on hold | out | 25 | OF | • When SMIIC register control bit 12CSHDN=1 • See Fig. 8. | 2.7 to 3.6 | 2.5 | | | Tint |
| tin | | on more | S Ou | tHD;STAx | SM0CK (P22) SM0DA (P23) | Standard clock mode Specified as interval up to time when output state starts changing. | | 4.1 | | | |
| | |) ' | Output | REP | | High-speed clock mode Specified as interval up to time when output state starts changing. | | 1.0 | | | μs |
| | | | Input | tSU;STA | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | | 1.0 | | | Tfilt |
| | start up tii | condition me | | tSU;STAx | SM0CK (P22) SM0DA (P23) | • Standard clock mode • Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 5.5 | | | |
| | | | Output | | | High-speed clock mode Specified as interval up to time when output state starts changing. | | 1.6 | | | - μs |

| D | | Cl1 | Applicable | Conditions | | | Specifica | ation | |
|--------------------------------------|--------|----------|----------------------------|--|---------------------|--------------------|-----------|-------|-------|
| Parameter | | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | Min | typ | max | Unit |
| | Input | tSU;STO | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | | 1.0 | | | Tfilt |
| Stop condition setup time | Ou | tSU;STOx | SM0CK (P22) SM0DA (P23) | • Standard clock mode • Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 4.9 | | | |
| | Output | | | High-speed clock mode Specified as interval up to time when output state starts changing. | | 1.1 | | | μѕ |
| | Input | tHD;DAT | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | | 0 | | | |
| Data hold time | Output | tHD;DATx | SM0CK (P22) SM0DA (P23) | • Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 1 | | 1.5 | Tfilt |
| | Input | tSU;DAT | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | | 1 | NE | 2 | |
| Data setup time | Output | tSU;DATx | SM0CK (P22) SM0DA (P23) | Specified as interval up to time when output state starts changing | 2.7 to 3.6 | itSCL- 1.5Tfilt | swi | 101 | Tfilt |
| | Input | tF | SM0CK (P22) SM0DA (P23) | • See Fig. 8. | 2.7 to 3.6 | o P | NA. | 300 | |
| SM0CK and SM0DA pins fall time | Output | tF | SMOCK (P22) SMODA (P23) | • hen SMUC register control bits FSLW-1, P5V=1 | R3 M | 20+0.1Cb | | 250 | ns |
| | out | | TR | SM0CK SM0DA port output FAST mode Ch<400pF | 3.0 to 3.6 | | | 100 | |

Note 4-8-1. These specifications are theoretical values. Add margin depending on its use.

Note 4-8-2: The value of Tfilt is determined by the values of the register SMICOBRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency. THIS DEV

| BRP1 | BRP0 | Tfilt |
|------|------|--------|
| 0 | 0 | tCYC×1 |
| 0 | 1 | tCYC×2 |
| 1 | 0 | tCYC×3 |
| 1 | 1 | tCYC×4 |

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

 $250 \text{ ns} \ge T \text{filt} > 140 \text{ ns}$

Note 4-8-3: Cb represents the total loads (in pF) connected to the bus pins. $Cb \le 400 \text{ pF}$

Note 4-8-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

 $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$

BRDQ (bit5) = 1

SCL frequency setting ≤ 100 kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

 $250 \text{ ns} \ge T \text{filt} > 140 \text{ ns}$

BRDQ (bit5) = 0

SCL frequency setting ≤ 400 kHz

5-1. SMIIC1 Simple SIO Mode Input/Output Characteristics

| | Parameter | Symbol | Applicable | Conditions | | | Specif | fication | |
|---------------|-----------------------------------|------------|--------------------------|--|---------------------|------|-----------------|----------|------|
| | | | Pin/Remarks | | V _{DD} [V] | min | typ | max | unit |
| Serial clock | Period Low level | tSCK (12) | SM0CK (PB4) | See Fig. 6. | | 4 | | | |
| clock | Low level pulse width | tSCKL (12) | | | 2.7 to 3.6 | 2 | | | |
| | High level pulse width | tSCKH (12) | | | | 2 | | | tCYO |
| | Period | tSCK (13) | SM0CK (PB4) | • CMOS output selected • See Fig. 6. | | 4 | | | |
| | Period Coc Low level pulse width | tSCKL (13) | , | Č | 2.7 to 3.6 | | 1/2 | | |
| | High level pulse width | tSCKH (13) | | | | | 1/2 | | tSCI |
| Serial input | Data setup time | tsDI (8) | SM0DA (PB5), | • Specified with respect to rising edge of SIOCLK | | 0.03 | | | |
| input | Data hold time | thDI (8) | | • See Fig. 6. | 2.7 to 3.6 | 0.03 | | 710 | |
| Serial output | Output delay time | tdD0 (12) | SM0DO (PB6), SM0DA | • Specified with respect to falling edge of SIOCLK • Specified as interval up to | | | NF | 1tCYC | μs |
| ıtput | | | (PB5) | time when output state starts changing. | 2.7 to 3.6 | OK | 200 | +0.05 | 7 |
| | | | | See Fig. 6. | 0.5 | 1 | 50 | 410 | Ì |
| | | | | etical values. Add margo | OUR | COP | δM_{II} | | |

5-2. SMIIC1 I²C Mode Input/Output Characteristics

| | р | arameter | | Symbol | Applicable | Conditions | | | Specif | ication | |
|-------|----------------|---------------------------------|--------|----------|----------------------------|--|---------------------|-----|----------|---------|-------|
| | | arameter | | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Clock | Input clock | Period | | tSCL | SM1CK (PB4) | • See Fig. 8. | | 5 | | | |
| | lock | Low level pulse widt | h | tSCLL | | | 2.7 to 3.6 | 2.5 | | | |
| | | High level | | tSCLH | | | · | 2 | | | Tfilt |
| | Outp | Period | | tSCLx | SM1CK (PB4) | • Specified as interval up to time when output state starts | | 10 | | | |
| | Output clock | Low level pulse widt | h | tSCLLx | (1) | changing. | 2.7 to 3.6 | | 1/2 | | |
| | | High level pulse widt | | tSCLHx | | | | | 1/2 | | tSCL |
| pir | ıs inp | X and SM0E put spike ssion time | | tsp | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | 2.7 to 3.6 | | | 1 | Tfilt |
| | | | Input | tBUF | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | | 2.5 | | NI | Tfilt |
| | wee | ease time n start and | Output | tBUFx | SM1CK (PB4) SM1DA (PB5) | Standard clock mode Specified as interval up to time when output state starts changing High-speed clock mode Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 5.5 | NA NA | 710 | μѕ |
| | | | In | tHD;STA | SM1CK (PB4) SM1DA (PB5) | • hen SMIIC register control bit, L2CS HDS=0 • See Fig. 8. | RIN | 2.0 | | | |
| | | estart | Input | | JOTE | • When SMIIC register control bit 12CSHDC=1 • See Fig. 3. | 27. 26 | 2.5 | | | Tfilt |
| tin | ie . | on hold | S Ou | tHD;STAx | SM1CK (PB4) SM1DA (PE5) | * Standard clock mode * Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 4.1 | | | |
| | |) * | Output | REP | | • High-speed clock mode • Specified as interval up to time when output state starts changing. | | 1.0 | | | μѕ |
| | | | Input | tSU;STA | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | | 1.0 | | | Tfilt |
| | start up ti | condition me | | tSU;STAx | SM1CK (PB4) SM1DA (PB5) | • Standard clock mode • Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 5.5 | | | |
| | | | Output | | | High-speed clock mode Specified as interval up to time when output state starts changing. | | 1.6 | | | - μs |

| Parameter | | Symbol | Applicable | Conditions | | | Specifica | ation | |
|--------------------------------------|--------|----------|----------------------------|--|---------------------|--------------------|-----------|-------|-------|
| Parameter | | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | Min | typ | max | Unit |
| | Input | tSU;STO | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | | 1.0 | | | Tfilt |
| Stop condition setup time | Ou | tSU;STOx | SM1CK (PB4) SM1DA (PB5) | Standard clock mode Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 4.9 | | | |
| | Output | | | High-speed clock mode Specified as interval up to time when output state starts changing. | | 1.1 | | | μs |
| | Input | tHD;DAT | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | | 0 | | | |
| Data hold time | Output | tHD;DATx | SM1CK (PB4) SM1DA (PB5) | Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 1 | | 1.5 | Tfilt |
| | Input | tSU;DAT | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | | 1 | NE | 2 | |
| Data setup time | Output | tSU;DATx | SM1CK (PB4) SM1DA (PB5) | Specified as interval up to time when output state starts changing | 2.7 to 3.6 | itSCL- 1.5Tfilt | emi | 101 | Tfilt |
| | Input | tF | SM1CK (PB4) SM1DA (PB5) | • See Fig. 8. | 2.7 to 3.6 | o P | A M | 300 | |
| SM0CK and SM0DA pins fall time | Out | tF | SM1CK (PB4) SM1DA (PB5) | • hen SMIIC register control bits FSLW=1, PHV=1 | 3 17 | 20+0.1Cb | | 250 | ns |
| | out | | TR | SM0CK S140DA port output FAST made Cb ≤ 400pF | 3 to 3.6 | | | 100 | |

Note 4-10-1. These specifications are theoretical values. Add margin depending on its use.

Note 4-10-2: The value of Tfilt is determined by the values of the register SMIC1BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

| BRP1 | BRP0 | Tfilt |
|------|------|--------|
| 0 | 0 | tCYC×1 |
| 0 | 1 | tCYC×2 |
| 1 | 0 | tCYC×3 |
| 1 | 1 | tCYC×4 |

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

 $250 \text{ ns} \ge T \text{filt} > 140 \text{ ns}$

Note 4-10-3: Cb represents the total loads (in pF) connected to the bus pins. $Cb \le 400 \text{ pF}$

Note 4-10-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

 $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$

BRDQ (bit5) = 1

THIS DE

SCL frequency setting ≤ 100 kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC1BRG as follows:

 $250 \text{ ns} \ge T \text{filt} > 140 \text{ ns}$

BRDQ (bit5) = 0

SCL frequency setting $\leq 400 \text{ kHz}$

6-1. SLIIC0 Simple SIO Mode Input/Output Characteristics

| Phorecomparis VDD [V] min typ max unit look of the palse width High level palse width (PAS). Specified with respect to frising edge of SIOCLK 'See Fig. 6. Output delay time talD0 (13) SLODO (PAS) the specified with respect to falling edge of SIOCLK (PAS) the when output state starts changing. See Fig. 6. Note 4-11-1: These specifications are theoretical values. Add marsin spending on the specification of the values of the palse of the | <u> </u> | | Parameter | Symbol | Applicable Pin/Remarks | Conditions | X7 [X7] | | Specific | | |
|--|---------------|----------|-----------------|--------------|------------------------|---|--------------------|-----------|----------|-----|------|
| Pulse width High level pulse width Pulse width Data setup time tsDI (9) Data hold time thDI (9) See Fig. 6. Output delay time tdD0 (13) SL0DA (PA5), See Fig. 6. See Fig. 6. Output delay time tdD0 (13) SL0DA (PA6), SL0DA (PA6), SL0DA (PA6), SL0DA (PA6) SL0DA (PA6), SL0DA (PA | Ser | Inp | Period | tSCK (13) | SL0CK | See Fig. 6. | vDD[v] | | іур | max | unit |
| High level pulse width Post Data setup time tsDI (9) Data hold time thDI (9) Data hold time thDI (9) See Fig. 6. | ial clock | ut clock | | tSCKL (13) | (PA4) | | 2.7 to 3.6 | | | | tCYC |
| Data setup time tsD1 (9) SL0DA (PA5), *Specified with respect to rising edge of SIOCLK 2.7 to 3.6 0.03 0.03 0.03 See Fig. 6. *Specified with respect to rising edge of SIOCLK 2.7 to 3.6 0.03 0.03 0.03 0.03 See Fig. 6. *Specified with respect to falling edge of SIOCLK *Specified as interval up to time when output state starts changing. *See Fig. 6. *See Fig. 6. *Specified as interval up to time when output state starts changing. *See Fig. 6. | | | High level | tSCKH (13) | | | | 2 | | | |
| Output delay time ltdD0 (13) SL0DO (PA6), falling edge of SIOCLK SL0DA (PA5) SL0DA (PA5) time when output state starts changing. See Fig. 6. Note 4-11-1: These specifications are theoretical values. Add margin depending on its use. | Serial | Dat | | tsDI (9) | | | 25. 26. | 0.03 | | | |
| (PA6), SLODA Specified as interval up to time when output state starts changing. See Fig. 6. Note 4-11-1: These specifications are theoretical values. Add margin depending on its use. | input | Dat | ta hold time | thDI (9) | | • See Fig. 6. | 2.7 to 3.6 | 0.03 | | | |
| Note 4-11-1: These specifications are theoretical values. Add margin depending on its use. | Serial output | Out | tput delay time | tdD0 (13) | (PA6), SL0DA | falling edge of SIOCLK • Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | | | | μs |
| CONNE POR NE POR NATION CONTRE FOR INFORMATION CONTRE FOR INFORMATION | N | ote | 4-11-1: Thes | e specificat | ions are the | | in dependi | ng on its | use. | W. | |
| | S | | EVICE | PLEPER | OT RESE | ECONINE PO CONTACTO NTATIVE FO | DED OUR DRIN | FOF | MA | | |

6-2. SLIIC1 I²C Mode Input/Output Characteristics

| | | | G 1 1 | Applicable | O IV | | | Specifi | cation | |
|---------------------|--|--------|----------|-----------------------------|---|---------------------|--------------------|---------|--------|-------|
| P | Parameter | | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | Min | typ | max | Unit |
| Input clock | Period | | tSCL | SL0CK (PA4) | • See Fig. 8. | | 5 | | | |
| lock | Low level pulse widt | h | tSCLL | | | 2.7 to 3.6 | 2.5 | | | Tfilt |
| | High level pulse widt | | tSCLH | | | | 2 | | | |
| pins inj | X and SL0DA put spike ssion time | Λ. | tsp | SL0CK (PA4) SL0DA (PA5) | • See Fig. 8. | 2.7 to 3.6 | | | 1 | Tfilt |
| | lease time en start and | Input | tBUF | SL0CK (PA4) SL0DA (PA5) | • See Fig. 8. | 2.7 to 3.6 | 2.5 | | | Tfilt |
| Start/re | estart | | tHD;STA | SL0CK (PA4) SL0DA (PA5) | • When SMIIC register control bit, I2CSHDS=0 | | 2.0 | | | K. |
| condition time | on hold | Input | | | • See Fig. 8. • When SMIIC register control bit I2CSHDS=1 • See Fig. 8. | 2.7 to 3.6 | 2.5 | NE | 1 | Tfilt |
| Restart setup ti | condition | Input | tSU;STA | SL0CK (PA4) SL0DA (PA5) | • See Fig. 8. | 2.7 to 3.6 | 1.0 | sell | (10) | Tfilt |
| Stop co | ondition ime | Input | tSU;STO | SLOCK (PA4) SLODA (PA5) | Soe Fig. 8. CONNER | 2.7 to 3.6 | 1.0 | | | Tfilt |
| Data la | old time | Input | 1/9 | SLOCK (PA4) SLODA (PA5) | See Fig. 8 | 27to 26 | 0 | | | m.c.1 |
| Data no | ana anne | Output | tHD:DATx | SLOCK (PA-1) SLODA (PA5) | Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 1 | | 1.5 | Tfili |
| 3 | | Input | tSU;DAT | SL0CK (PA4) SL0DA (PA5) | • See Fig. 8. | | 1 | | | |
| Data se | etup time | Output | tSU;DATx | SL0CK (PA4) SL0DA (PA5) | Specified as interval up to time when output state starts changing. | 2.7 to 3.6 | 1tSCL- 1.5Tfilt | | | Tfil |

7. UARTO Operating Conditions at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

| Donomoton | Cl1 | Applicable | Can disiana | _ | | Speci | fication | |
|---------------|--------|-------------|-------------|---------------------|-----|-------|----------|--------|
| Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Transfer rate | UBR0 | U0RX (P13), | | | | | | |
| | | U0TX (P14), | | 27. 26 | 4 | | | DOGWO |
| | | U0BRG | | 2.7 to 3.6 | 4 | | 8 | tBGCYC |
| | | (P07) | | | | | | |

Note 4-9: tBGCYC denotes one cycle of the baudrate clock source.

8. UART2 Operating Conditions at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

| D | G 1.1 | Applicable | C IV | | | Speci | ification | |
|---------------|--------|----------------------------|------------|---------------------|-----|-------|-----------|--------|
| Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Transfer rate | UBR2 | U2RX (P16), U2TX (P17), | | | | | | |
| | | 0217 (F17), | | 2.7 to 3.6 | 8 | _ < | 4096 | tBGCYC |
| | | | | | | | | 15 |

| | | | | | | | | 25 |
|----------------|------------|-------------|----------------------------------|---------------------|---------|----------|-----------|--------|
| Note 4-10: tBG | CYC denote | s one cycle | of the baudrate clock so | ource. | | | | |
| 0 IIADT2 Ono | rating Con | ditions of | Γa=–40 to +85°C, V _{SS} | 1-Vgg2-V | Igg Vic | 704-0V | N | |
| 9. UAKTS OPE | rating Con | uitions at | 1a-40 to +83 C, VSS | 1-1882-1 | VSS3-VS | 55 1-0 V | | : |
| | 0 1 1 | Applicable | O THE | | | Spec | itication | |
| Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| Transfer rate | UBR3 | U3RX (P34), | | | - P | -0 | | |
| | | U3TX (P35), | | 2.7 to 3.6 | 8 | 2 | 4096 | tBGCYC |
| | | | | 70, | 20 | No | | |

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source

■ Pulse Input Conditions at Ta=-40 to +85°C,

| D | Sample - | A li a la Dia /B (a | OLIVE | | | Specif | ication | |
|----------------|--------------|------------------------|---------------------------------|---------------------|-----|--------|---------|-------|
| Parameter | Symbol | Applicable Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| High/low level | tPIH (1) | ıN Γ0 (P30), | • Int :rrupt source flag can be | | | | | |
| pulse width | tPIL (1) | INT1 (P31), | set. | | | | | |
| 11 | O^{\prime} | INT2 (P32), | • Event inputs for timers 2 and | | | | | |
| (N) | 1 | INT3 (P33). | 3 are enabled. | 27. 26 | 2 | | | , CVC |
| | | INT4 (P20), | | 2.7 to 3.6 | 2 | | | tCYC |
| SV | | IN15 (P21), | | | | | | |
| | 2 | NΤ6 (P40), | | | | | | |
| | | INT7 (P41) | | | | | | |
| | tPIL (2) | RESB | Resetting is enabled. | 2.7 to 3.6 | 10 | | | μs |

■ AD Converter Characteristics at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

1. 12-bit AD Conversion Mode

| | | Applicable Pin | | | | Specif | ication | |
|----------------------------|--------|----------------------------|----------------------------|------------|----------|--------|----------|------|
| Parameter | Symbol | /Remarks | Conditions | VDD[V] | min | typ | max | unit |
| Resolution | NAD | AN0 (P60) | | 2.7 to 3.6 | | 12 | | bit |
| Absolute accuracy | ETAD | to AN7 (P67), AN8 (P70) | (Note 6-1) | 2.7 to 3.6 | | | ±16 | LSB |
| Conversion time | TCAD12 | | Conversion time calculated | 3.0 to 3.6 | 64 | | 115 | |
| | | , , , | | 2.7 to 3.6 | 128 | | 230 | μs |
| Analog input voltage range | VAIN | | | 2.7 to 3.6 | V_{SS} | | v_{DD} | V |
| Analog port | IAINH | | VAIN=V _{DD} | 2.7 to 3.6 | | | 1 | |
| input current | IAINL | | VAIN=V _{SS} | 2.7 to 3.6 | -1 | | | μА |

- Conversion time calculation formula: TCAD12= ($\frac{52}{AD \text{ division ratio}}$ +2) × tCYC

2. 8-bit AD Conversion Mode

| | | Applicable Pin | | | | Specifi | cation | |
|----------------------------|--------|----------------------------|----------------------------|--------------------------|--------------|---------|-------------|------|
| Parameter | Symbol | /Remarks | Conditions | V _{DD} [V] | min | typ | ınax | unit |
| Resolution | NAD | AN0 (P60) | | 2.7 to 3.6 | 0 | 8 | | bit |
| Absolute accuracy | ETAD | to AN7 (P67), AN8 (P70) | (Note 6-1) | 2.7 to 3.6 | <0' | -60 | ±1.5 | LSB |
| Conversion time | TCAD8 | to AN15 (P77) | Conversion time calculated | 3.0 to 3.6 2.7 to 3.6 | 39 79 | 6/ | 71 140 | μs |
| Analog input voltage range | VAIN | | 73. | 2.7 to 3.6 | $V_{\rm SS}$ | 500 | $V_{ m DD}$ | V |
| Analog port | IAINH | | VAIN=V _{DD} | 2.7 to 3.6 | (CO) | | 1 | |
| input current | IAINL | | VAIN=V _{SS} | 2.7 to 3.6 | -1 | | | μA |

- Conversion time calculation formula: $TCAD8 = (\frac{.2}{AD \text{ alivision ratio}} + 2) \times tCYC$

Note 6-1. The quantization error ($\pm 1/2$ LSB) is excluded from the absolute accuracy.

- Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.
 - The conversion time is twice the normal value when one of the following conditions occurs:
 - The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
 - The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

■ Consumption Current Characteristics at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

tvn · 3 3V

| Normal mode consumption current (Note 7-1) Vode | unit mA |
|--|------------|
| consumption current (Note 7-1) $ = V_{DD} 2 \\ = V_{DD} 3 \\ = V_{DD} 4 $ $ = V_{D$ | mA |
| mode FmX'tal=32.768 kHz crystal oscillator mode System clock set to 10 MHz Internal RC oscillation stopped 1/1 frequency division mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768 kHz crystal oscillator mode System clock set to internal RC oscillation 1/1 frequency division mode | mA |
| • FmX'tal=32.768 kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode | (|
| IDDOD (4) | |
| Internal RC oscillation stopped | μΑ |
| Continued on next | t page. |

Continued from preceding page.

| consumption current (Note 7-1) | Symbol DDHALT (1) DDHALT (2) | Pin/Remarks V _{DD} 1 =V _{DD} 2 =V _{DD} 3 =V _{DD} 4 | Conditions • HALT mode • FmCF=12 MHz ceramic oscillator mode • FmX'tal=32.768 kHz crystal oscillation mode • System clock set to 12 MHz • Internal RC oscillation stopped | V _{DD} [V] | min | 1.7 | max 3.5 | unit |
|--------------------------------------|---------------------------------------|--|---|---------------------|-----|-----|---------|------|
| consumption current (Note 7-1) | | =V _{DD} 2 =V _{DD} 3 | • FmCF=12 MHz ceramic oscillator mode • FmX'tal=32.768 kHz crystal oscillation mode • System clock set to 12 MHz | 3.0 to 3.6 | | 1.7 | 3.5 | |
| ID | DHALT (2) | 1 | • 1/1 frequency division mode | | | | | |
| | ייייייייייייייייייייייייייייייייייייי | | • HALT mode • FmCF=10 MHz ceramic oscillator mode • FmX'tal=32.768 kHz crystal oscillator mode • System clock set to 10 MHz • Internal RC oscillation stopped • 1/1 frequency division mode | 2.7 to 3.6 | | 1.5 | 3.2 | mA |
| ID | ODHALT (3) | | HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768 kHz crystal oscillator mode System clock set to internal RC oscillation 1/1 frequency division mode | · 27 to 3.6 | OP | 0.2 | 0.8 | 7 |
| ID | ODHALT (4) | -,(| • HALT mode • Fmc F=0Hz (oscillation stopped) • FmX'tal=32.768 kHz crystal escillator mode • System clock set to 32.768 kHz • internal RC oscillation stopped • 1/1 frequency division mode | 2.7 to 3.6 | OP | 8.5 | 65 | μА |

Continued from preceding page.

| | | Applicable | | | | Specifi | ication | |
|-----------------------|-------------|-------------|---|---------------------|-----|---------|---------|------|
| Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| HOLD mode consumption | IDDHOLD (1) | VDD1 | HOLD mode • CF1=V _{DD} or open | 2.7 to 3.6 | | 0.2 | 45 | |
| current | | | (external clock mode) | | | | | |
| | IDDHOLD (2) | | HOLD mode • CF1=V _{DD} or open (external clock mode) | 2.7 to 3.6 | | 1.2 | 48 | |
| | | | • LVD option selected | | | | | |
| HOLDX mode | IDDHOLD (3) | | HOLDX mode | | | | | |
| consumption | | | • CF1=V _{DD} or open | | | | | |
| current | | | (external clock mode) | 2.7 to 3.6 | | 4.6 | 60 | μΑ |
| | | | • FmX'tal=32.768 kHz crystal oscillator mode | | | | | |
| | IDDHOLD (4) | | HOLDX mode | | | | | |
| | | | • CF1=V _{DD} or open | | | | | .6 |
| | | | (external clock mode) | | | | | |
| | | | • FmX'tal=32.768 kHz crystal | 2.7 to 3.6 | | 5.6 | 63 | |
| | | | oscillator mode | | | | U. | |
| | | | • LVD option selected | | | | 7 | |

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

■ F-ROM Programming Characteristics at Ta= 40 to +85°C, VSS1=VSS2=VSS3=VSS4=6V

| | _ | | Applicable | | | 0/, | Specificat | tion | |
|----|-----------------------------|-----------|-------------|---|---------------------|-----|------------|------|------|
| | Parameter | Symbol | Pin/Remarks | Conditions | V _{DD} [V] | min | typ | max | unit |
| | Onboard programming current | IDDFW (1) | VDD | • Microcontroller erase current current is excluded | 2.7 to 3.6 | | | 10 | mA |
| | Onboard programming time | tFW (1) | | • 2K-byte erase operation | 2.7 to 3.6 | | | 25 | ms |
| • | time | tFW (2) | MO | *2-b/te programming operation | 2.7 to 3.6 | | | 45 | μs |
| | EV | CE P | EAG | 3ENII | | | | | |
| TH | SOL | RE | PK | | | | | | |

■ Power-on Reset (POR) Characteristics at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

| | | | | | | Specif | ication | |
|--------------------------------|--------|-------------|---|-------------------------|------|--------|---------|------|
| Parameter | Symbol | Pin/Remarks | Conditions | Option selected voltage | min | typ | max | unit |
| Por release | PORRL | | • Select from option. | 2.57V | 2.47 | 2.57 | 2.72 | |
| voltage | | | (Note 8-1) | 2.87V | 2.77 | 2.87 | 3.02 | |
| Detction voltage unknown state | POUKS | | • See Fig10. (Note 8-2) | | | 0.7 | 0.95 | V |
| Power supply rise time | PORIS | | • Power supply rise time from 0V to 1.6V. | | | | 100 | ms |

Note8-1: The POR release level can be selected out of 2 levels only when the LVD reset function is disabled.

Note8-2: POR is in an unknown state before transistors start operation.

■ Low Voltage Detection Reset (LVD) Characteristics at Ta=40 to +85°C

VSS1=VSS2=VSS3=VSS4=0V

| - 00 - 00 | - DD - DD | | | | | | | |
|-----------------|-----------|-------------|---|-----------------|--------------|---------|--------|------|
| | | | | | | Specifi | cation | 5 |
| Parameter | Symbol | Pin/Remarks | Conditions | Option selected | min | typ | max | unit |
| | | | | voltage | | JP | nux | unit |
| LVD reset | LVDET | | Select from option. | | | 115 | . 7 | |
| voltage | | | (Note 9-2) | 2.81V | 2.71 | 2.81 | 2.96 | V |
| (Note 9-2) | | | • See Fig. 11. | | | | | |
| LVD hysteresis | LVHYS | | | | \mathbf{O} | | 7 | 7 |
| width | | | | 2.81V | G | 60 | | mV |
| Detection | LVUKS | | • See Fig. 11. | | 0/1/ | 70 | | |
| voltage unknown | | | (Note 9-3) | NV .Q | | 6.0 | 0.95 | V |
| state | | | 1/2 | | | | | |
| Low voltage | TLVDW | | •LVDET-0.5V | 10,4 | | | | |
| detection | | | • See Fig. 12. | 11/1 | | | | |
| minimum width | | | | -2" | 0.2 | | | mS |
| (Replay | | | 250 1 | | | | | |
| sensitivity) | | | K | | | | | |

Note9-1: LVD reset voltage specification values do not include hysteresis voltage.

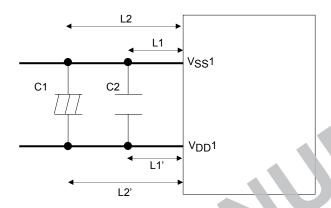
Note⁹ 2: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note9-3: LVD is in an unknown state before transistors start operation.

■ Power Pin Treatment Conditions 1 (Vpp1, Vss1)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

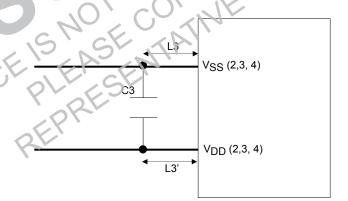
- Connect among the V_{DD}1 and V_{SS}1 pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately $0.1~\mu F$ or larger.
- The $V_{\text{DD}}\mathbf{1}$ and $V_{\text{SS}}\mathbf{1}$ traces must be thicker than the other traces.



■ Power Pin Treatment Conditions 2 (V_{DD}(2, 3, 4), V_{SS}(2, 3, 4))

Connect capacitors that meet the following condition between the VDD(2, 3, 4) and VSS(2, 3, 4) pins:

- Connect among the $V_{DD}(2, 3, 4)$ and $V_{SS}(2, 3, 4)$ pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The $V_{DD}(2, 3, 4)$ and $V_{SS}(2, 3, 4)$ traces must be thicker than the other traces.



■ Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

| Nominal | | | | Circuit Constant | | | | Oscill Stabilizat | lation ion Time | |
|-----------|-----------------------|-----------------|------------|------------------|-----------|------------|--------------|----------------------|--------------------|------------------------|
| Frequency | Vendor Name Resonator | | C3 [pF] | C4 [pF] | Rf [Ω] | Rd2 [Ω] | Range [V] | Typ [ms] | max [ms] | Remarks |
| 12 MHz | | CSTCE12M0G52-R0 | (10) | (10) | OPEN | 330 | 2.2 to 3.6 | 0.02 | 0.2 | C1, C2 integrated type |
| 10.141 | MURATA | CSTCE10M0G52-R0 | (10) | (10) | OPEN | 680 | 2.2 to 2.6 | 0.02 | 0.2 | C1, C2 integrated type |
| 10 MHz | | CSTLS10M0G53-B0 | (15) | (15) | OPEN | 680 | 2.2 to 3.6 | 0.02 | 0.2 | C1, C2 integrated type |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the lower limit level of the operating voltage range (see Figure 4)

■ Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation capuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

| Nominal | | ъ. | | Circuit | Constan | ı | Operating Voltage | | lation tion Time | 0. |
|------------|------------------|--------------------|------------|---------|------------|------------|-------------------|-----------------|---------------------|----------|
| Frequency | Vendor Name | dor Name Resonator | C3 [pF] | C4 [pF] | Rf2 [Ω] | Rd2 [Ω] | Range [V] | typ max [s] [s] | Remarks | |
| 32.768 kHz | EPSON TOYOCOM | MC-306 | 10 | 10 | Open | 330K | 2.2 to 3.6 | 1.0 | 3.0 | CL=7.0pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note: The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

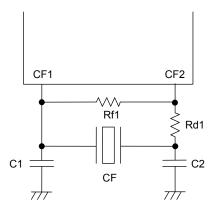


Figure 1 CF oscillator circuit

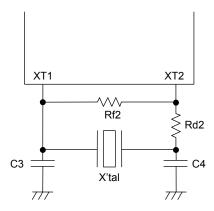
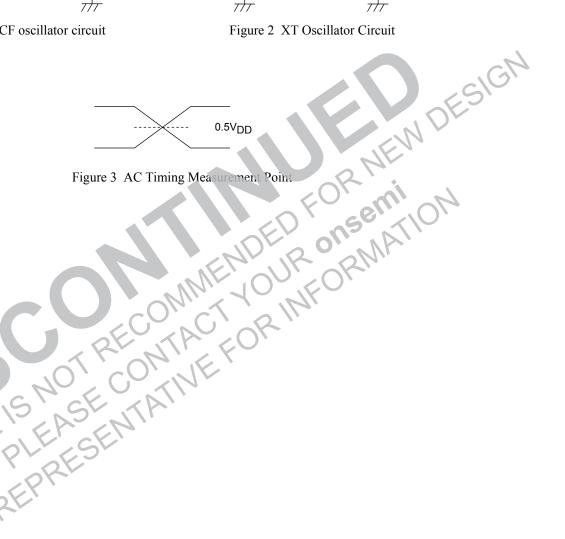
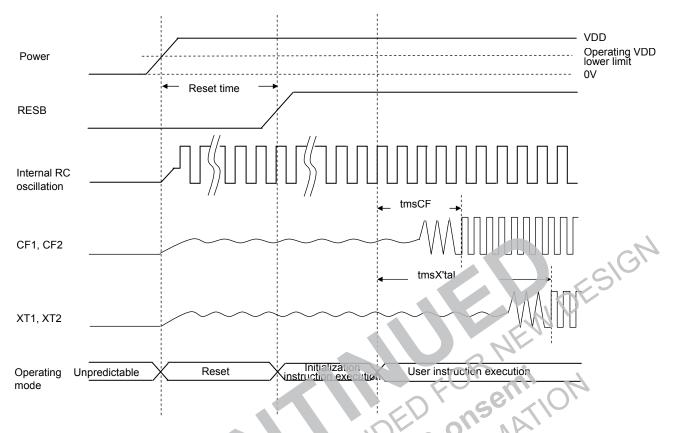
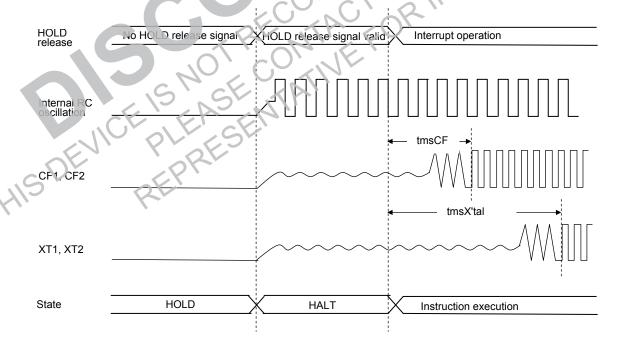


Figure 2 XT Oscillator Circuit



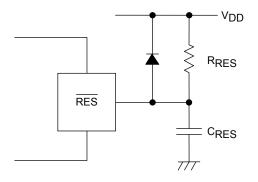


Reset Time and Oscillation Stabilization Time



HOLD Release and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time Timing Charts

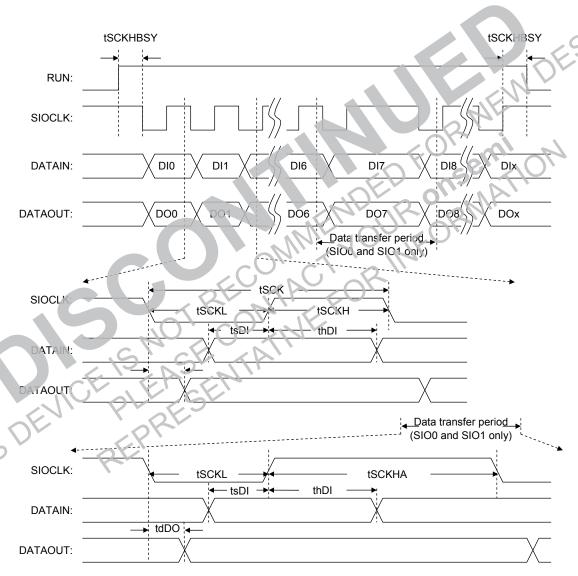


Note:

Reset signal must be present when power supply rises.

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10 μs after the supply voltage gets stabilized.

Figure 5 Reset Circuit



^{*} Remarks: DIx and DOx denote the last bits communicated; x=0 to 32768

Figure 6 Serial I/O Waveforms

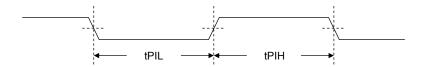
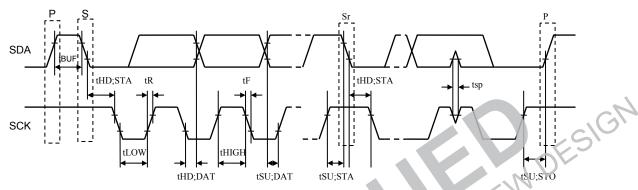


Figure 7 Pulse Input Timing Signal Waveform



S: Start condition

P: Stop condition

Sir: Restart condition

Figure 8 I²C Timing

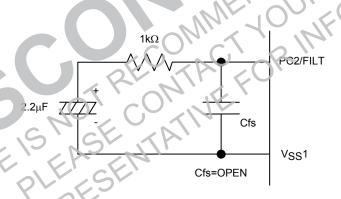


Figure 9 Recommended FILT Circuit

* Take at least 50ms to oscillation to stabilize after PLL is started.

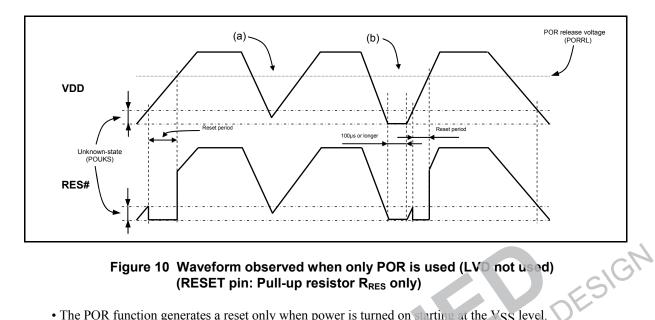


Figure 10 Waveform observed when only POR is used (LVD not used) (RESET pin: Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100 us or longer.

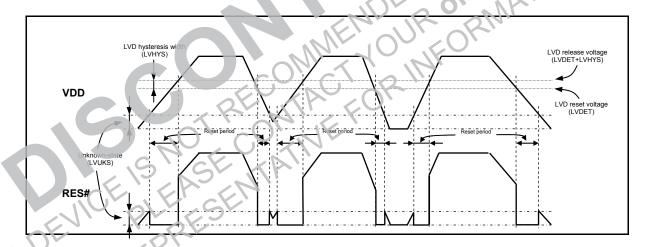


Figure 14 Waveform observed when both POR and LVD functions are used (RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

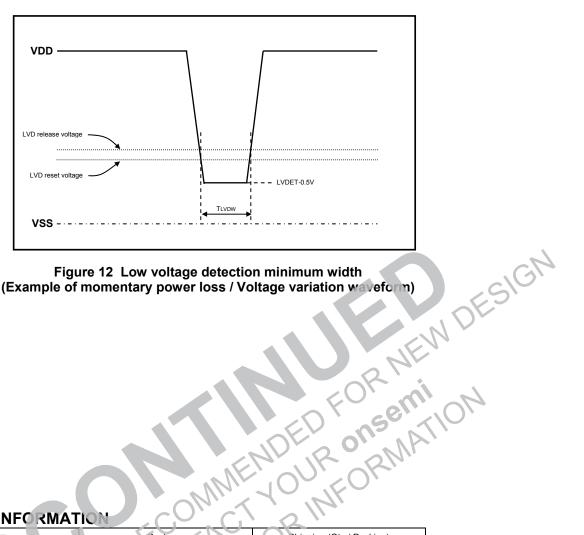


Figure 12 Low voltage detection minimum width (Example of momentary power loss / Voltage variation waveform)

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|------------------|---------------------------|--------------------------|
| LC88FC2F0BUTJ-2H | (Pb-Free / Halogen Free) | 900 / Tray JEDEC |
| THIS DEVICE PLE | ASENTATIVE RESENTATIVE | |

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