ON Semiconductor

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- Base timer
  - <1> Clock may be selected from OSC0 (32.768 kHz crystal oscillator) and frequency-divided output of system clock.
  - <2> Interrupts can be generated in 7 timing schemes.

■ Real time clock

- <1> Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leapyear calculation function.
- <2> Consisted of Indipendent second-minuit-hour-day-month-yeare-century counters.

■ Serial interfaces

- SIO0 : 8-bit synchronous SIO
  - <1> LSB first/MSB first mode selectable
  - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
  - <6> Wakeup function
- SIO1 : 8-bit synchronous SIO
  - <1> LSB first/MSB first mode selectable
  - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
  - <6> Wakeup function
- SIO4 : 8-bit synchronous SIO
  - <1> LSB first/MSB first mode selectable
  - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
  - <6> Wakeup function
- SMIIC0 : Single master I^2C/8-bit synchronous SIO
  - Mode 0 : Single-master mode communication
  - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
- SMIIC1 : Single master I^2C/8-bit synchronous SIO
  - Mode 0 : Single-master mode communication
  - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
- SLIIC0 : Slave I^2C/8-bit synchronous SIO
  - Mode 0 : I^2C slave mode communication
  - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
    - Note: usable only with the external clock source

- UART0
  - <1> Data length : 8 bits (LSB first)
  - <2> Start bits : 1 bit
  - <3> Stop bits : 1 bit
  - <4> Parity bits : None/even parity/odd parity
  - <5> Transfer rate : 4/8 cycle
  - <6> Baudrate source clock : P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer4 cycle.
  - <7> Full duplex communication

  Note : The "cycle" refers to one period of the baudrate clock source.

- UART2
  - <1> Data length : 8 bits (LSB first)
  - <2> Start bits : 1 bit
  - <3> Stop bits : 1/2 bit
  - <4> Parity bits : None/even parity/odd parity
  - <5> Transfer rate : 8 to 4096 cycle
  - <6> Baudrate source clock : System clock/OSC0/OSC1/P26 input signal
  - <7> Wakeup function
  - <8> Full duplex communication

  Note : The "cycle" refers to one period of the baudrate clock source.

- UART3
  - <1> Data length : 8 bits (LSB first)
  - <2> Start bits : 1 bit
  - <3> Stop bits : 1/2 bit
  - <4> Parity bits : None/even parity/odd parity
  - <5> Transfer rate : 8 to 4096 cycle
  - <6> Baudrate source clock : System clock/OSC0/OSC1/P36 input signal
  - <7> Wakeup function
  - <8> Full duplex communication

  Note : The "cycle" refers to one period of the baudrate clock source.

■ AD converter

- <1> 12/8 bits resolution selectable
- <2> Analog input : 16 channels
- <3> Comparator mode

■ PWM

- PWM0 : Multifrequency 12-bit PWM × 2 channels (PWM0A and PWM0B)
  - <1> 2-channel pairs controlled independently of one another
  - <2> Clock source selectable from system clock or OSC1
  - <3> 8-bit prescaler : TPWMR0= (prescaler value + 1) × clock period
  - <4> 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
  - <5> Fundamental wave PWM mode
    - Fundamental wave period : 16 TPWMR0 to 256 TPWMR0
    - High pulse width : 0 to (Fundamental wave period - TPWMR0)
  - <6> Fundamental wave + additional pulse mode
    - Fundamental wave period : 16 TPWMR0 to 256 TPWMR0
    - Overall period : Fundamental wave period × 16
    - High pulse width : 0 to (Fundamental wave period - TPWMR0)

■ CRC operating circuit

■ Watchdog timer

- <1> Driven by the base timer + internal watchdog timer dedicated counter
- <2> Interrupt or reset mode selectable

■ Infrared Remote Controller Receiver Circuit

1) Noise rejection function (noise filter time constant: Approx. 120 μs when the 32.768 kHz crystal oscillator is selected as the reference clock source)
2) Supports data encording systems such as PPM (Pulse Position Modulation) and Manchester encording
3) X'tal HOLD mode release function

■ Internal Reset Function

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level can be selected by option configuration.

■ Interrupts (peripheral function))

- 61 sources (33 modules), 14 vector addresses

<1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.

<2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Module
1	08000H	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer 0 (2)
4	0800CH	INT0 (1)
5	08014H	INT1 (1)
6	08018H	INT2 (1) / timer 1 (2) / UART2 (4)
7	0801CH	INT3 (1) / timer 2 (4) / SMIIC0 (1) / SLIIC1 (1)
8	08020H	INT4 (1) / timer 3 (2) / Infared remote control receiver (4)
9	08024H	INT5 (1) / timer 4 (1) / SIO1 (2)
10	0802CH	PWM0 (1) / SMIIC1 (1)
11	08030H	ADC (1) / timer 5 (1) / SIO4 (2)
12	08034H	INT6 (1) / timer 6 (1) / UART 3 (4)
13	08038H	INT7 (1) / SIO0 (2) / SIO0(2)
14	0803CH	Port 0 (3) / Port 5 (8) / RTC (1) / CRC (1)

- 3 priority levels selectable
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

■ Subroutine stack : RAM area

- Subroutine calls that automatically save PSW, interrupt vector calls : 6 bytes
- Subroutine calls that do not automatically save PSW : 4 bytes

■ Multiplication/division instructions

- 16 bits × 16 bits (4 tCYC execution time)
- 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
- 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

■ Oscillator circuits

- RC oscillator circuit (internal) : For system clock
- CF oscillator circuit (built-in Rf circuit) : For system clock(OSC1)
- Crystal oscillator circuit (built-in Rf circuit) : For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal) : For system clock (In the case of exception processing)
- VCO oscillator circuit : For timer3,4,5,6,7 clock

■ System clock divider function

- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

■ Standby function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
  <1> Oscillation is not stopped automatically.
  <2> Released by a system reset or occurrence of an interrupt.
- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
  <1> OSC1, RC, and OSC0 oscillations automatically stop.
  <2> There are six ways of releasing the HOLD mode:
  (1) Setting the reset pin to the low level
  (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
  (3) Having an interrupt source established at port 0
  (4) Having an interrupt source established at port 5
  (5) Having an interrupt established at SIO0, SIO1 or SIO4
  (6) Having an interrupt established at UART2 or UART3
- HOLDX mode : Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
  <1> OSC1 and RC oscillations automatically stop.
  <2> OSC0 maintains the state that is established when the HOLDX mode is entered.
  <3> There are nine ways of releasing the HOLDX mode.
  (1) Setting the reset pin to the low level
  (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6,and INT7 pins to the specified level
  (3) Having an interrupt source established at port 0
  (4) Having an interrupt source established at port 5
  (5) Having an interrupt source established at the base timer circuit
  (6) Having an interrupt established at SIO0, SIO1 or SIO4
  (7) Having an interrupt established at UART2 or UART3
  (8) Having an interrupt established at Infared remote control receiver.
  (9) Having an interrupt source established at the real time clock circuit

■ On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

■ Package form

- TQFP100 (14 × 14) : Pb-Free and Halogen Free type

■ Development tools

- On-chip debugger: EOCUIF1 or EOCUIF2 + LC88FC2H0A

■ Programming board

Package	Programming Board
TQFP100 (14 × 14)	W88F52TQ

■ Flash ROM Programmer

Maker		Model	Supported Version	Device
Flash Support Group Company (FSG)	Single programmer	AF9709C		
	Gang programmer	AF9723/AF9723B(Main body) (Include Ando Electric Co.,Ltd. models		
		AF9833(Unit) (Include Ando Electric Co.,Ltd. Models)		
Flash Support Group Company (FSG) + ON Semiconductor (Note 1)	On-board Single / Gang programmer	AF9101/AF9103(Main budy) (FSG models)	(Note 2)	LC88FC2H0A
		SIB88 Type A (Interface driver) (ON Semiconductor model)		
ON Semiconductor	Single / Gang programmer	SKK Type C (SanyoFWS)	Application Version After 1.08 Chip Data Version After 2.46	LC88FC2H0A
	On-board Single programmer	FWS-X16DI Type 2	Application Version After 1.08 Chip Data Version After 2.45	LC88FC2H0A

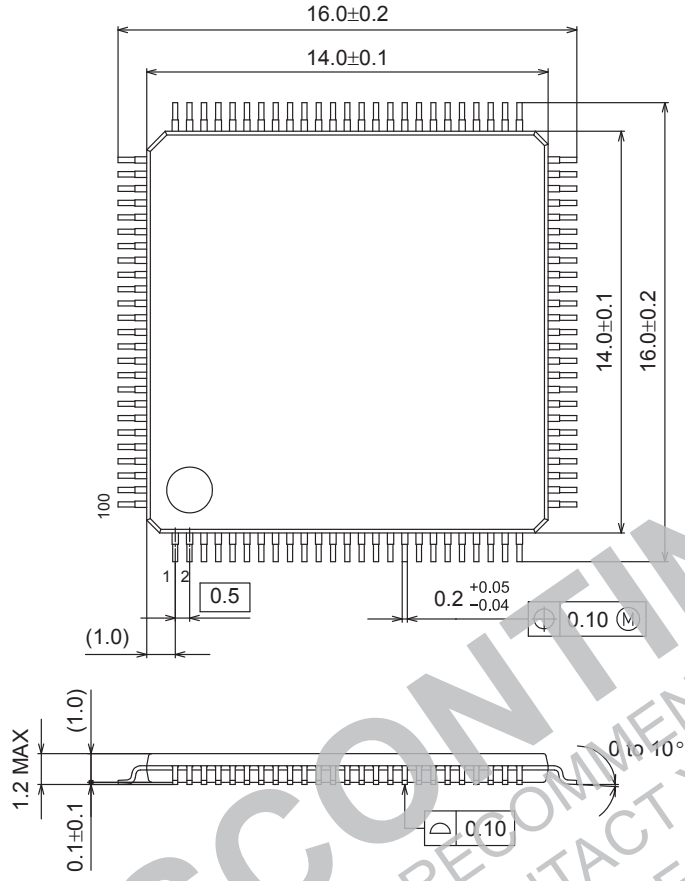
For information about AF-Series :
Flash Support Group Company (TOA ELECTRONICS, Inc.)
TEL : +81-53-459-1050
E-mail : sales@j-fsg.co.jp

Note1 : On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from our company (SIB88-TypeA) together can give a PC-less, standalone on-board-programming capabilities.
Note2 : It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

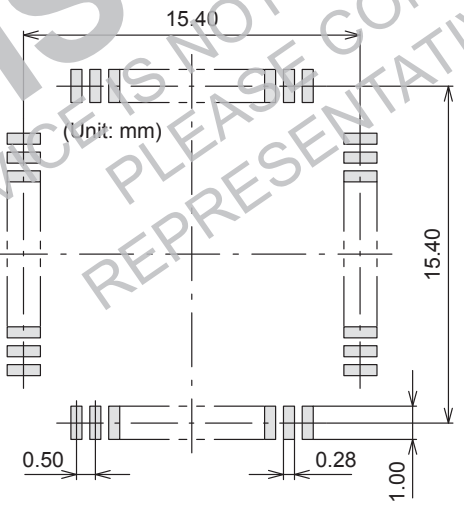
Package Dimensions

unit : mm

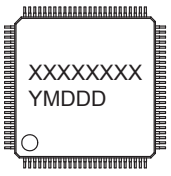
TQFP100 14x14 / TQFP100
CASE 932AY
ISSUE A



SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



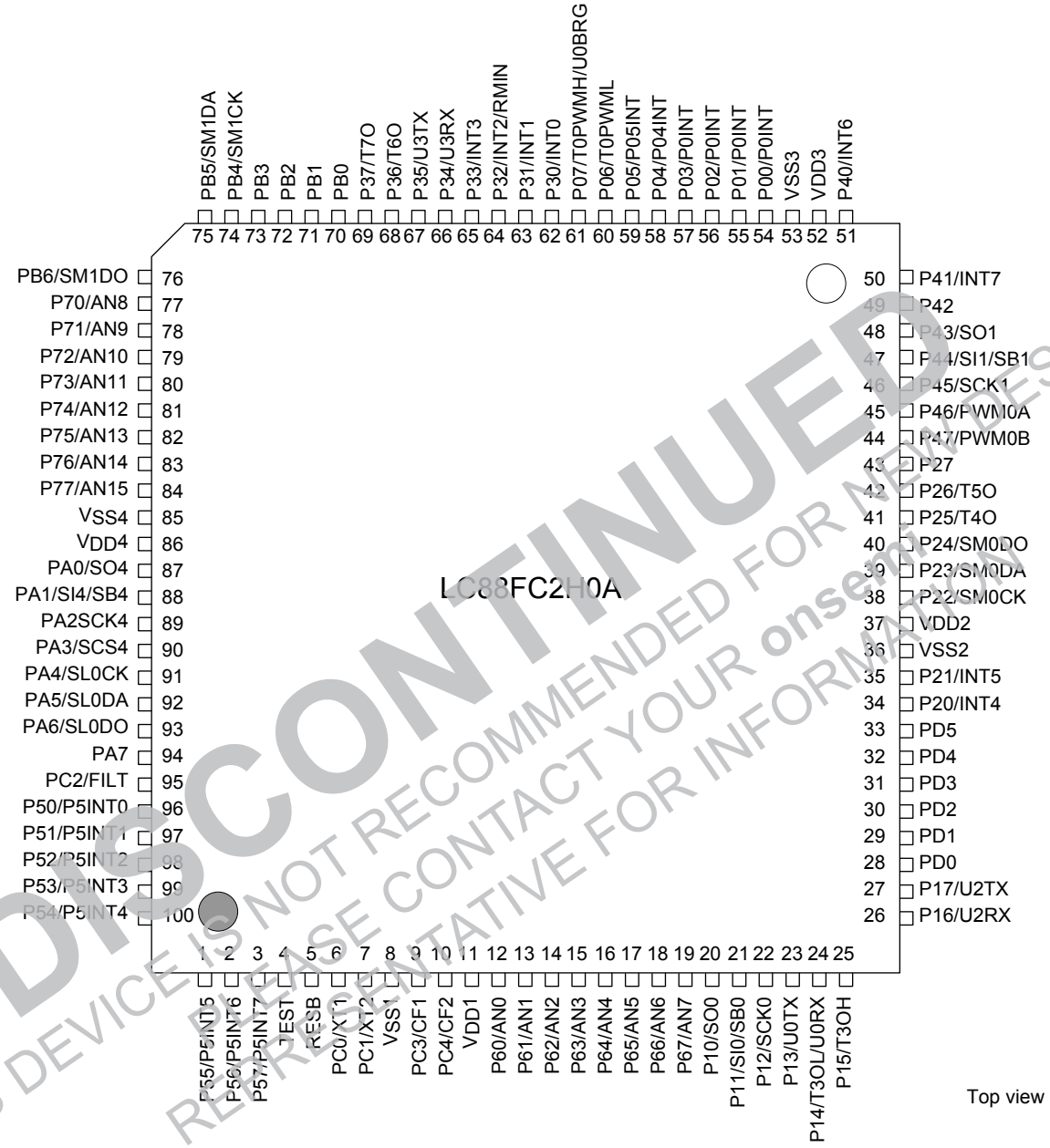
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pinout



Top view

TQFP100 (14×14) (Pb-Free and Halogen free type)