Continued from preceding page.

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
HOLD mode consumption current	IDDHOLD (1)	V_{DD}1	HOLD mode ・CF1=VDD or open (external clock mode)	2.7 to 3.6		0.2	50	μA
	IDDHOLD (2)		HOLD mode ・CF1=VDD or open (external clock mode) ・LVD option selected	2.7 to 3.6		1.2	53	
HOLDX mode consumption current	IDDHOLD (3)		HOLDX mode ・CF1=VDD or open (external clock mode) ・FmX'tal=32.768 kHz crystal oscillator mode	2.7 to 3.6		4.6	71	
	IDDHOLD (4)		HOLDX mode ・CF1=VDD or open (external clock mode) ・FmX'tal=32.768 kHz crystal oscillator mode ・LVD option selected	2.7 to 3.6		5.6	74	

Note 7-1 : The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

■ **F-ROM Programming Characteristics** at Ta=+10 to +55°C, V_{SS1}=V_{SS2}=V_{SS3}=V_{SS4}=0V

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW (1)	V_{DD}1	・Microcontroller core current is excluded.	2.7 to 3.6			10	mA
Onboard programming time	tFW (1)		・2 page erase operation	2.7 to 3.6			25	ms
	tFW (2)		・2 byte programming operation	2.7 to 3.6			45	μs

■ Power-on Reset (POR) Characteristics at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				Option selected voltage	min	typ	max	unit
Por release voltage	PORRL		・Select from option. (Note 8-1)	2.57V	2.47	2.57	2.72	V
				2.87V	2.77	2.87	3.02	
Detction voltage unknown state	POUKS		・See Fig 10. (Note 8-2)			0.7	0.95	
Power supply rise time	PORIS		・Power supply rise time from 0V to 1.6V.				100	ms

Note8-1 : The POR release level can be selected out of 2 levels only when the LVD reset function is disabled.
Note8-2 : POR is in an unknown state before transistors start operation.

■ Low Voltage Detection Reset (LVD) Characteristics

at Ta=–40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

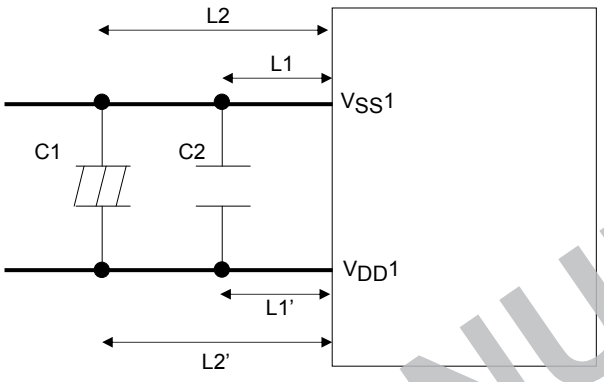
Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				Option selected voltage	min	typ	max	unit
LVD reset voltage (Note 9-1)	LVDET		・Select from option. (Note 9-2) ・See Fig 11.	2.81V	2.71	2.81	2.96	V
LVD hysteresis width	LVHYS			2.81V		60		mV
Detection voltage unknown state	LVUKS		・See Fig 11. (Note 9-3)			0.7	0.95	V
Low voltage detection minimum width (Replay sensitivity)	TLVDW		・LVDET-0.5V ・See Fig 12.		0.2			ms

Note9-1 : LVD reset voltage specification values do not include hysteresis voltage.
Note9-2 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.
Note9-3 : LVD is in an unknown state before transistors start operation.

■ Power Pin Treatment Conditions 1 ($V_{DD}1$, $V_{SS}1$)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins :

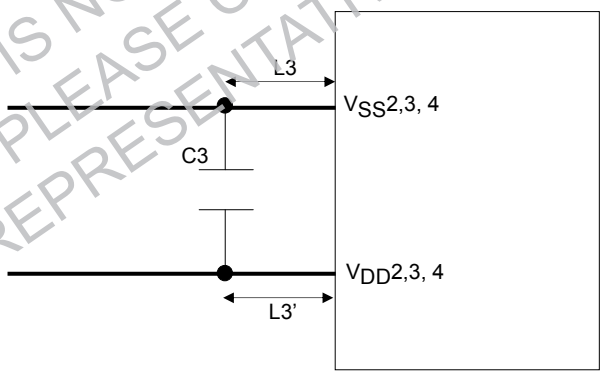
- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
  The capacitance of C2 should be approximately 0.1μF or larger.
- The $V_{DD}1$ and $V_{SS}1$ traces must be thicker than the other traces.



■ Power Pin Treatment Conditions 2 ($V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4)

Connect capacitors that meet the following condition between the $V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4 pins :

- Connect among the $V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4 pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1μF or larger.
- The $V_{DD}2$, 3, 4 and $V_{SS}2$, 3, 4 traces must be thicker than the other traces.



■ Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
10 MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	OPEN	680	2.2 to 2.6	0.02	0.2	C1, C2 integrated type
		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4)

■ Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768 kHz	EPSON TOYOCOM	MC-306	10	10	Open	330K	2.2 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note : The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

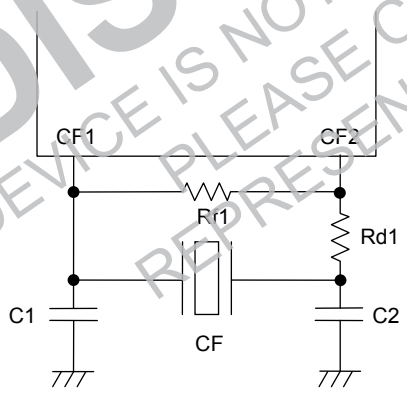


Figure 1. CF oscillator circuit

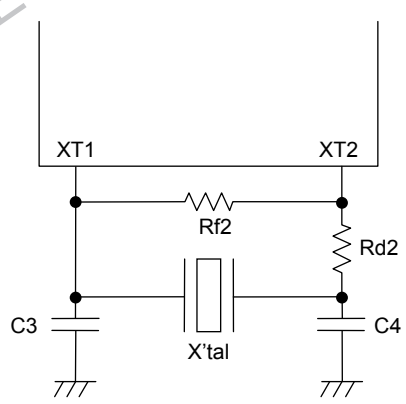


Figure 2. XT Oscillator Circuit

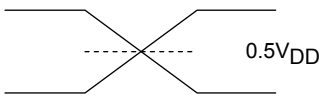
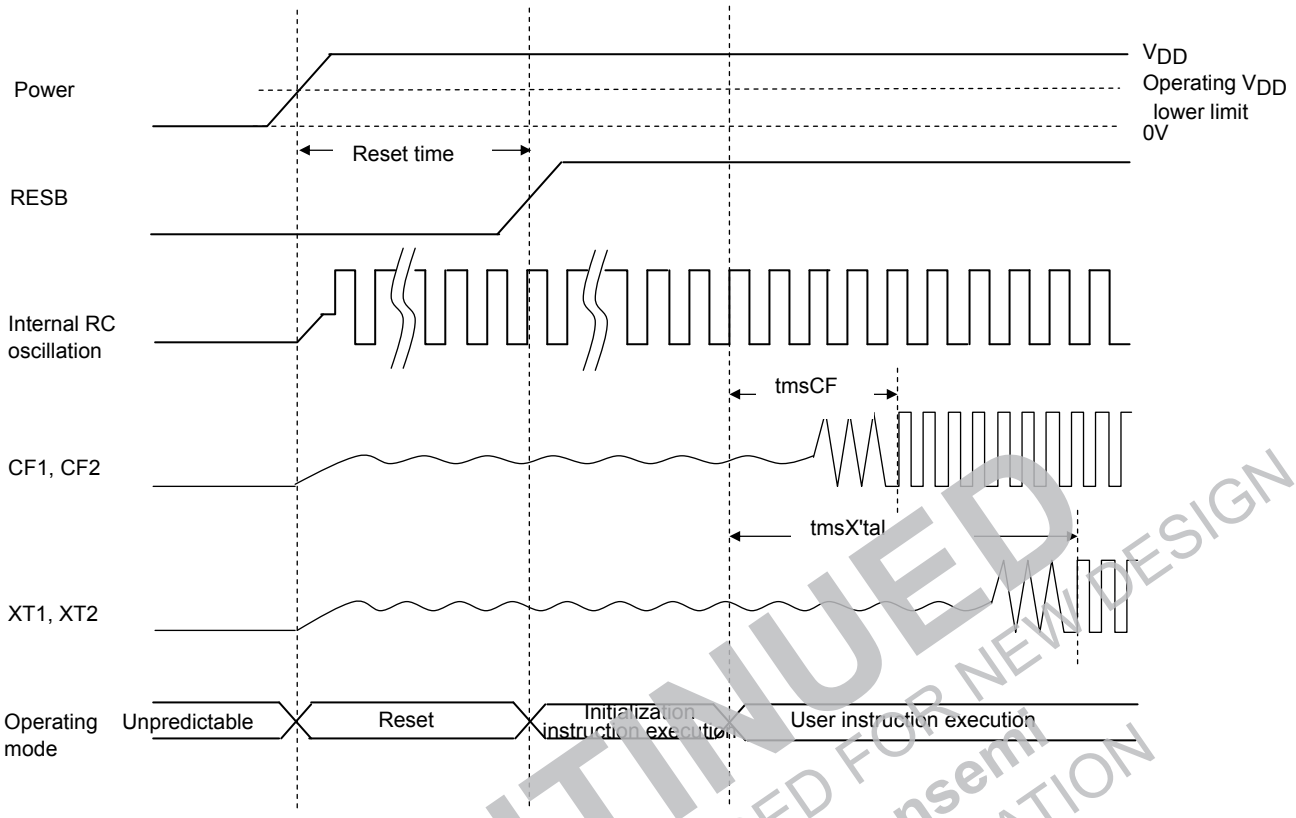
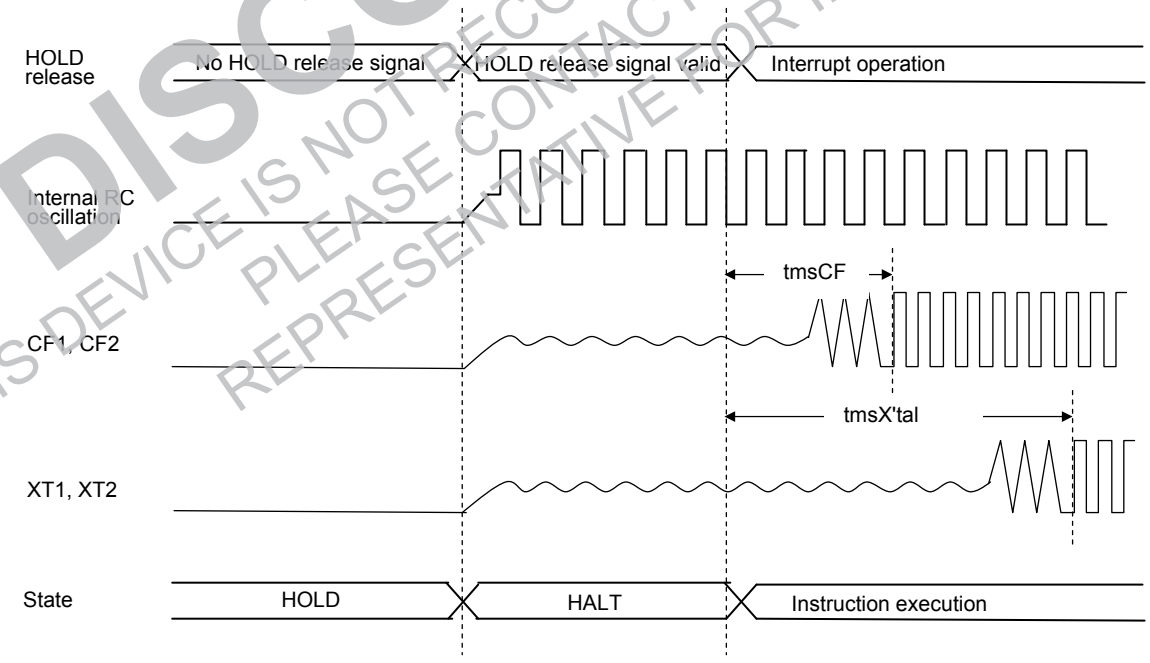


Figure 3. AC Timing Measurement Point

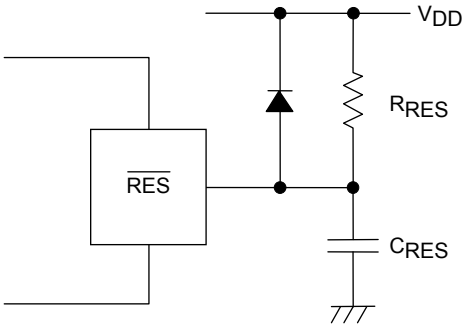


Reset Time and Oscillation Stabilization Time



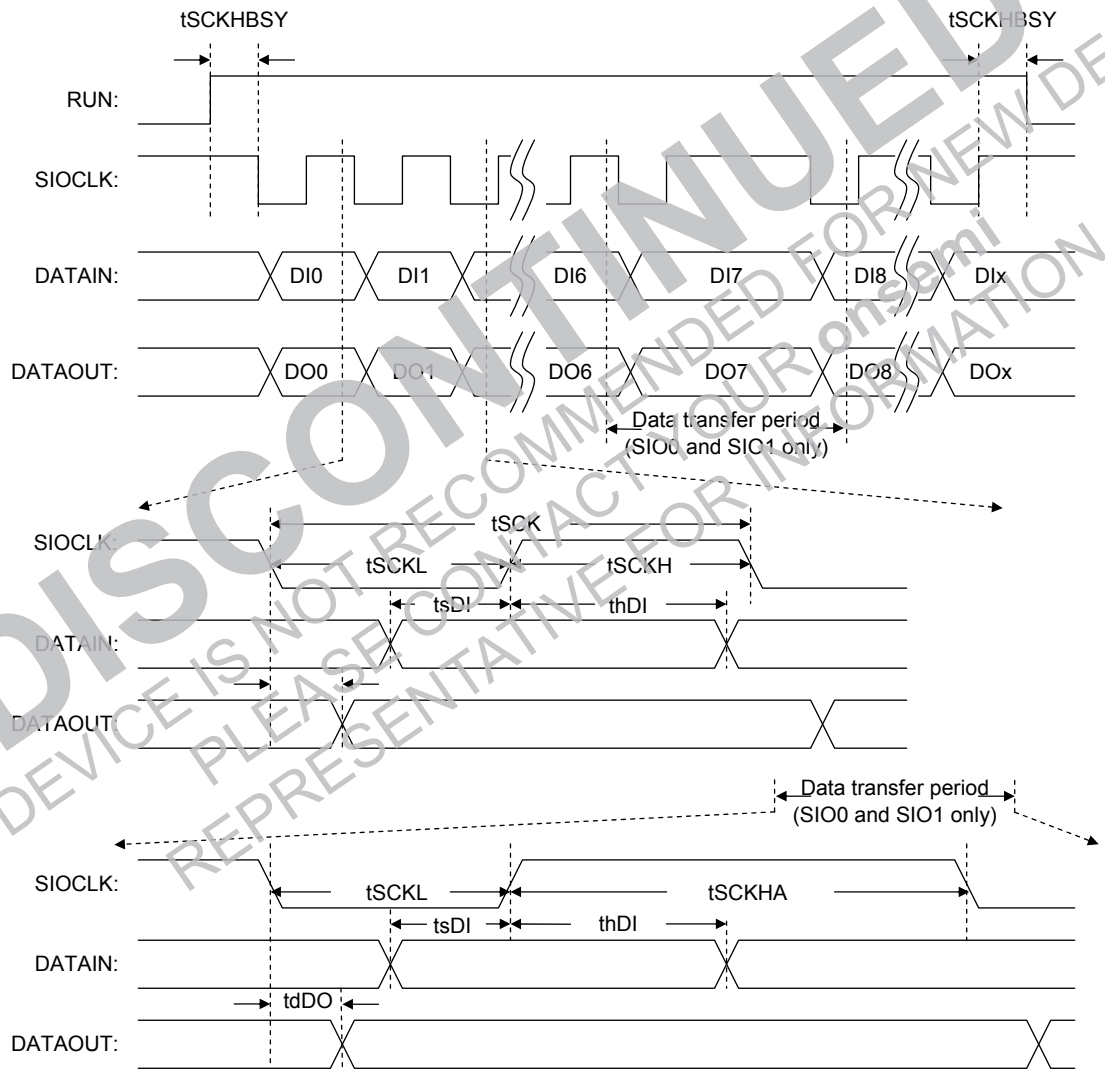
HOLD Release and Oscillation Stabilization Time

Figure 4. Oscillation Stabilization Time Timing Charts



Note :
Reset signal must be present when power supply rises.
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10 μs after the supply voltage gets stabilized.

Figure 5. Reset Circuit



* Remarks: DIx and DOx denote the last bits communicated; x=0 to 32768

Figure 6. Serial I/O Waveforms

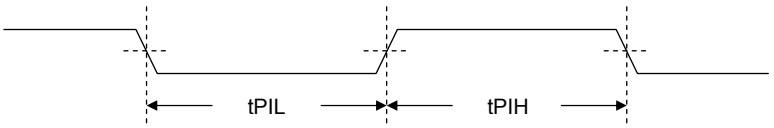
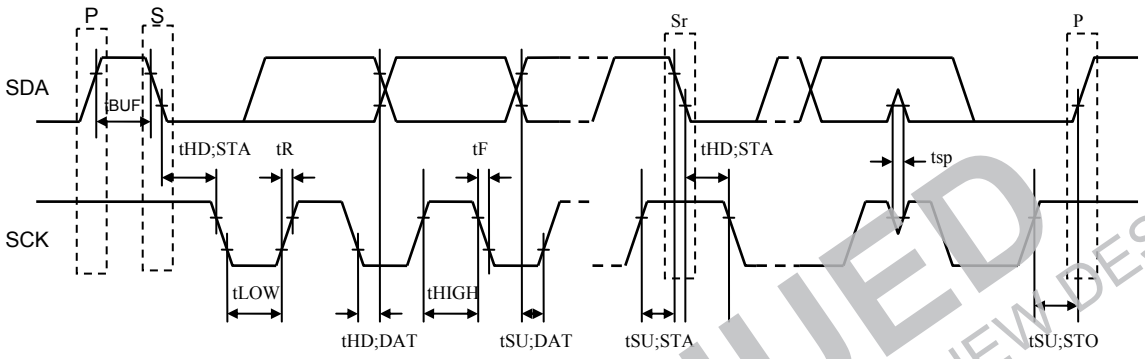


Figure 7. Pulse Input Timing Signal Waveform



S : Start condition
P : Stop condition
Sir : Restart condition

Figure 8. I^2C Timing

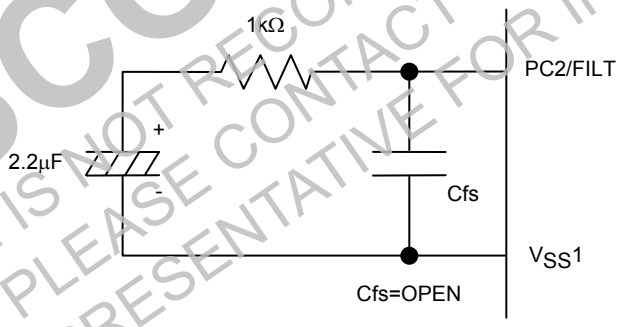


Figure 9. Recommended FILT Circuit

* Take at least 50ms to oscillation to stabilize after PLL is started.

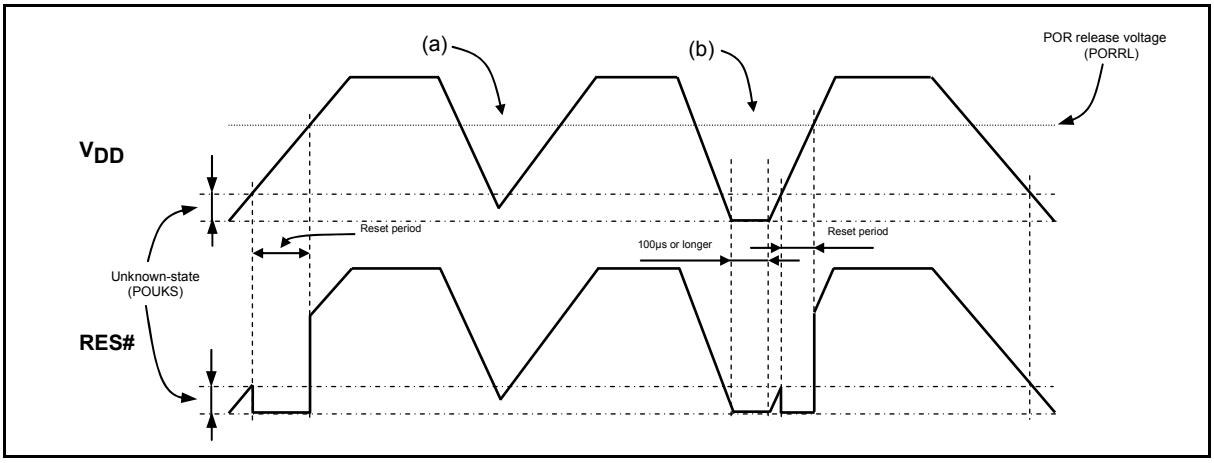


Figure 10. Waveform observed when only POR is used (LVD not used)
(RESET pin : Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

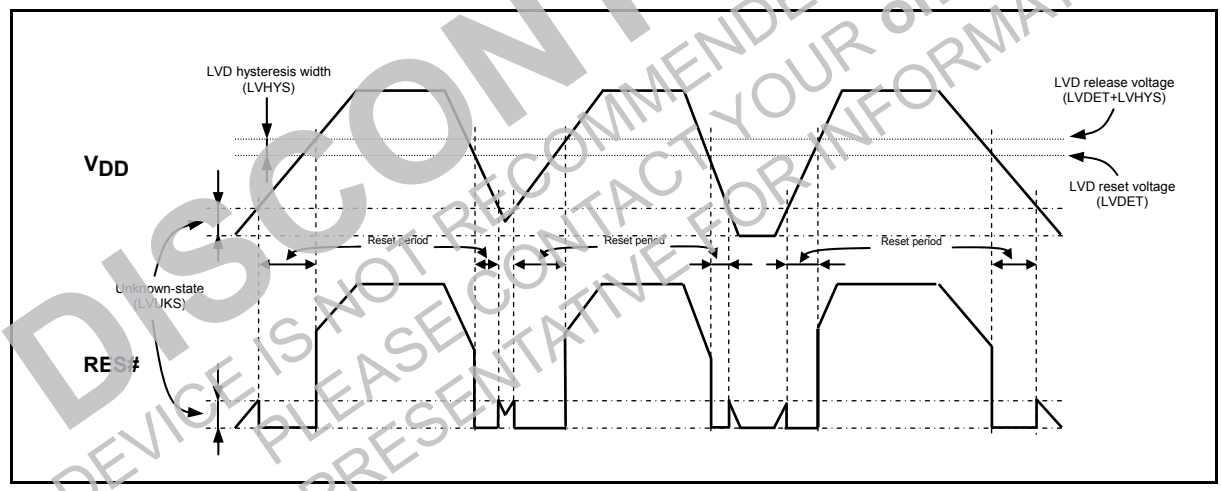


Figure 11. Waveform observed when both POR and LVD functions are used
(RESET pin : Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

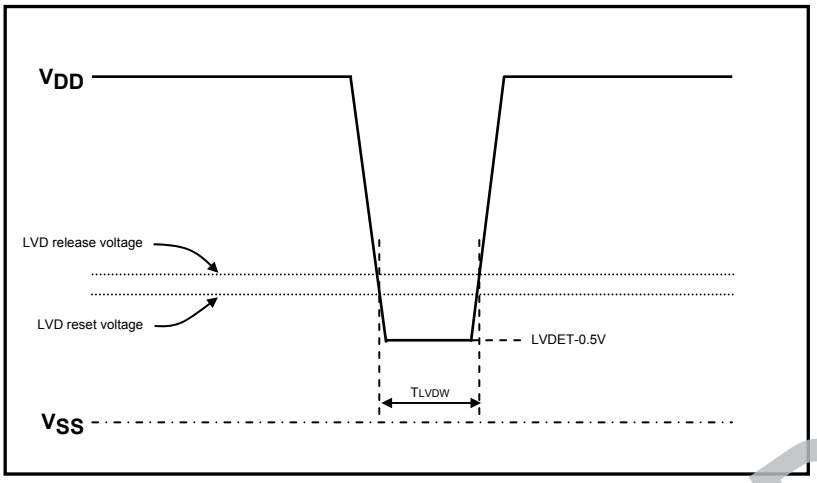


Figure 12. Low voltage detection minimum width
(Example of momentary power loss / Voltage variation waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC88FC3H0AUTJ-2H	TQFP 100 14x14 (Pb-Free / Halogen Free)	900 / Tray JEDEC