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LE25U20AFD

Serial Flash Memory
2 Mb (256K x 8)

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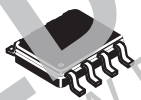


VSOIC8 NB

Overview

The LE25U20AFD is a serial interface-compatible flash memory device with a 256K × 8-bit configuration. It uses a single 2.5 V power supply. While making the most of the features inherent to a serial flash memory device, the LE25U20AFD is housed in an 8-pin ultra-miniature package. These features make this device ideally suited to storing program codes in applications such as portable information devices, which are required to have increasingly more compact dimensions. Moreover, by using the small sector erase function this product is also suitable for the parameter or the date storage usage with comparatively little rewriting times that becomes a capacity shortage in EEPROM.

Features

- Read / write operations enabled by single 2.5 V power supply :
  2.30 to 3.60 V supply voltage range
- Operating frequency : 30 MHz
- Temperature range : –40 to +85°C
- Serial interface : SPI mode 0, mode 3 supported
- Sector size : 4K bytes/small sector, 64K bytes/sector
- Small sector erase, sector erase, chip erase functions
- Page program function (256 bytes / page)
- Block protect function
- Status functions : Ready/busy information, protect information
- Highly reliable read/write
  Number of rewrite times : 100,000 times
  Small sector erase time : 40 ms (typ), 150 ms (max)
  Sector erase time : 80 ms (typ), 250 ms (max)
  Chip erase time : 250 ms (typ), 1.6 s (max)
  Page program time : 4.0 ms / 256 bytes (typ), 5.0 ms / 256 bytes (max)
- Data retention period : 20 years
- Package : VSOIC8 NB

* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION

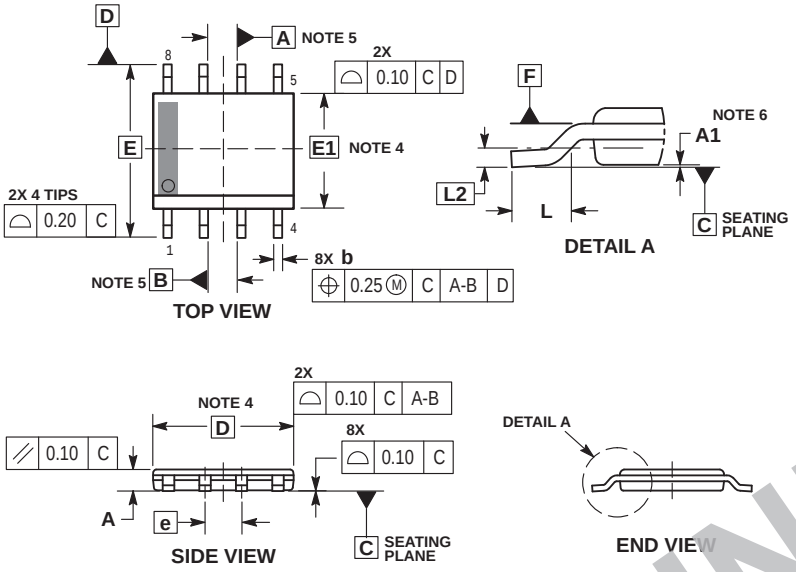
See detailed ordering and shipping information on page 21 of this data sheet.

May 2024 - Rev. 1
Publication Order Number :
LE25U20AFD/D

Package Dimensions

unit : mm

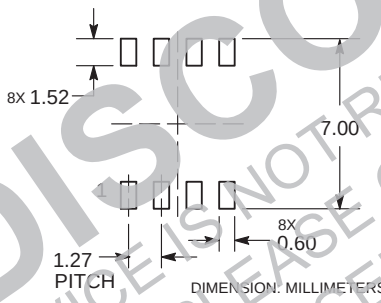
VSOIC8 NB
CASE 753AA
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

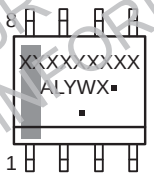
DIM	MILLIMETERS MIN	MAX
A	0.65	0.85
A1	---	0.05
b	0.31	0.51
c	0.17	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

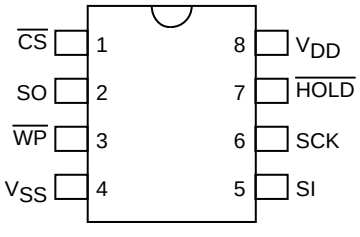


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G”, may or not be present.

Figure 1 Pin Assignments



Top view

Figure 2 Block Diagram

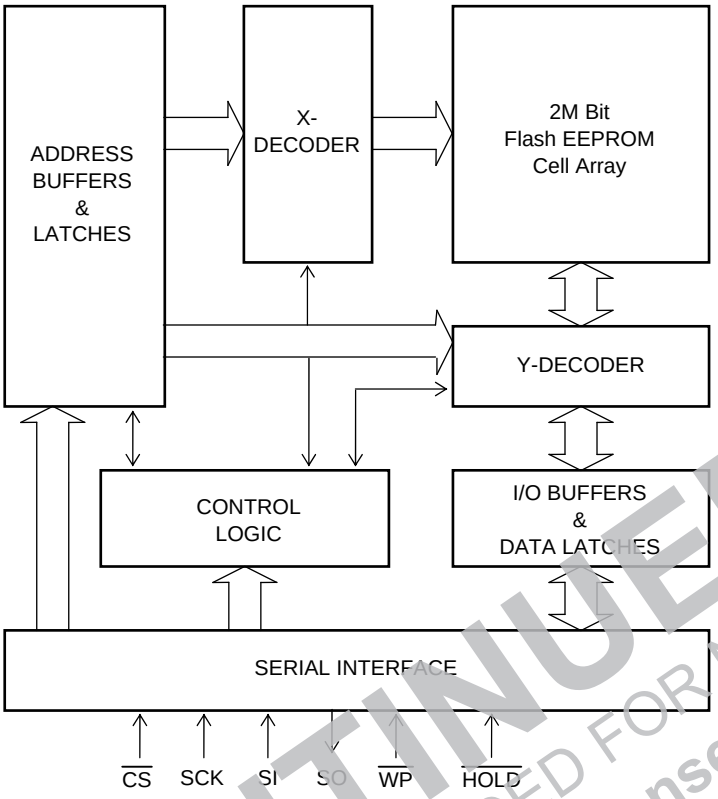


Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI	Serial data input	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock.
SO	Serial data output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock.
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$	Write protect	The status register write protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{HOLD}$	Hold	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power supply	This pin supplies the 2.30 to 3.60 V supply voltage.
V_{SS}	Ground	This pin supplies the 0 V supply voltage.

Device Operation

The LE25U20AFD features electrical on-chip erase functions using a single 2.5 V power supply, that have been added to the EPROM functions of the industry standard that support serial interfaces. Interfacing and control are facilitated by incorporating the command registers inside the chip. The read, erase, program and other required functions of the device are executed through the command registers. The command addresses and data input in accordance with "Table 2 Command Settings" are latched inside the device in order to execute the required operations. "Figure 3 Serial Input Timing" shows the timing waveforms of the serial data input. First, at the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are introduced internally in sequence starting with bit 7 in synchronization with the rising SCK edge. At this time, output pin SO is in the high-impedance state. The output pin is placed in the low-impedance state when the data is output in sequence starting with bit 7 synchronized to the falling clock edge during read, status register read and silicon ID. Refer to "Figure 4 Serial Output Timing" for the serial output timing.

The LE25U20AFD supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0			
	0Bh	A23-A16	A15-A8	A7-A0	X		
Small sector erase	D7h/20h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *	PD *	PD *
Write enable	06h						
Write disable	04h						
Power down	B9h						
Status register read	05h						
Status register write	01h	DATA					
Read silicon ID 1	9Fh						
Read silicon ID 2	ABh	X	X	X			
Exit power down mode	ABh						

Explanatory notes for Table 2

"X" signifies "don't care" (that is to say, any value may be input).

The "h" following each code indicates that the number given is in hexadecimal notation.

Addresses A23 to A18 for all commands are "Don't care".

In order for commands other than the read command to be recognized, $\overline{CS}$ must rise after all the bus cycle input.

*: "PD" stands for page program data.

Figure 3 Serial Input Timing

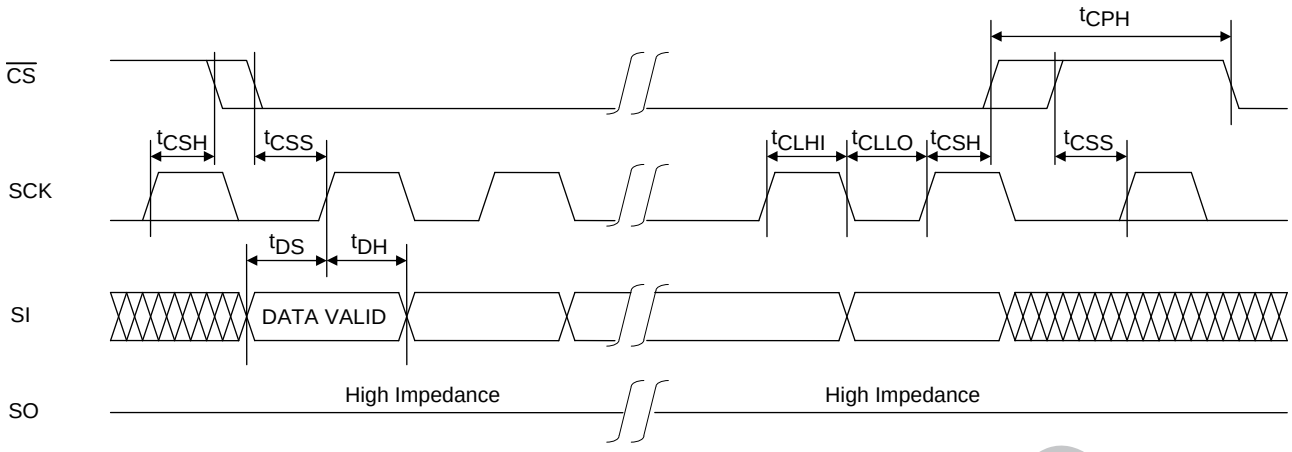
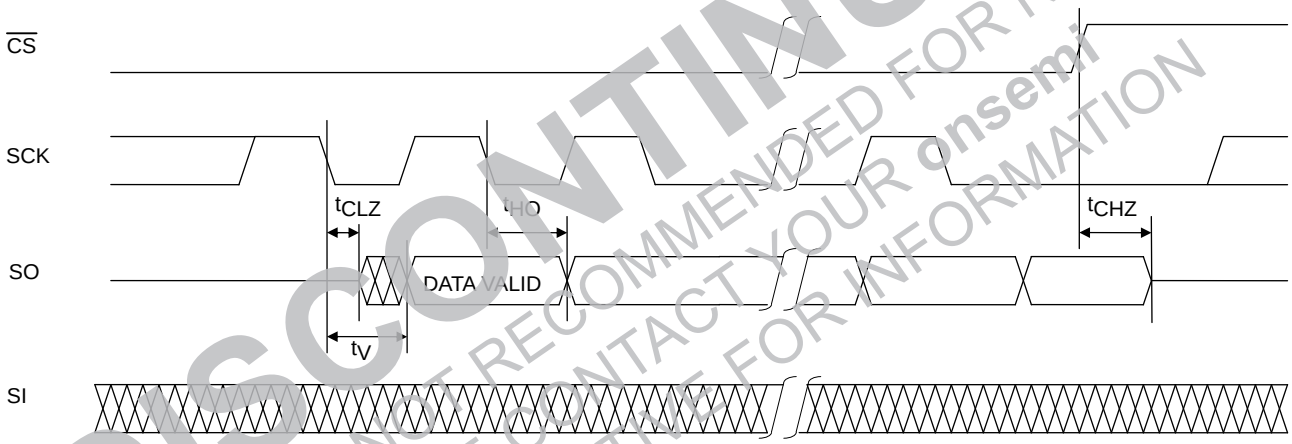


Figure 4 Serial Output Timing



Description of Commands and Their Operations

"Table 2 Command Settings" provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Read

There are two read commands, the 4 bus cycle read command and 5 bus cycle read command. Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h), and the data in the designated addresses is output synchronized to SCK. The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 5-a 4 Bus Read" shows the timing waveforms.

Consisting of the first through fifth bus cycles, the 5 bus cycle read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 5-b 5 Bus Read" shows the timing waveforms. The only difference between these two commands is whether the dummy bits in the fifth bus cycle are input.

When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (3FFFFh), the internal address returns to the lowest address (00000h), and data output is continued.

By setting the logic level of $\overline{CS}$ to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 5-a 4 Bus Read

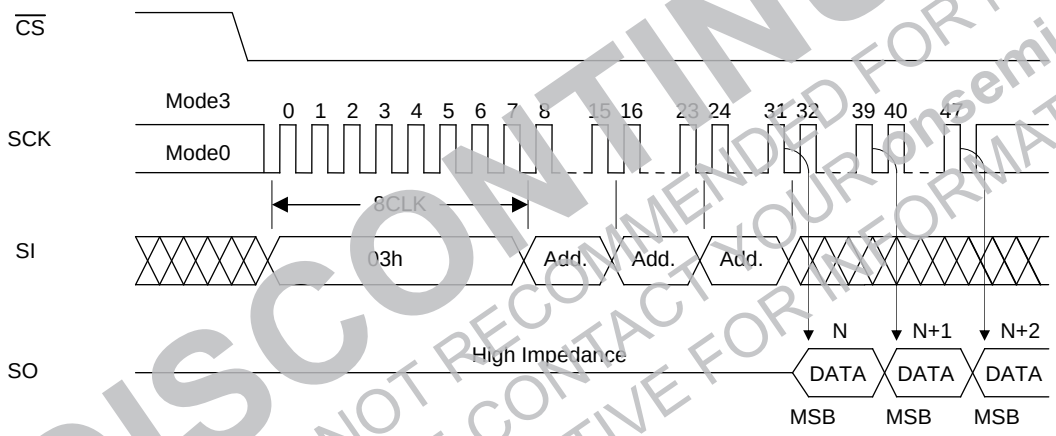
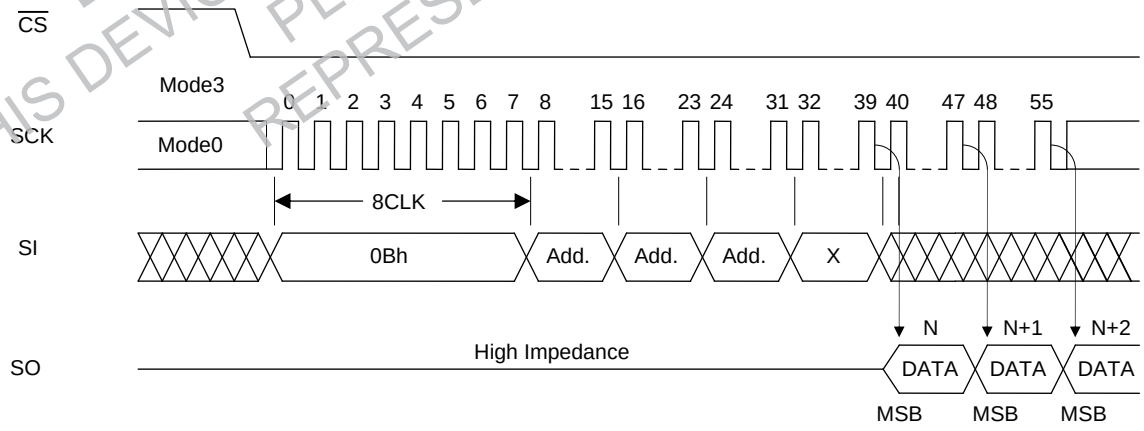


Figure 5-b 5 Bus Read



2. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 3 Status registers" gives the significance of each bit.

Table 3 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{RDY}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information See status register descriptions on BP0 and BP1.	Nonvolatile information
		1		
Bit3	BP1	0		Nonvolatile information
		1		
Bit4			Reserved bits	0
Bit5				0
Bit6				0
Bit7	SRWP	0	Status register write enabled	Nonvolatile information
		1	Status register write disabled	

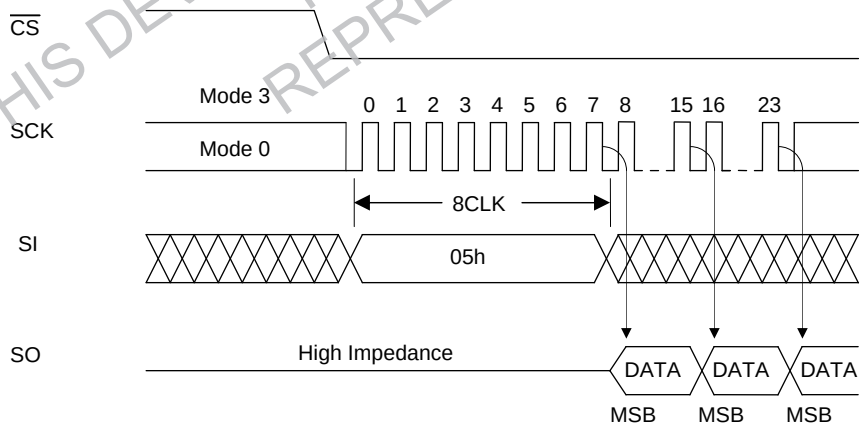
2-1. Status Register Read

The contents of the status registers can be read using the status register read command. This command can be executed even during the following operations.

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

"Figure 6 Status Register Read" shows the timing waveforms of status register read. Consisting only of the first bus cycle, the status register command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK) with which the eighth bit of (05h) has been input. In terms of the output sequence, SRWP (bit 7) is the first to be output, and each time one clock is input, all the other bits up to $\overline{RDY}$ (bit 0) are output in sequence, synchronized to the falling clock edge. If the clock input is continued after $\overline{RDY}$ (bit 0) has been output, the data is output by returning to the bit (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by the status register read command at any time (even during a program or erase cycle).

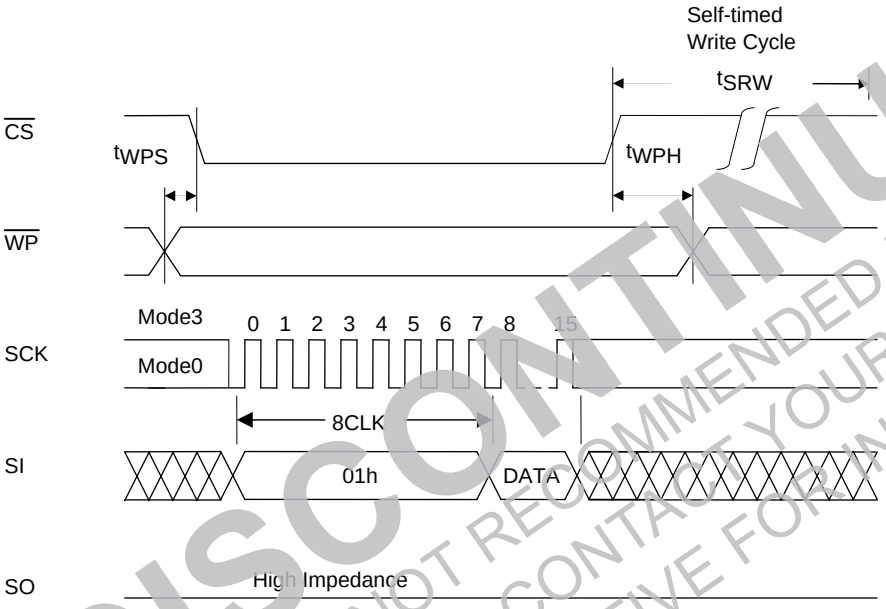
Figure 6 Status Register Read



2-2. Status Register Write

The information in status registers BP0, BP1, and SRWP can be rewritten using the status register write command. RDY, WEN, bit 4, bit 5, and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 7 Status Register Write" shows the timing waveforms of status register write, and Figure 20 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising CS edge after the data has been input following (01h). Erase and program are performed automatically inside the device by status register write so that erasing or other processing is unnecessary before executing the command. By the operation of this command, the information in bits BP0, BP1, and SRWP can be rewritten. Since bits RDY (bit 0), WEN (bit 1), bit 4, bit 5, and bit 6 of the status register cannot be written, no problem will arise if an attempt is made to set them to any value when rewriting the status register. Status register write ends can be detected by RDY of status register read. Information in the status registers can be rewritten 1,000 times (min.). To initiate status register write, the logic level of the WP pin must be set high and status register WEN must be set to "1".

Figure 7 Status Register Write



2-3. Contents of Each Status Register

RDY (bit 0)

The RDY register is for detecting the write (program, erase and status register write) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.

WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0". In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power-on
- Upon completion of small sector erase, sector erase or chip erase
- Upon completion of page program
- Upon completion of status register write

* If a write operation has not been performed inside the LE25U20AFD because, for instance, the command input for any of the write operations (small sector erase, sector erase, chip erase, page program, or status register write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1 (bits 2, 3)

Block protect BP0 and BP1 are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 4 Protect level setting conditions".

Table 4 Protect Level Setting Conditions

Protect Level	Status Register Bits		Protected Area
	BP1	BP0	
0 (Whole area unprotected)	0	0	None
1 (1/4 protected)	0	1	30000h to 3FFFFh
2 (1/2 protected)	1	0	20000h to 3FFFFh
3 (Whole area protected)	1	1	00000h to 3FFFFh

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the $\overline{WP}$ pin is low, the status register write command is ignored, and status registers BP0, BP1, and SRWP are protected. When the logic level of the $\overline{WP}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 5 SRWP setting conditions".

Table 5 SRWP Setting Conditions

$\overline{WP}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

Bits 4, Bits 5, and Bits 6 are reserved bits, and have no significance.

Figure 21 Erase Flowcharts

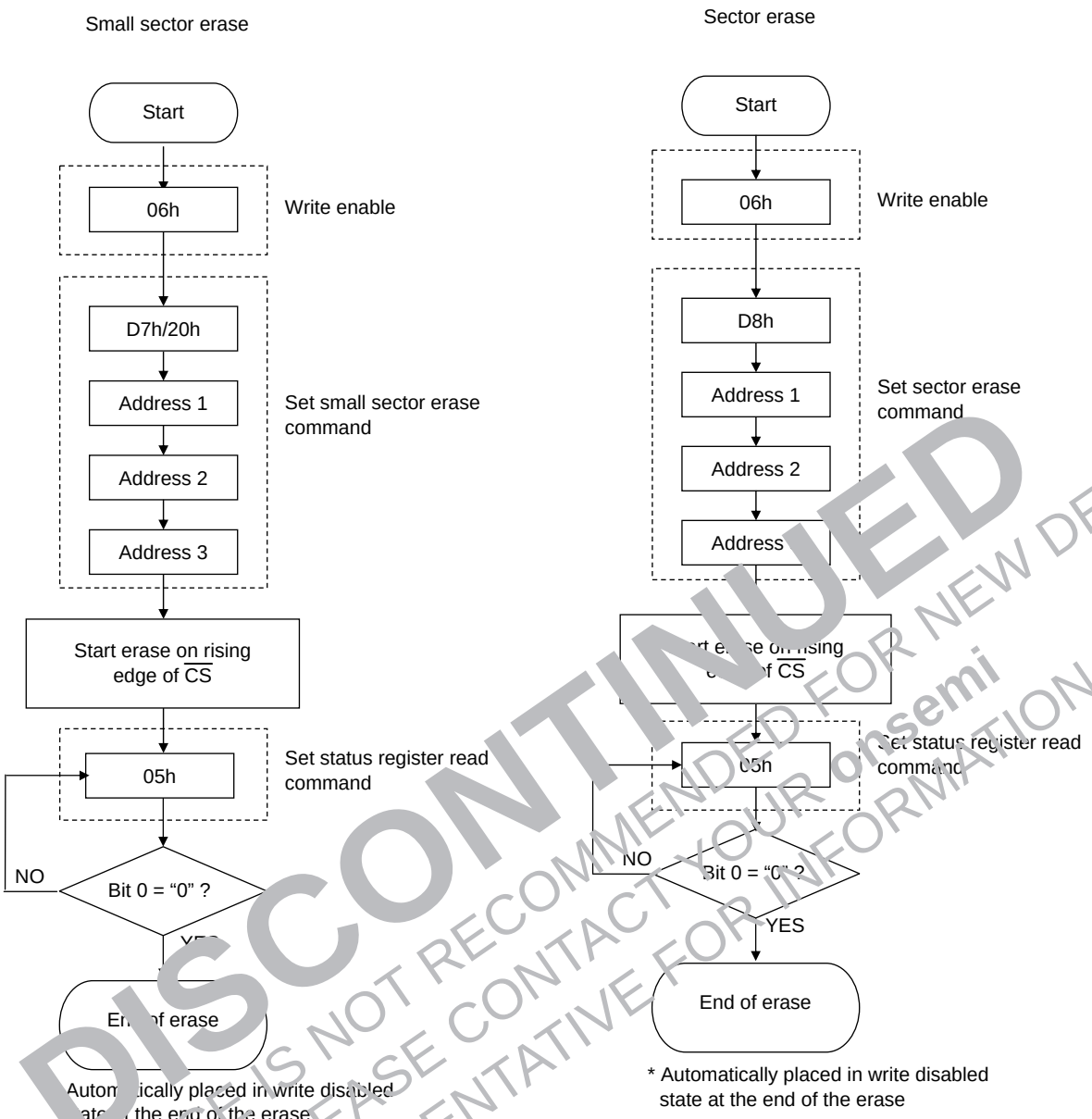
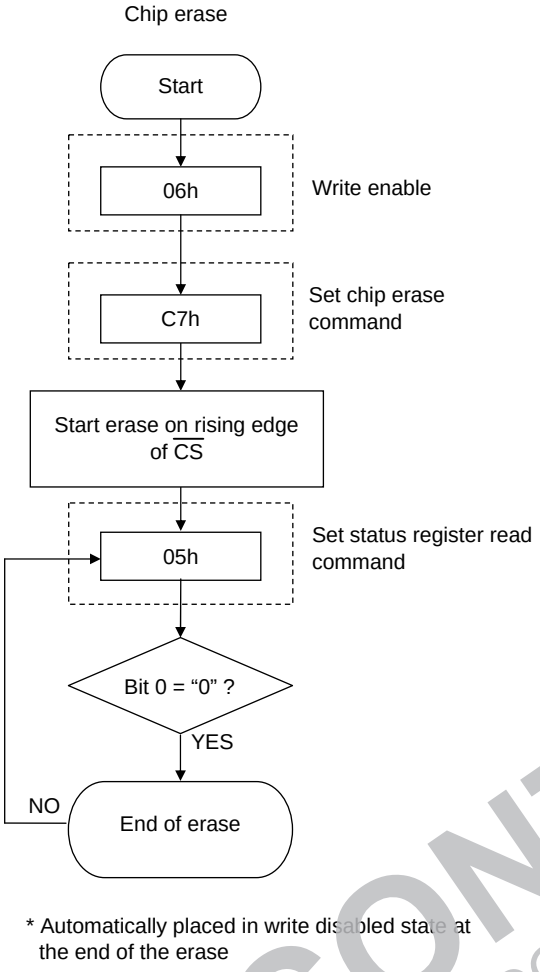
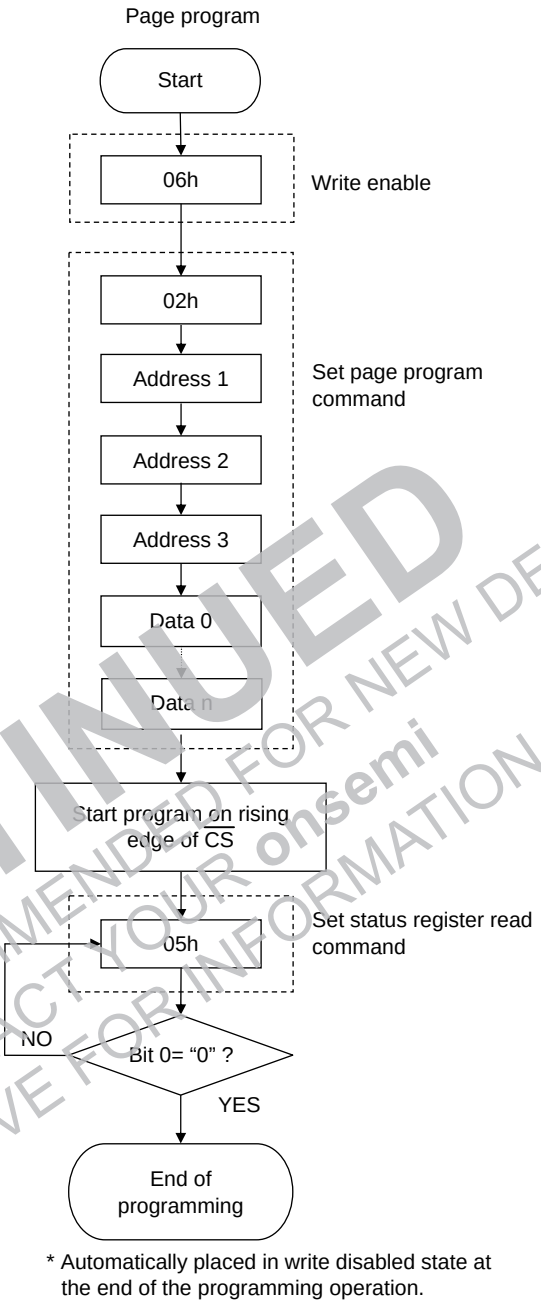


Figure 22 Page Program Flowchart





ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LE25U20AFD-AH	VSOIC8 NB (Pb-Free / Halogen Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF