BP0, BP1, BP2, TB (Bits 2, 3, 4, 5)

Block protect BP0, BP1, BP2 and TB are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 5 Protect level setting conditions".

BP0, BP1, and BP2 are used to select the protected area and TB to allocate the protected area to the higher-order address area or lower-order address area.

Table 5. Protect Level Setting Conditions

Protect Level	Status Register Bits				Protected Area
	TB	BP2	BP1	BP0	
0 (Whole area unprotected)	X	0	0	0	None
T1 (Upper side 1/8 protected)	0	0	0	1	07FFFFh to 070000h
T2 (Upper side 1/4 protected)	0	0	1	0	07FFFFh to 060000h
T3 (Upper side 1/2 protected)	0	0	1	1	07FFFFh to 040000h
B1 (Lower side 1/8 protected)	1	1	0	1	[illegible]FFh to 000000h
B2 (Lower side 1/4 protected)	1	1	1	0	01FF[illegible]h to 000000h
B3 (Lower side 1/2 protected)	1	1	1	1	03FF[illegible]h to 000000h
4 (Whole area protected)	X	1	X	X	[illegible]FFFFh to 000000h

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the $\overline{WP}$ pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, TB and SRWP are protected. When the logic level of the $\overline{WP}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 6 SRWP setting conditions".

Table 6. SRWP Setting Conditions

$\overline{WP}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

Bit 6 are reserved bits, and have no significance.

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4. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 8 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

5. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 9 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).

Figure 8 Write Enable

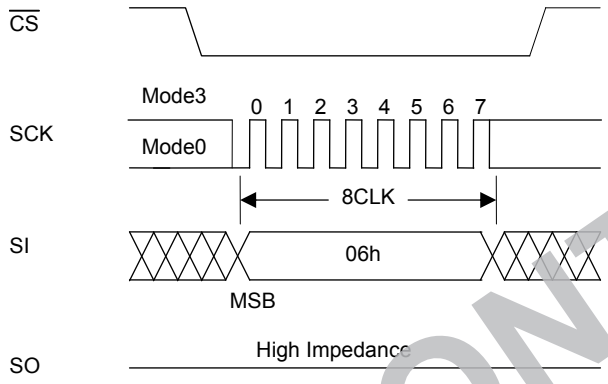
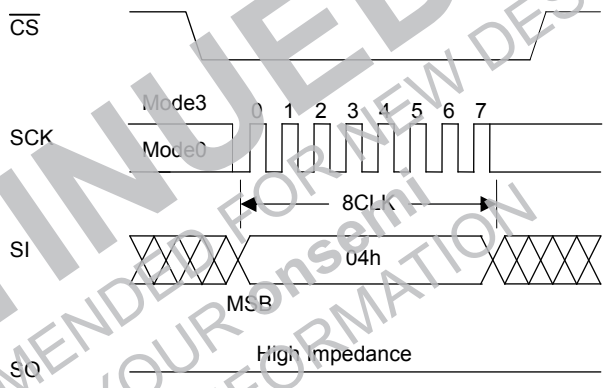


Figure 9 Write Disable



6. Power-down

The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 10 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 11 Exiting from Power-down" shows the timing waveforms of the power-down exit command.

Figure 10. Power-down

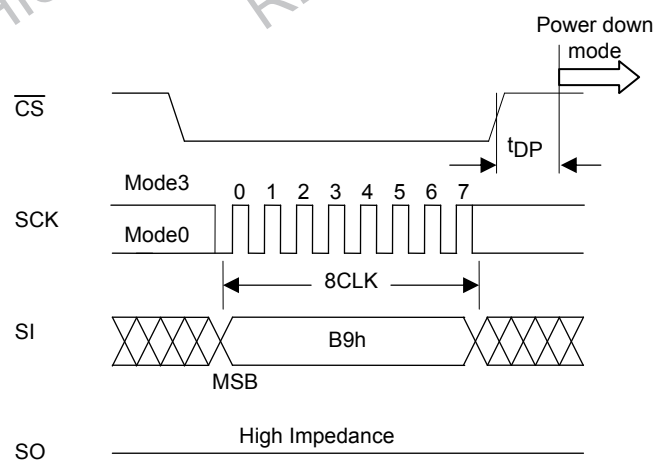
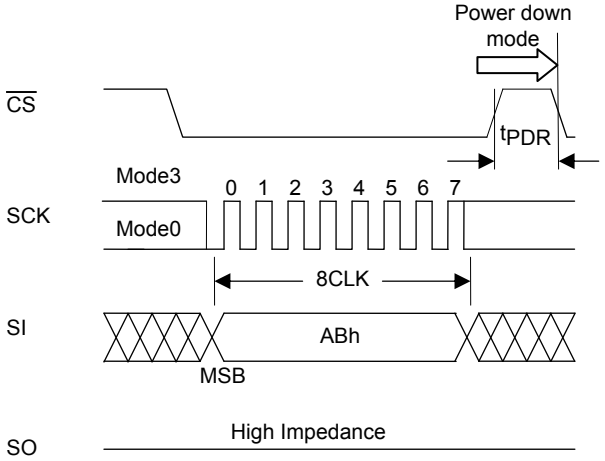


Figure 11. Exiting from Power-down



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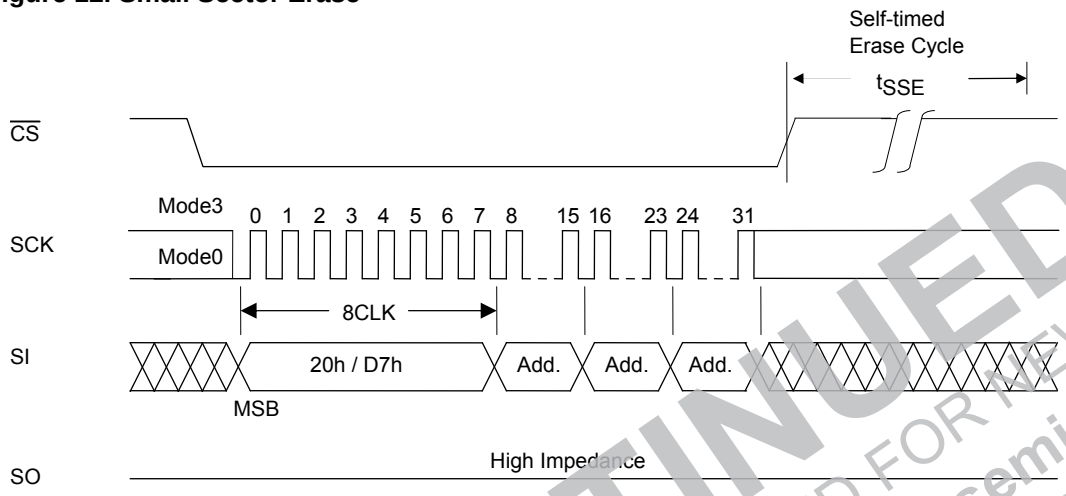
7. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 4Kbytes. "Figure 12 Small Sector Erase" shows the timing waveforms, and Figure 21 shows a small sector erase flowchart. The small sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (20h) or (D7h). Addresses A18 to A12 are valid, and Addresses A23 to A19 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

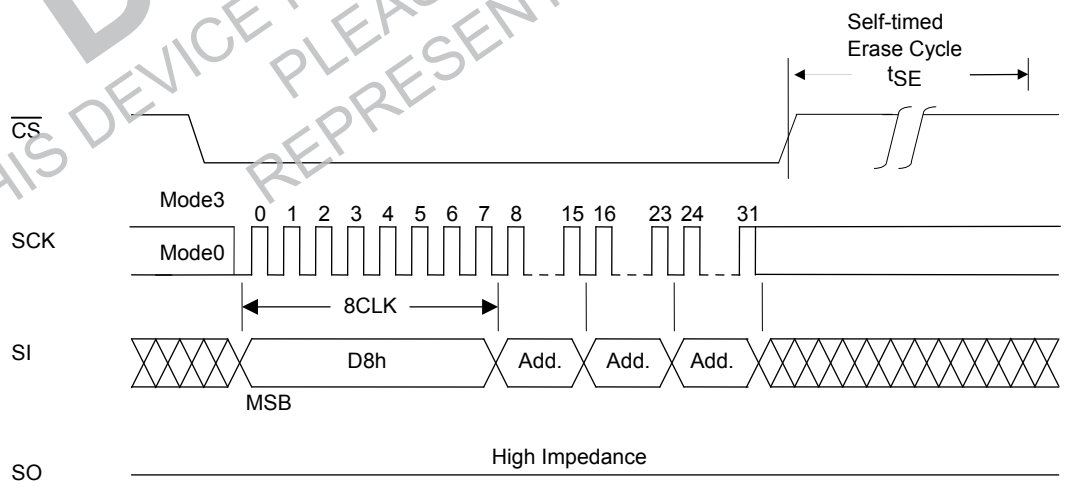
Figure 12. Small Sector Erase



8. Sector Erase

Sector erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64Kbytes. "Figure 13 Sector Erase" shows the timing waveforms, and Figure 21 shows a sector erase flowchart. The sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D8h). Addresses A18 to A16 are valid, and Addresses A23 to A19 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

Figure 13. Sector Erase



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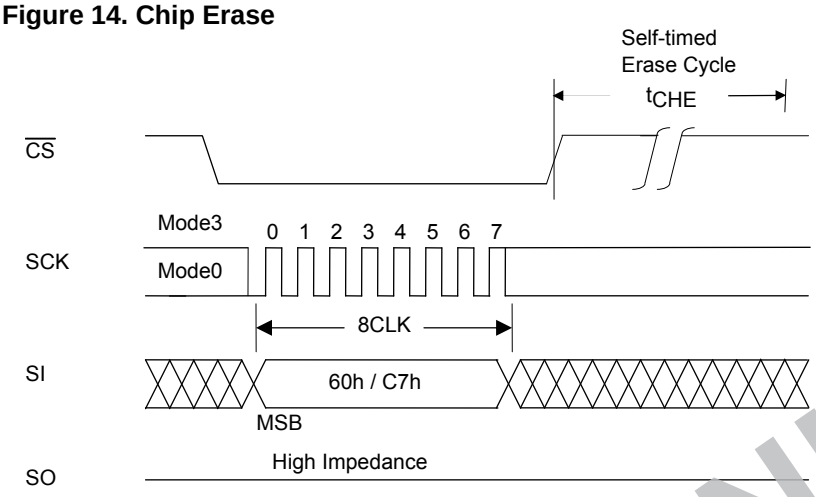
9. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 14 Chip Erase" shows the timing waveforms, and Figure 21 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (60h) or (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

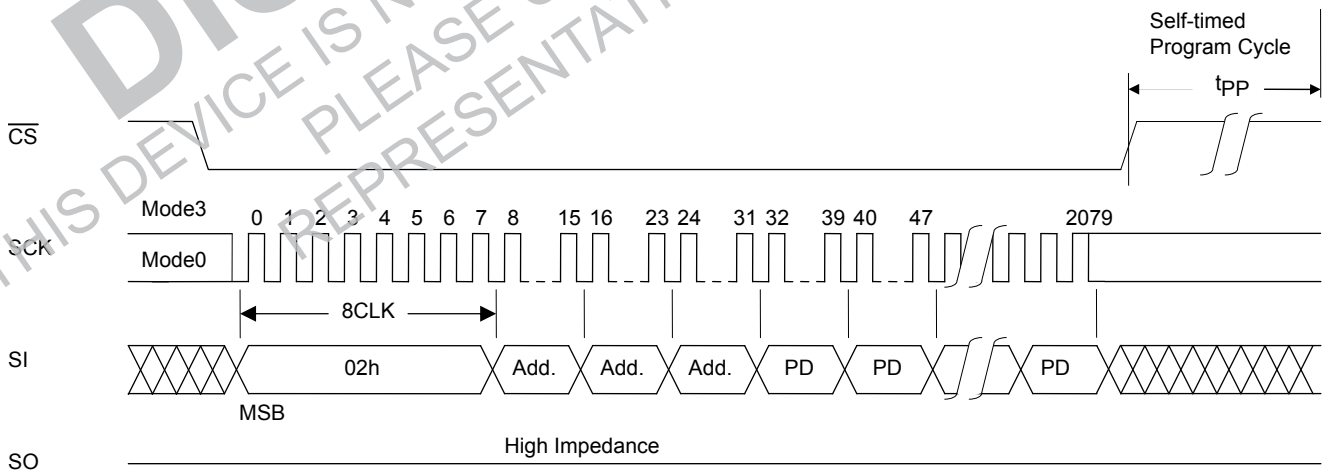
Figure 14. Chip Erase



10. Page Program

Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A18 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 15 Page Program" shows the page program timing waveforms, and Figure 22 shows a page program flowchart. After the falling $\overline{CS}$ edge, the command (02H) is input followed by the 24-bit addresses. Addresses A18 to A0 are valid. The program data is then loaded at each rising clock edge until the rising $\overline{CS}$ edge, and data loading is continued until the rising $\overline{CS}$ edge. If the data loaded has exceeded 256 bytes, the 256 bytes loaded last are programmed. The program data must be loaded in 1-byte increments, and the program operation is not performed at the rising $\overline{CS}$ edge occurring at any other timing.

Figure 15. Page Program



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11. Silicon ID Read

ID read is an operation that reads the manufacturer code and device ID information. The silicon ID read command is not accepted during writing. There are two methods of reading the silicon ID, each of which is assigned a device ID. In the first method, the read command sequence consists only of the first bus cycle in which (9Fh) is input. In the subsequent bus cycles, the manufacturer code 62h which is assigned by JEDEC, 2-byte device ID code (memory type, memory capacity), and reserved code are output sequentially. The 4-byte code is output repeatedly as long as clock inputs are present, "Table 7-1 JEDEC ID code " lists the silicon ID codes and "Figure 16-a JEDEC ID read" shows the JEDEC ID read timing waveforms.

The second method involves inputting the ID read command. This command consists of the first through fourth bus cycles, and the one bite silicon ID can be read when 24 dummy bits are input after (ABh). "Table 7-2 ID code " lists the silicon ID codes and "Figure 16-b ID read" shows the ID read timing waveforms.

If the SCK input persists after a device code is read, that device code continues to be output. The data output is transmitted starting at the falling edge of the clock for bit 0 in the fourth bus cycle and the silicon ID read sequence is finished by setting $\overline{CS}$ high.

Table 7-1. JEDEC ID code

		Output code
Manufacturer code		62h
2 byte device ID	Memory type	06h
	Memory capacity code	13h(4M Bit)
Device code	1	00h

Table 7-2. ID code

	Output Code
1 byte device ID	6E (LE25U40CMD)

Figure 16-a. JEDEC ID Read

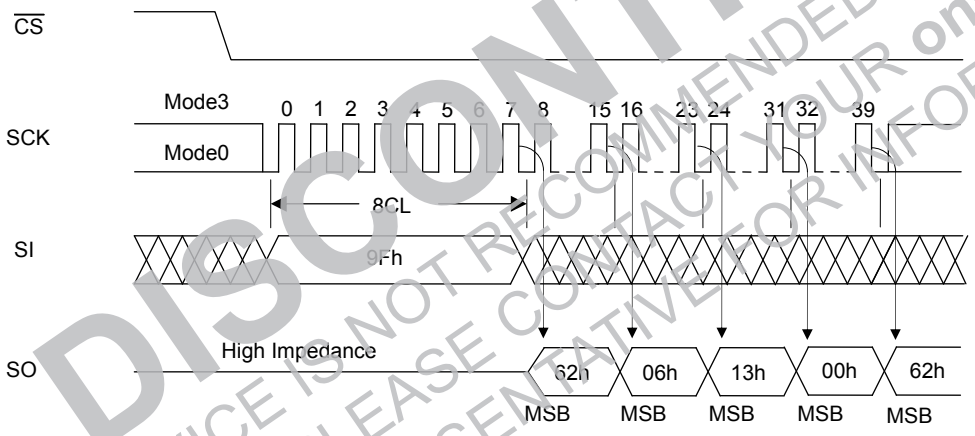
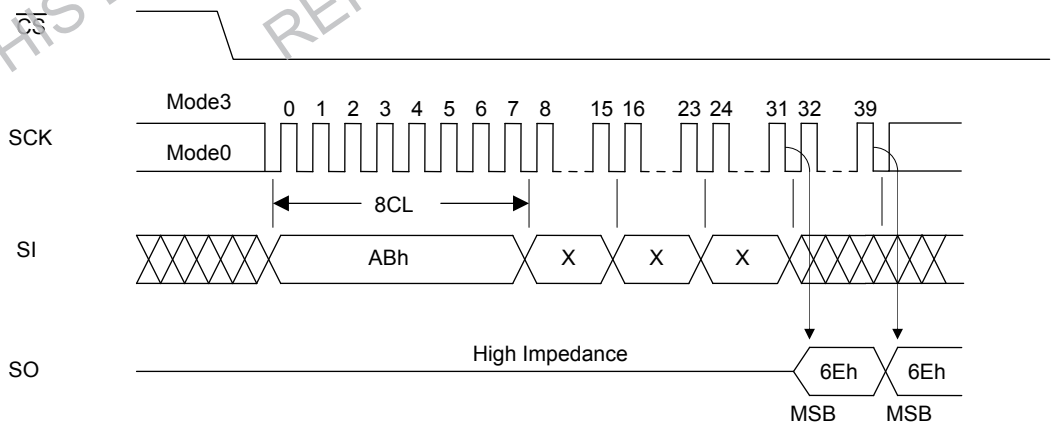


Figure 16-b. ID Read



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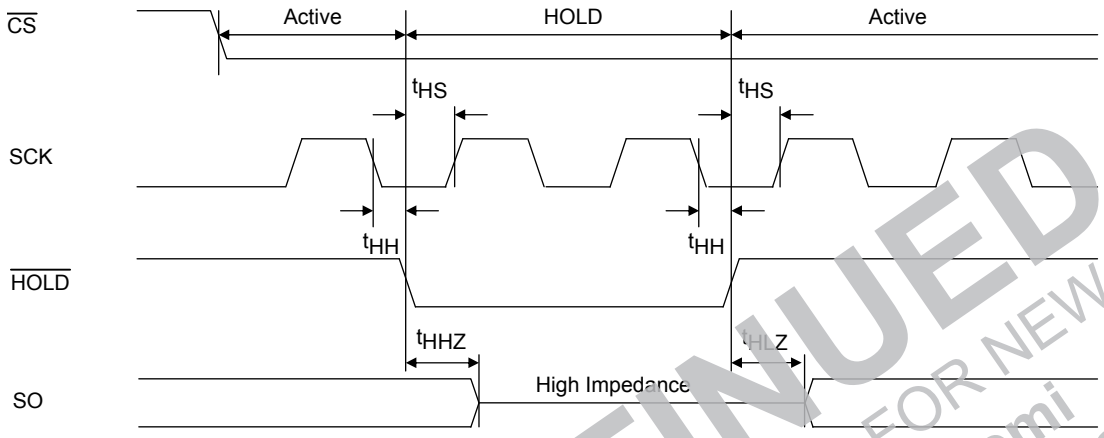
12. Hold Function

Using the $\overline{HOLD}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure17 $\overline{HOLD}$" shows the timing waveforms. The device is placed in the hold status at the falling $\overline{HOLD}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{HOLD}$ edge. When the logic level of SCK is high, $\overline{HOLD}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{CS}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{CS}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

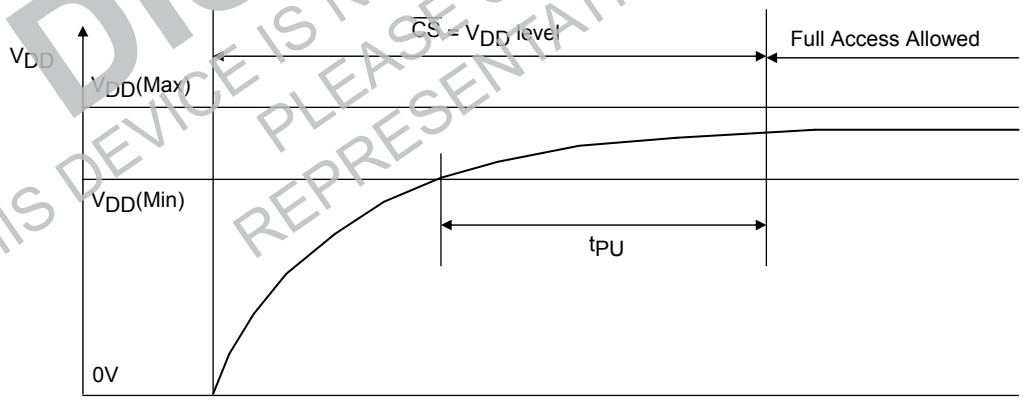
Figure 17. $\overline{HOLD}$



13. Power-on / Power-down

In order to protect against unintentional writing, $\overline{CS}$ must be within at V_{DD}−0.3 to V_{DD}+0.3 on power-on. After power-on, the supply voltage has stabilized at V_{DD} min. or higher, waits for t_{PU} before inputting the command to start a device operation. The device is in the standby state and not in the power-down state after power is turned on. To put the device into the power-down state, it is necessary to enter a power-down command.

Figure 18. Power-on Timing



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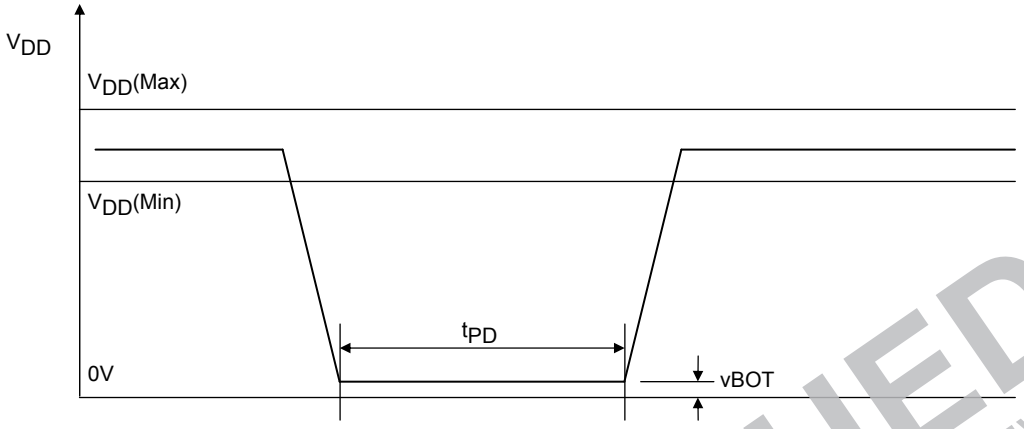
LE25U40CMD incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19. Power-down Timing



Power-on timing

Parameter	Symbol	spec		unit
		min	max	
power-on to operation time	t_{PU}	100		μs
power-down time	t_{PD}	10		ms
power-down voltage	t_{BOT}		0.2	V

14. Software Data Protection

The LE25U40CMD eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)
- When the page program data is not in 1-byte increments
- When the status register write command is input for 2 bus cycles or more

15. Decoupling Capacitor

A 0.1uF ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

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Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{DD} max	With respect to V_{SS}	−0.5 to +4.6	V
DC voltage (all pins)	VIN/VOUT	With respect to V_{SS}	−0.5 to V_{DD}+0.5	V
Storage temperature	Tstg		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage	V_{DD}		2.3 to 3.6	V
Operating ambient temperature	Topr		−40 to 85	°C

Allowable DC Operating Conditions

Parameter	Symbol	Conditions			Ratings min	Ratings typ	Ratings max	unit
Read mode operating current	I_{CCR}	SCK=0.1V_{DD}/0.9V_{DD}, $\overline{HOLD}$=$\overline{WP}$=0.9V_{DD}, Output = open	Single	25MHz			6	mA
				40MHz			10	
			Dual	40MHz			12	mA
Write mode operating current (erase + page program)	I_{CCW}	t_{SSE}= t_{SE}= t_{CHE}=Typ, t_{PP}=Max					15	mA
CMOS standby current	I_{SB}	$\overline{CS}$=V_{DD}, $\overline{HOLD}$=$\overline{WP}$=V_{DD}, SI=V_{SS}/V_{DD}, SO=open,					50	μA
Power-down standby current	I_{DSB}	$\overline{CS}$=V_{DD}, $\overline{HOLD}$=$\overline{WP}$=V_{DD}, SI=V_{SS}/V_{DD}, SO=open,					10	μA
Input leakage current	I_{LI}						2	μA
Output leakage current	I_{LO}						2	μA
Input low voltage	V_{IL}				−0.3		0.3V_{DD}	V
Input high voltage	V_{IH}				0.7V_{DD}		V_{DD}+0.3	V
Output low voltage	V_{OL}	I_{OL}=100μA, V_{DD}=V_{DD} min					0.2	V
		I_{OL}=1.6mA, V_{DD}=V_{DD} min					0.4	
Output high voltage	V_{OH}	I_{OH}=−100μA, V_{DD}=V_{DD} min			V_{DD}−0.2			V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Data hold, Rewriting frequency

Parameter	condition	min	max	unit
Rewriting frequency	Program/Erase	100,000		times/ Sector
	Status resister write	1,000		times
Data hold		20		year

Pin Capacitance at Ta=25°C, f=1MHz

Parameter	Symbol	Conditions	Ratings max	unit
Output pin capacitance	C_{SO}	V_{SO}=0V	12	pF
Input pin Capacitance	C_{IN}	V_{IN}=0V	6	pF

Note: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

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AC Characteristics

Parameter			Symbol	Ratings			unit
				min	typ	max	
Clock frequency	Read instruction(03h)		f_{CLK}			25	MHz
	All instructions except for read(03h)					40	MHz
Input signal rising/falling time			t_{RF}	0.1			V/ns
SCK logic high level pulse width		25MHz	t_{CLHI}	16			ns
		40MHz		11.5			ns
SCK logic low level pulse width		25MHz	t_{CLLO}	16			ns
		40MHz		11.5			ns
$\overline{CS}$ setup time			t_{CSS}	8			ns
$\overline{CS}$ hold time			t_{CSH}	8			ns
Data setup time			t_{DS}	2			ns
Data hold time			t_{DH}	5			ns
$\overline{CS}$ wait pulse width			t_{CPH}	25			ns
Output high impedance time from $\overline{CS}$			t_{CHZ}			8	ns
Output data time from SCK			t_V		8	11	ns
Output data hold time			t_{HO}	1			ns
Output low impedance time from SCK			t_{CLZ}	0			ns
$\overline{HOLD}$ setup time			t_{HS}	5			ns
$\overline{HOLD}$ hold time			t_{HH}	3			ns
Output low impedance time from $\overline{HOLD}$			t_{HLZ}			9	ns
Output high impedance time from $\overline{HOLD}$			t_{HHZ}			9	ns
$\overline{WP}$ setup time			t_{WPS}	20			ns
$\overline{WP}$ hold time			t_{WPH}	20			ns
Power-down time			t_{DP}			3	μs
Power-down recovery time			t_{PDR}			3	μs
Write status register time			t_{SRW}		5	15	ms
Page programming cycle time			t_{PP}		4	5	ms
Small sector erase cycle time			t_{SSE}		40	150	ms
Sector erase cycle time			t_{SE}		80	250	ms
Chip erase cycle time			t_{CHE}		0.25	2.0	s

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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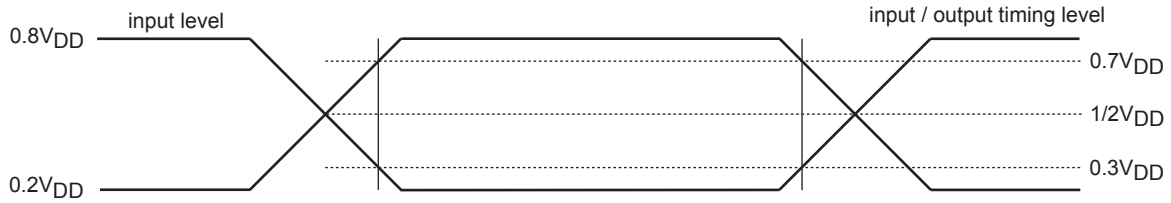
AC Test Condtions

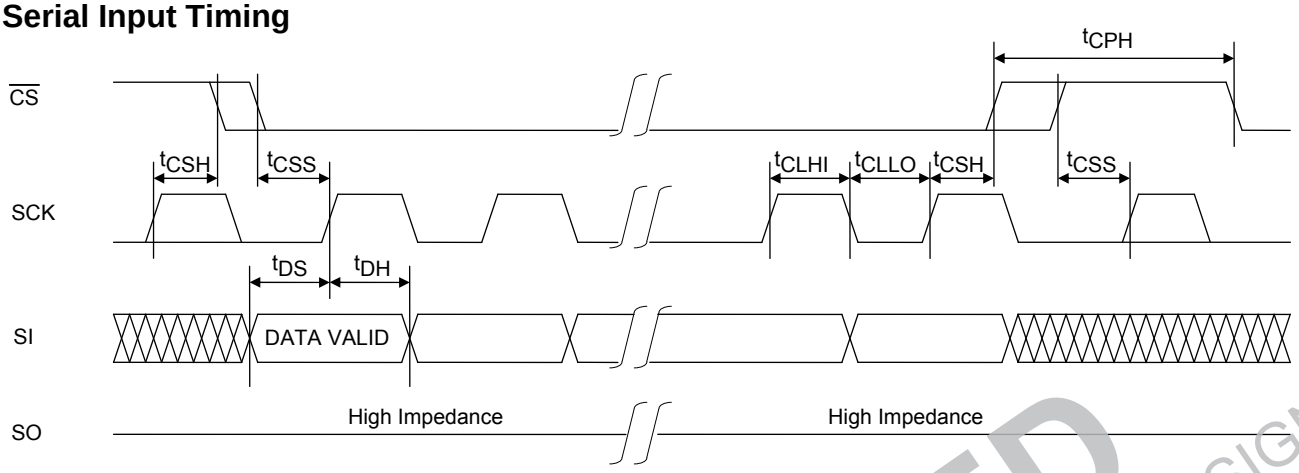
Input pulse level ····· $0.2V_{DD}$ to $0.8V_{DD}$
Input rising/falling time ·· 5ns
Input timing level ····· $0.3V_{DD}$, $0.7V_{DD}$
Output timing level ····· $1/2 \times V_{DD}$
Output load ····· 30pF

Note: As the test conditions for "typ", the measurements are conducted using 2.5V for V_{DD} at room temperature.

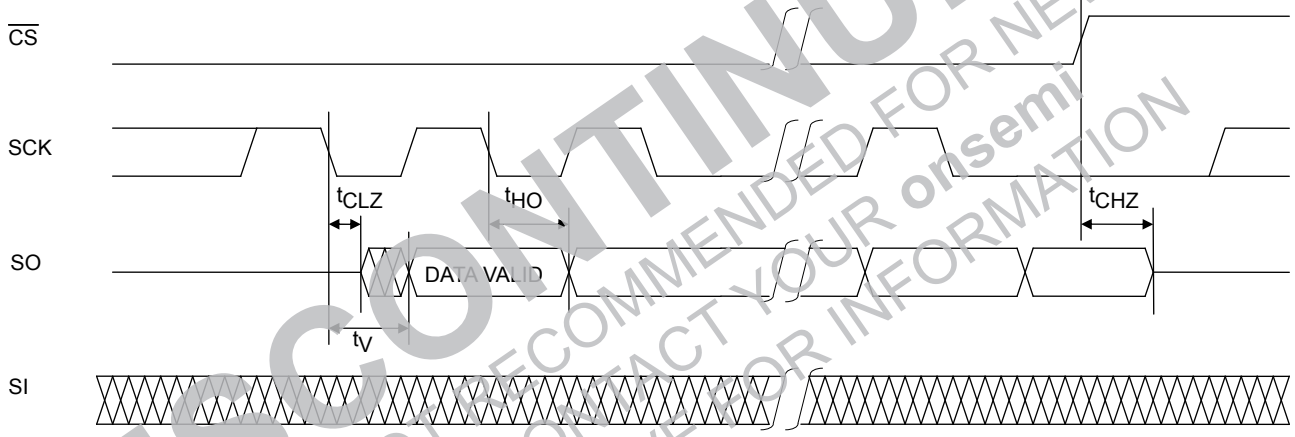


Timing waveforms

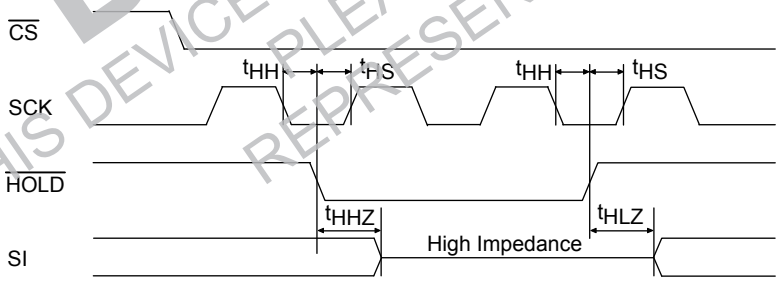
Serial Input Timing



Serial Output Timing



Hold Timing



Status register write Timing

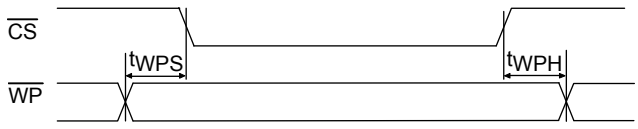


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Figure 20. Status Register Write Flowchart

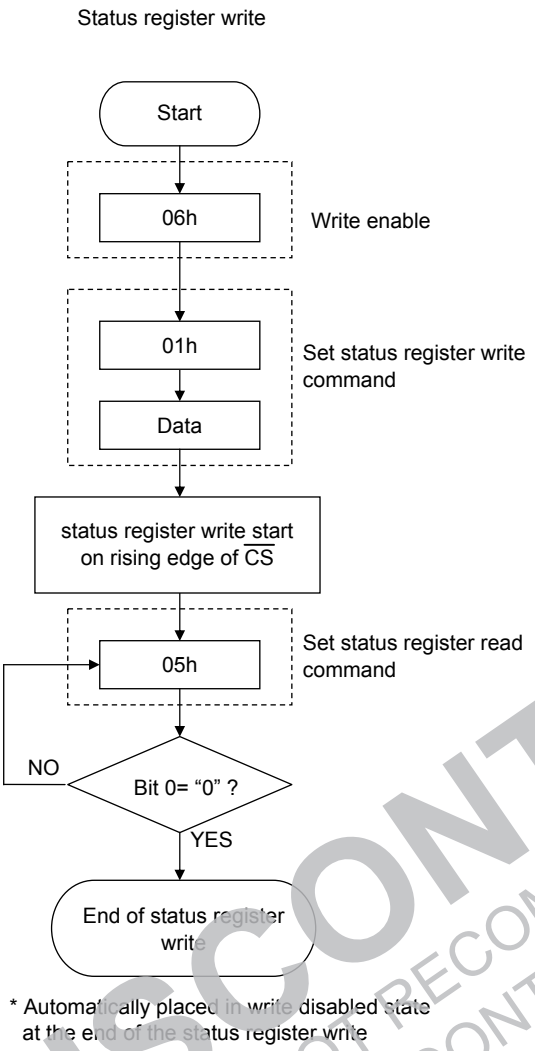

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Figure 21. Erase Flowcharts

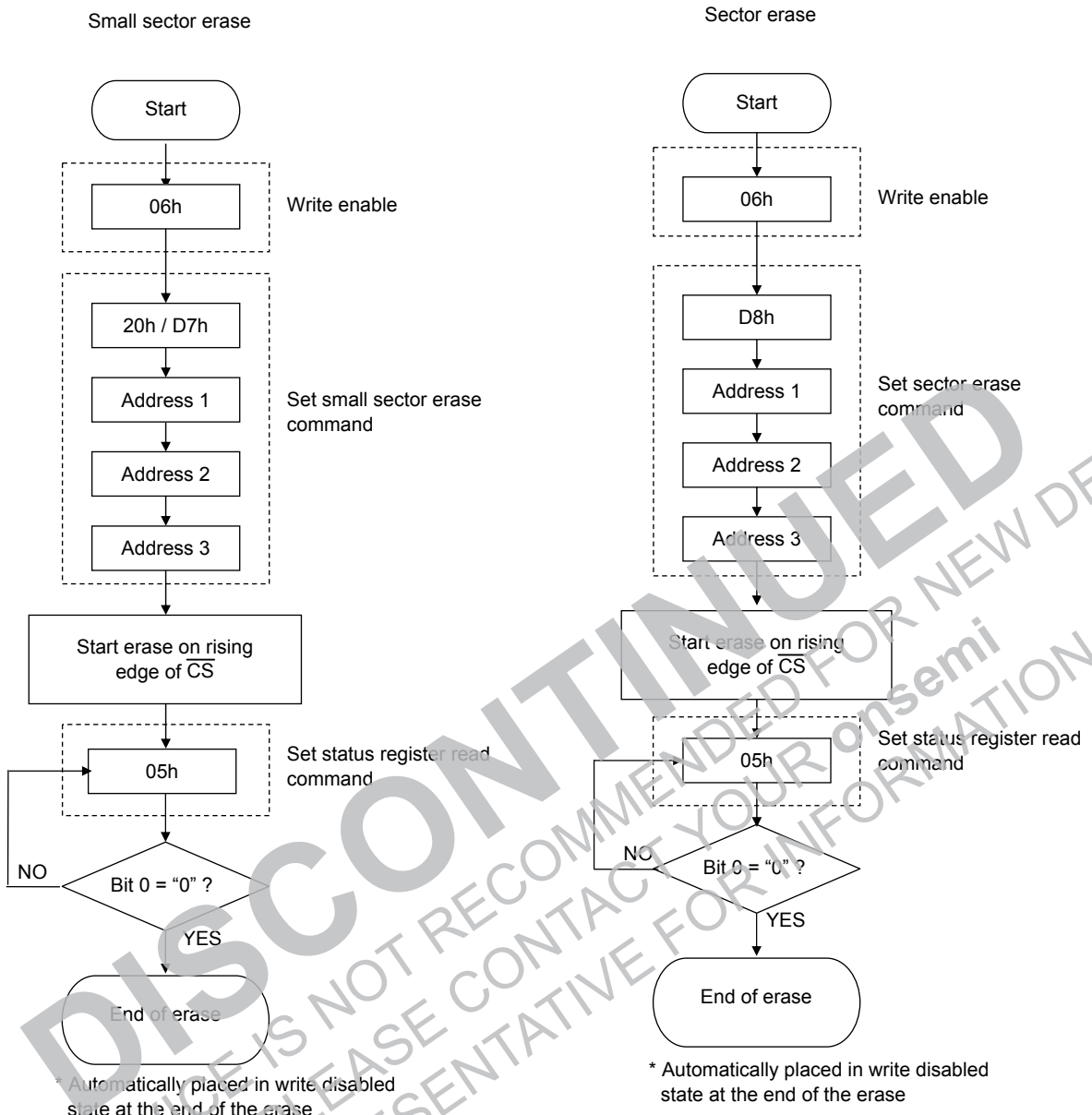

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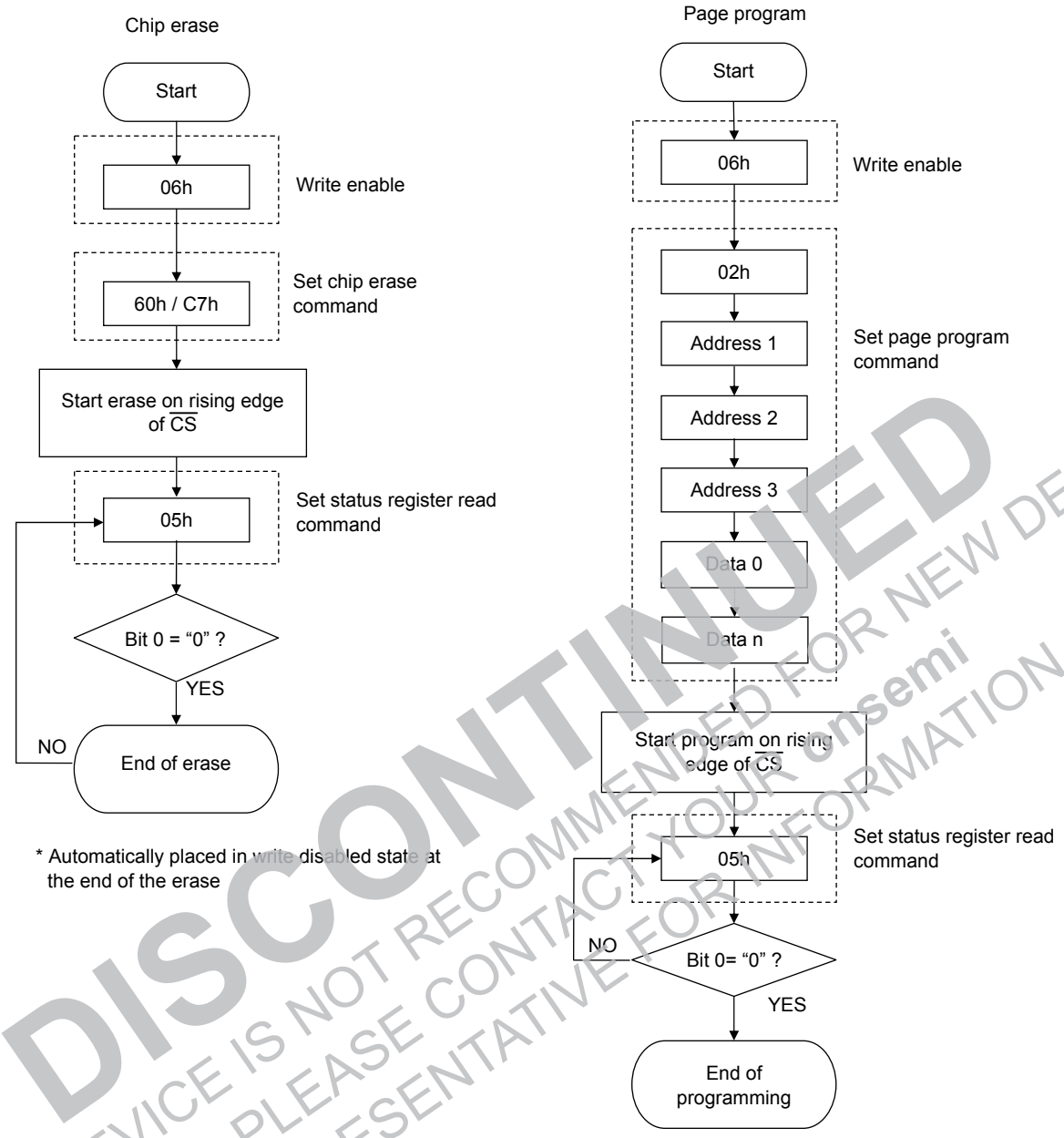
Figure 22. Page Program Flowchart



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ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LE25U40CMDTWG	SOIC 8, 150 mils (Pb-Free / Halogen Free)	2000 / Tape & Reel

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