

# 3.3 V/5 V ECL 9-Bit Shift Register

## MC100EP142

### Description

The MC100EP142 is a 9-bit shift register, designed with byte-parity applications in mind. The MC100EP142 is capable of performing serial/parallel data into serial/parallel out and shifting in only one direction. The nine inputs D0 – D8 accept parallel input data, while S-IN accepts serial input data. The QT0:87 outputs do not need to be terminated for the shift operation to function. To minimize power, any Q output not used should be left unterminated.

The SEL (Select) input pin is used to switch between the two modes of operation – SHIFT and LOAD. The shift direction is from Bit 0 to Bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK0 or CLK1; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero, overriding CLK0 and CLK1 inputs.

The 100 Series contains temperature compensation.

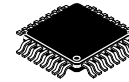
### Features

- Shift Frequency >2.8 GHz (Typical)
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- These Devices are Pb-Free and are RoHS Compliant



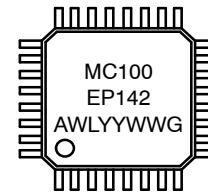
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LQFP-32  
FA SUFFIX  
CASE 561AB

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping
MC100EP142FAG	LQFP-32 (Pb-Free)	250 Units / Tray

# MC100EP142

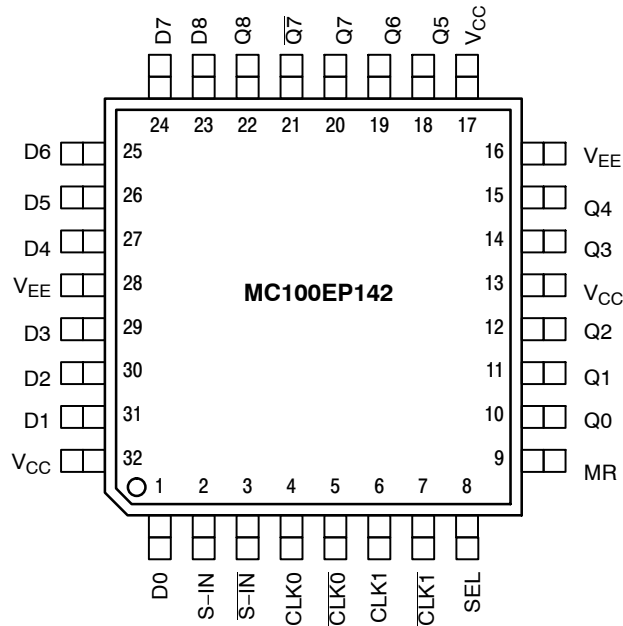


Figure 1. Pinout: LQFP-32 (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Default State	Description
1,31,30,29,27,26,25,24,23	D[0:8]	ECL Input	Low	Single-Ended Parallel Data Inputs [0:8]. Internal 75 kΩ to V <sub>EE</sub> .
2	S-IN	ECL Input	Low	Noninverted Differential Serial Input. Internal 75 kΩ to V <sub>EE</sub> .
3	S-IN	ECL Input	High	Inverted Differential Serial Input. Internal 75 kΩ to V <sub>EE</sub> and 36.5 kΩ to V <sub>CC</sub> .
4	CLK0	ECL Input	Low	Noninverted Differential CLK0 Input. Internal 75 kΩ to V <sub>EE</sub> .
5	CLK0	ECL Input	High	Inverted Differential CLK0B Input. Internal 75 kΩ to V <sub>EE</sub> and 36.5 kΩ to V <sub>CC</sub> .
6	CLK1	ECL Input	Low	Noninverted Differential CLK1 Input. Internal 75 kΩ to V <sub>EE</sub> .
7	CLK1	ECL Input	High	Inverted Differential CLK1B Input. Internal 75 kΩ to V <sub>EE</sub> and 36.5 kΩ to V <sub>CC</sub> .
8	SEL	ECL Input	Low	Single-Ended Select Logic Input. Internal 75 kΩ to V <sub>EE</sub> .
9	MR	ECL Input	Low	Single-Ended Master Reset Logic Input. Internal 75 kΩ to V <sub>EE</sub> .
10,11,12,14,15,18,19,22	Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q8	ECL Output	-	Single-Ended parallel Data outputs [0,1,2,3,4,5,6,8]. Typically Terminated with 50 Ω to V <sub>TT</sub> = V <sub>CC</sub> - 2 V.
13,17,32	V <sub>CC</sub>	-	-	Positive supply Voltage. All V <sub>CC</sub> Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
16,28	V <sub>EE</sub>	-	-	Negative supply Voltage. All V <sub>EE</sub> Pins must be Externally connected to Power Supply to Guarantee Proper Operation.
20	Q7	ECL Output	-	Noninverted Differential parallel/Serial Data Output 7. Typically Terminated with 50 Ω to V <sub>TT</sub> = V <sub>CC</sub> - 2 V.
21	Q7	ECL Output	-	Inverted Differential parallel/Serial Data Output 7. Typically Terminated with 50 Ω to V <sub>TT</sub> = V <sub>CC</sub> - 2 V.

1. All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

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**Table 2. TRUTH TABLE**

Function (Note 2)	SEL	S-IN	MR	CLK0	CLK1	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9
<b>Load</b>	L	X	L	Z	Z	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
<b>Shift</b>	H	L	L	Z	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
	H	H	L	Z	Z	H	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
<b>Reset</b>	X	X	H	Z	Z	L	L	L	L	L	L	L	L	L	L

2. All Load and Shift functions are accomplished on the positive edge of CLK0 or CLK1.

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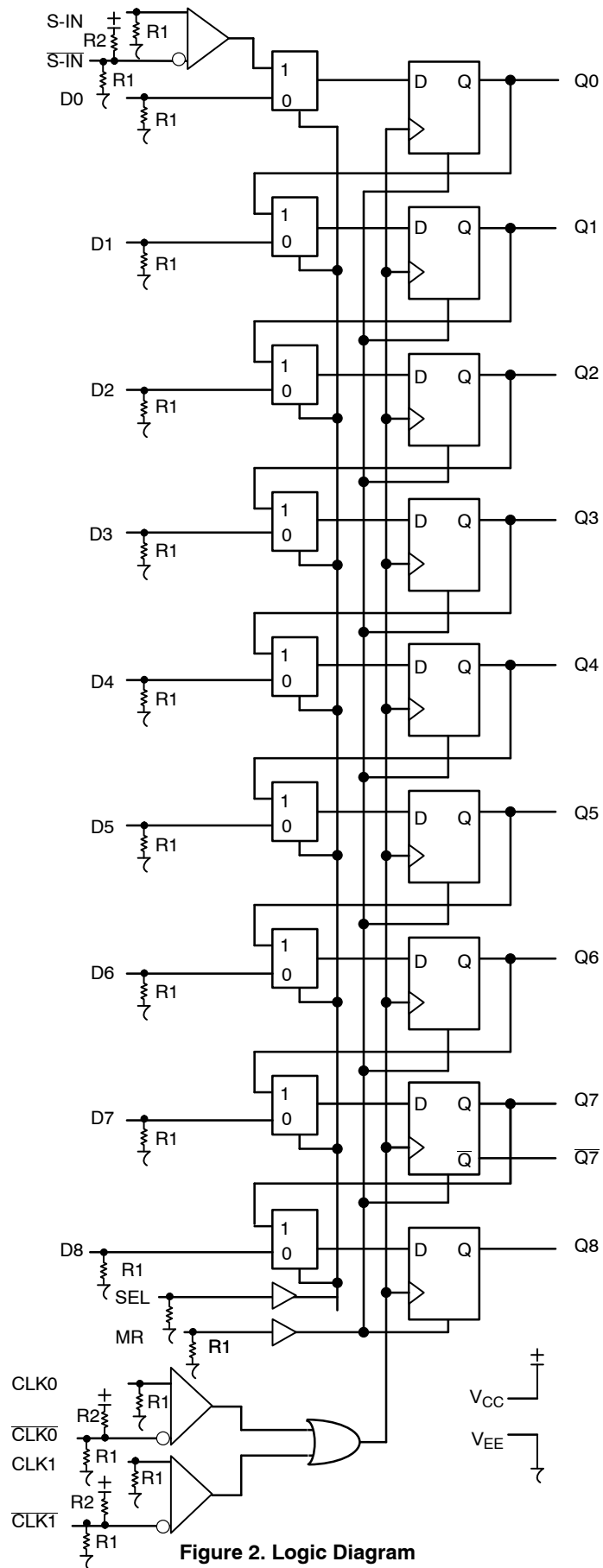


Figure 2. Logic Diagram

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**Table 3. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor (R1)	75 k $\Omega$
Internal Input Pullup Resistor (R2)	37.5 k $\Omega$
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 3) LQFP-32	Level 2
Flammability Rating Oxygen Index: 28 to 34	UL-94 V-0 @ 0.125 in
Transistor Count	405 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, refer to Application Note [AND8003/D](#).

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	Negative Power Supply	V <sub>CC</sub> = 0 V		-8	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> $\leq$ V <sub>CC</sub> V <sub>I</sub> $\geq$ V <sub>EE</sub>	6 -6	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	$^{\circ}$ C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	$^{\circ}$ C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	LQFP-32 LQFP-32	80 55	$^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	LQFP-32	12 to 17	$^{\circ}$ C/W
T <sub>sol</sub>	Wave Solder Pb-Free	$\leq$ 3 sec @ 260 $^{\circ}$ C		265	$^{\circ}$ C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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**Table 5. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	105	125	145	105	130	150	105	130	150	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 5)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1305		1675	1305		1675	1305		1675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ )			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) CLK0, CLK1, D, S-IN CLK0, CLK1, S-IN	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
5. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
6.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 6. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current (Note 8)	105	125	145	105	130	150	105	130	150	mA
$V_{OH}$	Output HIGH Voltage (Note 9)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 9)	3005	3180	3305	3005	3180	3305	3005	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3005		3375	3005		3375	3005		3375	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ )			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) CLK0, CLK1, D, S-IN CLK0, CLK1, S-IN	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

7. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

8. Required 500 lfm air flow when using +5 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ , 5  $\Omega$  to 10  $\Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC} - V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

9. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

10.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current (Note 12)	105	125	145	105	130	150	105	130	150	mA
$V_{OH}$	Output HIGH Voltage (Note 13)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 13)	-1995	-1820	-1695	-1995	-1820	-1695	-1995	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1995		-1625	-1995		-1625	-1995		-1625	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 14)	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ )			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) CLK0, CLK1, D, S-IN CLK0, CLK1, S-IN	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .

12. Required 500 lfm air flow when using -5 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ , 5  $\Omega$  to 10  $\Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC} - V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

13. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

14.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 8. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ;  $V_{EE} = 0.0\text{ V or }V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$  (Note 15)

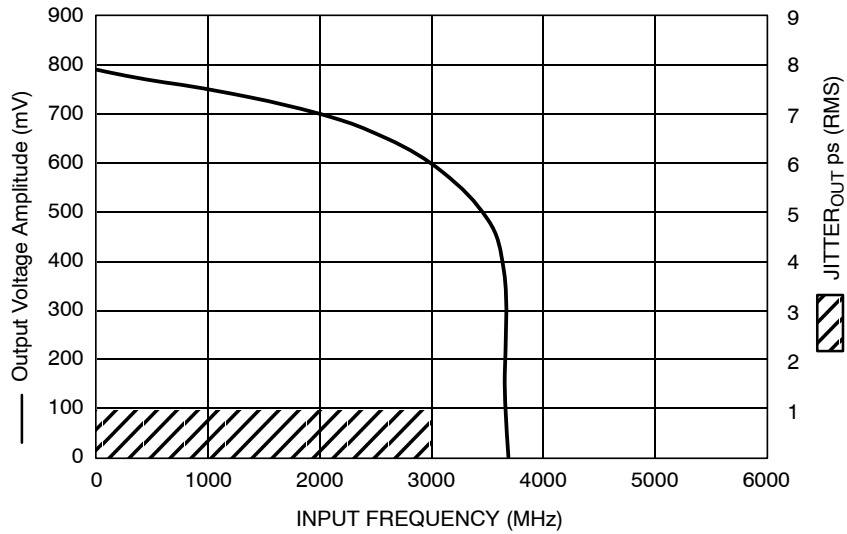
Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{SHIFT}$	Maximum Shift Frequency					2.8					GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output CLKx MR	500 500	625 625	750 750	550 550	675 675	800 800	575 575	700 700	825 825	ps
$t_s$	Setup Time D SEL	50 100	-50 50		50 100	-50 50		50 100	-50 50		ps
$t_h$	Hold Time D SEL	100 50	50 -50		100 50	50 -50		100 50	50 -50		ps
$t_{RR}$	Reset Recovery Time					800					ps
$t_{pw}$	Minimum Pulse Width					200					ps
$t_{SKEW}$	Within-Device Skew (Note 16) Duty Cycle Skew (Note 17) Q, $\bar{Q}$		50 5.0	100 20		50 5.0	100 20		50 5.0	100 20	ps
$t_{JITTER}$	Random Clock Jitter (Figure 3)		1	2		1	2		1	2	ps
$V_{inpp}$	Input Voltage Swing/Sensitivity (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ , $t_f$	Rise/Fall Times @ 50 MHz (20 - 80%)	110	180	250	125	190	275	150	215	300	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

15. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

16. Within-device skew is defined as identical transitions on similar paths through a device.

17. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.



**Figure 3. Output Voltage Amplitude / RMS Jitter vs. Input Frequency at Ambient Temperature (Typical)**



## MC100EP142

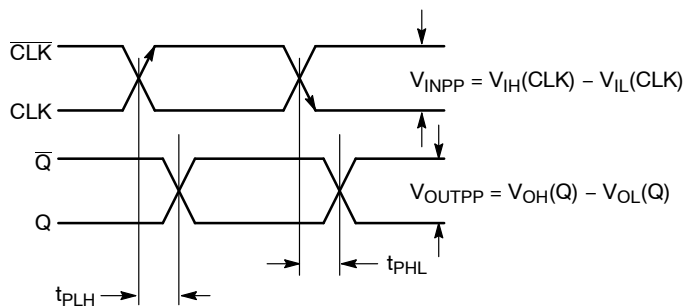


Figure 4. AC Reference Measurement

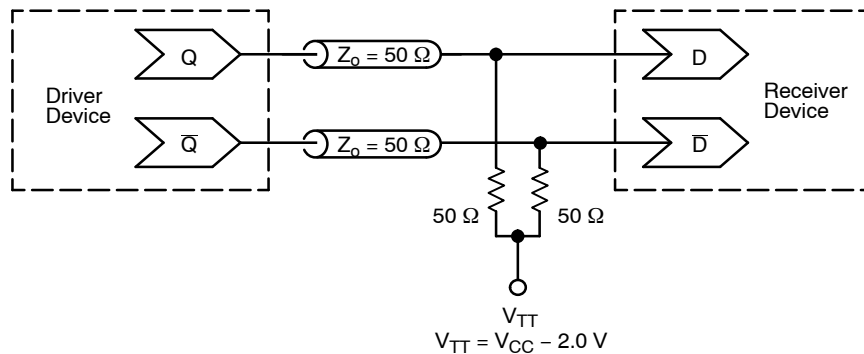


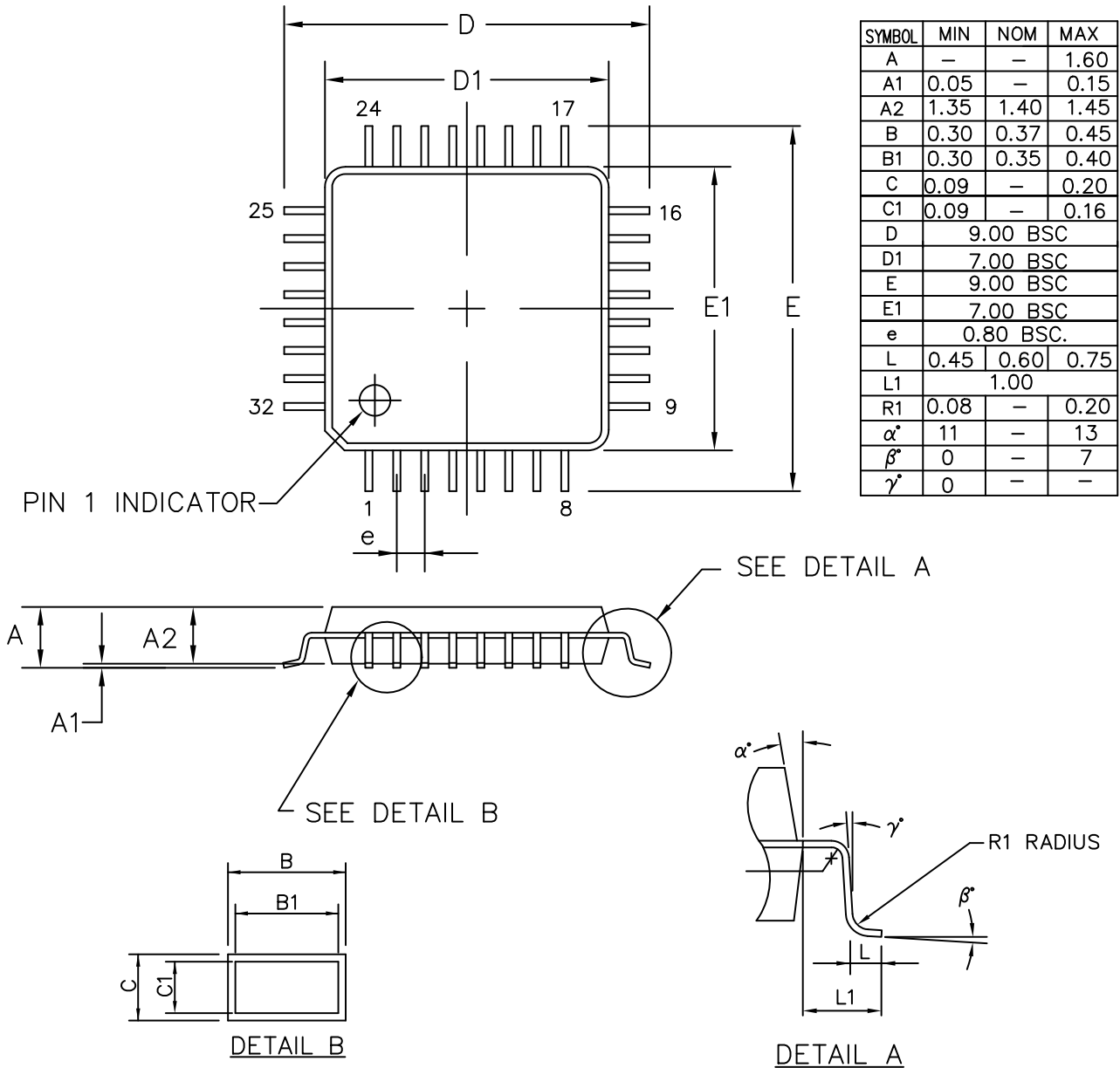
Figure 5. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

### Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D – Metastability and the ECLinPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1672/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLinPS
- AND8090/D – AC Characteristics of ECL Devices

**LQFP-32, 7x7**  
**CASE 561AB**  
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DATE 19 JUN 2008



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