

3.3V ECL 1:2 Differential Fanout Buffer MC100LVEL11

Description

The MC100LVEL11 is a differential 1:2 fanout buffer. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the LVEL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the LVEL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to $V_{\rm EE}$) the Q outputs will go LOW.

Features

- 330 ps Propagation Delay
- 5 ps Skew Between Outputs
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$ with $V_{EE} = -3.0 \text{ V}$ to -3.8 V
- Internal Input Pulldown Resistors on D, Pullup and Pulldown Resistors on D
- Q Output will Default LOW with Inputs Open or at V_{EE}
- These Devices are Pb-Free and are RoHS Compliant

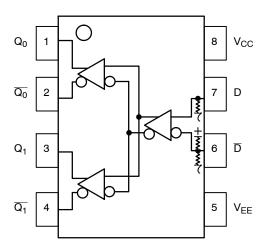


Figure 1. Logic Diagram and Pinout Assignment

1







SOIC-8 D SUFFIX CASE 751 TSSOP-8 DT SUFFIX CASE 948R

DFN8 MN SUFFIX CASE 506AA

MARKING DIAGRAMS







A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100LVEL11DG	SOIC-8 (Pb-Free)	98 Units/Tube
MC100LVEL11DR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel
MC100LVEL11DTG	TSSOP-8 (Pb-Free)	100 Units/Tube
MC100LVEL11DTR2G	TSSOP-8 (Pb-Free)	2500/Tape & Reel
MC100LVEL11MNR4G	DFN8 (Pb-Free)	1000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC100LVEL11

Table 1. PIN DESCRIPTION

Pin	Function
Q0, Q0 ; Q1, Q1	ECL Data Outputs
D, \overline{D}	ECL Data Inputs
V _{CC}	Positive Supply
V _{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. ATTRIBUTES

Charact	Value	
Internal Input Pulldown Resistor	75 kΩ	
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charge Device Model	> 4 KV > 400 V > 2 kV
Moisture Sensitivity, Indefinite Tir	ne Out of Drypack (Note 1) SOIC-8 TSSOP-8 DFN8	Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		63
Meets or exceeds JEDEC Spec B		

^{1.} For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	٧
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8 to 0	٧
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$\begin{aligned} & V_I \leq V_{CC} \\ & V_I \geq V_{EE} \end{aligned}$	6 to 0 -6 to 0	V
l _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +95	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
$\theta_{\sf JA}$	Thermal Resistance (Junction-to-Ambient)	0 lpfm 500 lpfm	SOIC-8 SOIC-8	190 130	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lpfm 500 lpfm	TSSOP-8 TSSOP-8	185 140	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T _{sol}	Wave Solder Pb-Free	<2 to 3 sec @ 260°C		265	°C
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

MC100LVEL11

Table 4. LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 3)

			-40°C			25°C			95°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		24	28		24	28		25	30	mA
V _{OH}	Output HIGH Voltage (Note 4)		2295	2420	2275	2345	2420	2275	2345	2420	mV
V _{OL}	Output LOW Voltage (Note 4)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V _{IH}		2135		2420	2135		2420	2135		2420	mV
V_{IL}		1490		1825	1490		1825	1490		1825	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8) $V_{pp} < 500 \text{ mV} \\ V_{pp} \geqq 500 \text{ mV}$	1.2 1.4		3.1 3.1	1.1		3.1 3.1	1.1		3.1 3.1	V V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current D D	0.5 -600			0.5 -600			0.5 -600			μ Α μ Α

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ± 0.3 V. 4. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.
- V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1.0 V.

Table 5. LVNECL DC CHARACTERISTICS $V_{CC} = 0.0 \text{ V}$; $V_{EE} = -3.3 \text{ V}$ (Note 6)

		−40°C		25°C		95°C					
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		24	28		24	28		25	30	mA
V _{OH}	Output HIGH Voltage (Note 7)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage (Note 7)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8) $V_{pp} < 500 \text{ mV} \\ V_{pp} \geqq 500 \text{ mV}$	-2.1 -1.9		-0.2 -0.2	-2.2 -2.0		-0.2 -0.2	-2.2 -2.0		-0.2 -0.2	V V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current D	0.5 -600			0.5 -600			0.5 -600			μ Α μ Α

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary ±0.3 V.
- Outputs are terminated through a 50 \(\Omega\) resistor to \(\V_{CC}\) 2.0 \(\V_{CM}\)
 V_{IHCMR} min varies 1:1 with \(\V_{EE}\), max varies 1:1 with \(\V_{CC}\). The \(\V_{IHCMR}\) range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between \(\V_{PP}\)min and 1.0 \(\V_{CC}\).

MC100LVEL11

Table 6. AC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$; $V_{EE} = 0.0 \text{ V}$ or $V_{CC} = 0.0 \text{ V}$; $V_{EE} = -3.3 \text{ V}$ (Note 9)

			-40°C		25°C			95°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	
f _{max}	Maximum Toggle Frequency					1.0					GHz	
t _{PLH} t _{PHL}	Propagation Delay to Output	235		385	255	330	405	285		435	ps	
t _{SKEW}	Within-Device Skew (Note 10) Device-to-Device (Note 11) Duty Cycle Skew (Note 12)		5 10	20 150 20		5 10	20 150 20		5 10	20 150 20	ps	
t _{JITTER}	Random Clock Jitter (RMS)					0.6					ps	
V_{PP}	Input Swing (Note 13)	200		1000	200		1000	200		1000	mV	
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	120		320	120	220	320	120		320	ps	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 9. VEE can vary ±0.3 V.
- 10. Within-device skew defined as identical transitions on similar paths through a device.
- 11. Device–to–device skew for identical transitions at identical $\dot{V_{CC}}$ levels.
- 12. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

 13. V_{PP}(min) is the minimum input swing for which AC parameters guaranteed. The device will function properly with input swings below 200 mV, however, AC delays may move outside of the specified range. The device has a DC gain of ≈40.

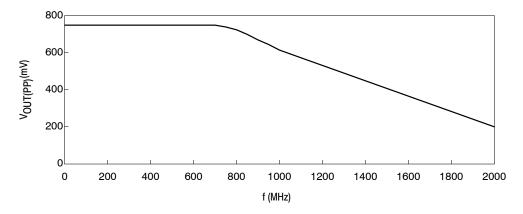


Figure 2. Output Swing versus Frequency

Resource Reference of Application Notes

AN1405/D ECL Clock Distribution Techniques AN1406/D Designing with PECL (ECL at +5.0 V) AN1503/D ECLinPS™ I/O SPiCE Modeling Kit AN1504/D Metastability and the ECLinPS Family AN1568/D Interfacing Between LVDS and ECL AN1672/D - The ECL Translator Guide

AND8001/D Odd Number Counters Design

AND8002/D Marking and Date Codes

Termination of ECL Logic Devices AND8020/D

AND8066/D Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

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DIMENSIONING AND TOLERANCING PER

PAD AS WELL AS THE TERMINALS.

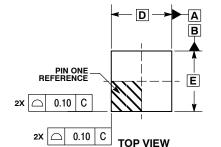
ASME Y14.5M, 1994 . CONTROLLING DIMENSION: MILLIMETERS. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED

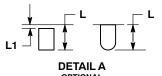


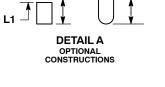


DFN8 2x2, 0.5P CASE 506AA **ISSUE F**

DATE 04 MAY 2016

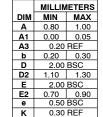




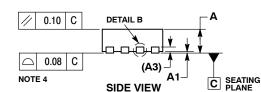


MOLD CMPD

EXPOSED Cu



NOTES



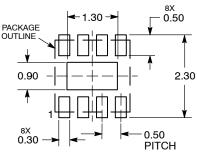
DETAIL B ALTERNATE CONSTRUCTIONS

RECOMMENDED SOLDERING FOOTPRINT*

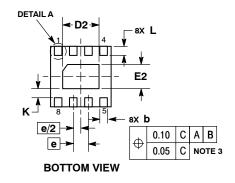
0.25

0.35

0.10



DIMENSIONS: MILLIMETERS



GENERIC MARKING DIAGRAM*



XX = Specific Device Code

= Date Code

= Pb-Free Device

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8, 2.0X2.0, 0.5MM PITCH		PAGE 1 OF 1		

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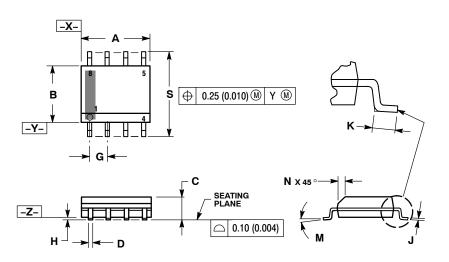
^{*}This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.





SOIC-8 NB CASE 751-07 **ISSUE AK**

DATE 16 FEB 2011



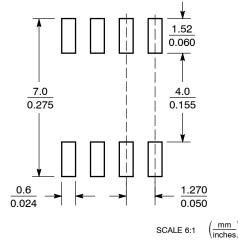
XS

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
М	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

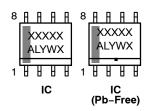
SOLDERING FOOTPRINT*

0.25 (0.010) M Z Y S



^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location = Wafer Lot

= Year = Work Week W = Pb-Free Package

XXXXXX XXXXXX AYWW AYWW H \mathbb{H} Discrete **Discrete** (Pb-Free)

XXXXXX = Specific Device Code = Assembly Location Α ww

= Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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SOIC-8 NB CASE 751-07 ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	7. BASE, #1 8. EMITTER, #1 STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
5. RXE 6. VEE 7. GND 8. ACC STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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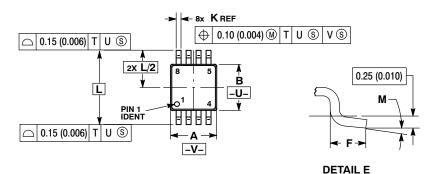
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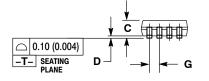


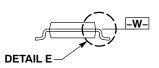


TSSOP-8 3.00x3.00x0.95 CASE 948R-02 **ISSUE A**

DATE 07 APR 2000







NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15

 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65	5 BSC 0.026 E		BSC
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6 °	0°	6°

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DESCRIPTION:	TSSOP-8 3.00x3.00x0.95		PAGE 1 OF 1

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