

# 5 V ECL ÷4 Divider

## MC10EL33, MC100EL33

### Description

The MC10EL/100EL33 is an integrated ÷4 divider. The differential clock inputs and the  $V_{BB}$  allow a differential, single-ended or AC coupled interface to the device. The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EL33's in a system.

The 100 Series contains temperature compensation.

### Features

- 650 ps Propagation Delay
- 4.0 GHz Toggle Frequency
- ESD Protection:
  - ◆ > 1 kV Human Body Model
  - ◆ > 100 V Machine Model
- PECL Mode Operating Range:  $V_{CC} = 4.2$  V to 5.7 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -4.2$  V to -5.7 V
- Internal Input Pulldown Resistors on CLK(s) and R.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity:
  - ◆ Level 1 for SOIC-8 NB
  - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in. Oxygen Index: 28 to 34
- Transistor Count = 95 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



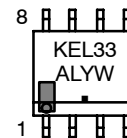
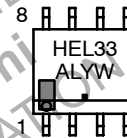
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SOIC-8 NB  
D SUFFIX  
CASE 751-07

### MARKING DIAGRAM



H = MC10  
K = MC100  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

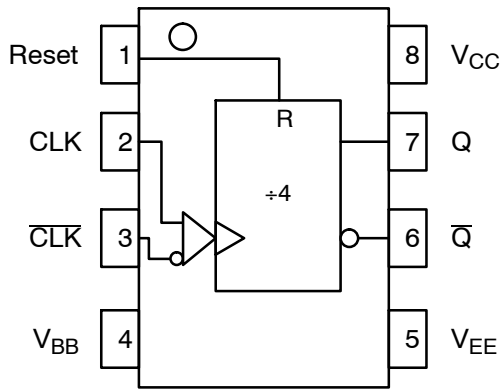
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device      | Package             | Shipping        |
|-------------|---------------------|-----------------|
| MC10EL33DG  | SOIC-8<br>(Pb-Free) | 98 Units / Tube |
| MC100EL33DG | SOIC-8<br>(Pb-Free) | 98 Units / Tube |

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**Table 1. PIN DESCRIPTION**

| Pin                          | Function                 |
|------------------------------|--------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Clock Inputs*        |
| Reset                        | ECL Asynch Reset*        |
| Q, $\overline{\text{Q}}$     | ECL Data Outputs         |
| $V_{\text{BB}}$              | Reference Voltage Output |
| $V_{\text{CC}}$              | Positive Supply          |
| $V_{\text{EE}}$              | Negative Supply          |

\*Pins will default low when left open.

**Figure 1. Logic Diagram and Pinout Assignment**

**Table 2. MAXIMUM RATINGS**

| Symbol               | Parameter  | Condition 1  | Condition 2  | Rating      | Unit                        |
|----------------------|--|--|--|-------------|-----------------------------|
| $V_{\text{CC}}$      | PECL Mode Power Supply                             | $V_{\text{EE}} = 0 \text{ V}$                                  |  | 8           | V                           |
| $V_{\text{EE}}$      | NECL Mode Power Supply                             | $V_{\text{CC}} = 0 \text{ V}$                                  |  | -8          | V                           |
| $V_{\text{I}}$       | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{\text{EE}} = 0 \text{ V}$<br>$V_{\text{CC}} = 0 \text{ V}$ | $V_{\text{I}} \leq V_{\text{CC}}$<br>$V_{\text{I}} \geq V_{\text{EE}}$ | 6<br>-6     | V                           |
| $I_{\text{out}}$     | Output Current                                     | Continuous<br>Surge  |  | 50<br>100   | mA                          |
| $I_{\text{BB}}$      | $V_{\text{BB}}$ Sink/Source                        |  |  | $\pm 0.5$   | mA                          |
| $T_{\text{A}}$       | Operating Temperature Range                        |  |  | -40 to +85  | $^{\circ}\text{C}$          |
| $T_{\text{stg}}$     | Storage Temperature Range                          |  |  | -65 to +150 | $^{\circ}\text{C}$          |
| $\theta_{\text{JA}}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm   | SOIC-8 NB<br>SOIC-8 NB   | 190<br>130  | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{\text{JC}}$ | Thermal Resistance (Junction-to-Case)              | Standard Board   | SOIC-8 NB  | 41 to 44    | $^{\circ}\text{C}/\text{W}$ |
| $T_{\text{sol}}$     | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260 $^{\circ}\text{C}$                          |  | 265         | $^{\circ}\text{C}$          |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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**Table 3. 10EL SERIES PECL DC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

| Symbol      | Characteristic   | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
|             |  | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current   |       | 27   | 33   |      | 27   | 33   |      | 27   | 33   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)   | 3920  | 4010 | 4110 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)  | 3050  | 3200 | 3350 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 3770  |      | 4110 | 3870 |      | 4190 | 3940 |      | 4280 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 3050  |      | 3500 | 3050 |      | 3520 | 3050 |      | 3555 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 3.57  |      | 3.7  | 3.65 |      | 3.75 | 3.69 |      | 3.81 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.5   |      | 4.6  | 2.5  |      | 4.6  | 2.5  |      | 4.6  | V             |
| $I_{IH}$    | Input HIGH Current   |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |      |      | 0.5  |      |      | 0.3  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpn.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $+0.25\text{ V} / -0.5\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

**Table 4. 10EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

| Symbol      | Characteristic   | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |  | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current   |       | 27    | 33    |       | 27    | 33    |       | 27    | 33    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)   | -1080 | -990  | -890  | -980  | -895  | -810  | -910  | -815  | -720  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)  | -1950 | -1800 | -1650 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | -1230 |       | -890  | -1130 |       | -810  | -1060 |       | -720  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | -1950 |       | -1500 | -1950 |       | -1480 | -1950 |       | -1445 | mV            |
| $V_{BB}$    | Output Voltage Reference   | -1.43 |       | -1.30 | -1.35 |       | -1.25 | -1.31 |       | -1.19 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.5  |       | -0.4  | -2.5  |       | -0.4  | -2.5  |       | -0.4  | V             |
| $I_{IH}$    | Input HIGH Current   |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |       |       | 0.5   |       |       | 0.3   |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpn.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $+0.25\text{ V} / -0.5\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

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**Table 5. 100EL SERIES PECL DC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

| Symbol      | Characteristic   | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
|             |  | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current   |       | 27   | 33   |      | 27   | 33   |      | 31   | 37   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)   | 3915  | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)  | 3170  | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 3835  |      | 4120 | 3835 |      | 4120 | 3835 |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 3190  |      | 3525 | 3190 |      | 3525 | 3190 |      | 3525 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 3.62  |      | 3.74 | 3.62 |      | 3.74 | 3.62 |      | 3.74 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.5   |      | 4.6  | 2.5  |      | 4.6  | 2.5  |      | 4.6  | V             |
| $I_{IH}$    | Input HIGH Current   |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

**Table 6. 100EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

| Symbol      | Characteristic   | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |  | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current   |       | 27    | 33    |       | 27    | 33    |       | 31    | 37    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)   | -1085 | -1005 | -880  | -1025 | -955  | -880  | -1025 | -955  | -880  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)  | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | -1165 |       | -880  | -1165 |       | -880  | -1165 |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | -1810 |       | -1475 | -1810 |       | -1475 | -1810 |       | -1475 | mV            |
| $V_{BB}$    | Output Voltage Reference   | -1.38 |       | -1.26 | -1.38 |       | -1.26 | -1.38 |       | -1.26 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.5  |       | -0.4  | -2.5  |       | -0.4  | -2.5  |       | -0.4  | V             |
| $I_{IH}$    | Input HIGH Current   |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

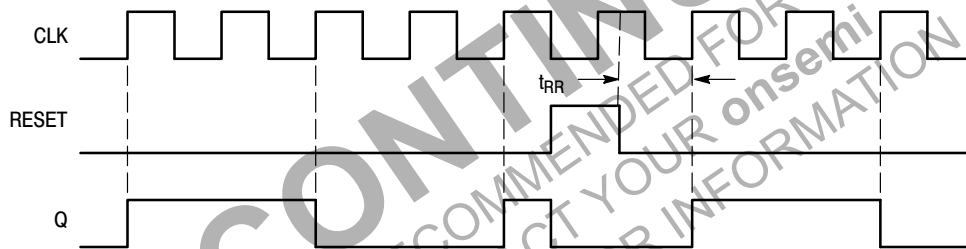
# MC10EL33, MC100EL33

**Table 7. AC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

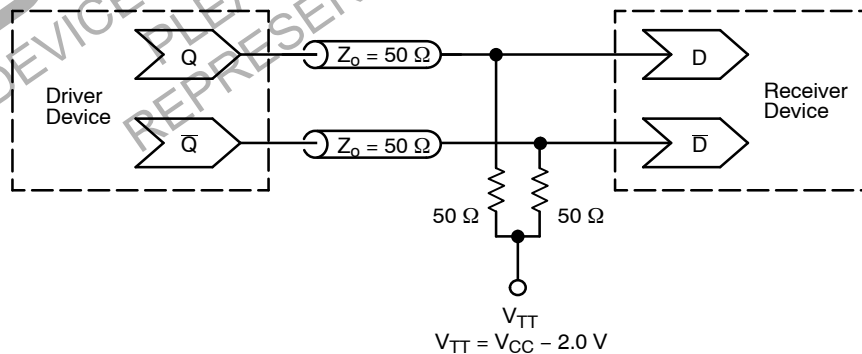
| Symbol                               | Characteristic                              | -40°C      |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|--------------------------------------|---|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                                      |   | Min        | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| f <sub>max</sub>                     | Maximum Toggle Frequency                    | 3.4        | 4.2        |            | 3.8        | 4.2        |            | 3.8        | 4.2        |            | GHz  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLK to Q<br>Reset to Q | 560<br>400 | 670<br>540 | 860<br>700 | 610<br>460 | 700<br>550 | 810<br>660 | 640<br>570 | 740<br>480 | 840<br>670 | ps   |
| t <sub>RR</sub>                      | Set/Reset Recovery                          | 400        | 200        |            | 400        | 200        |            | 400        | 200        |            | ps   |
| V <sub>PP</sub>                      | Input Swing (Note 2)                        | 150        |            | 1000       | 150        |            | 1000       | 150        |            | 1000       | mV   |
| t <sub>JITTER</sub>                  | Cycle-to-Cycle Jitter                       |            | 1.0        |            |            | 1.0        |            |            | 1.0        |            | ps   |
| t <sub>r</sub><br>t <sub>f</sub>     | Output Rise/Fall Times Q (20%–80%)          | 100        | 225        | 350        | 100        | 225        | 350        | 100        | 225        | 350        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 10 Series:  $V_{EE}$  can vary +0.25 V / -0.5 V.  
100 Series:  $V_{EE}$  can vary +0.8 V / -0.5 V.
- $V_{PP}(\text{min})$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 2. Timing Diagram**



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

## MC10EL33, MC100EL33

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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