

# 14-Bit Binary Counter

## MC14020B

The MC14020B 14-stage binary counter is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

### Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

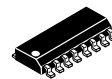
| Symbol            | Parameter   | Value                  | Unit        |
|-------------------|---|------------------------|-------------|
| $V_{DD}$          | DC Supply Voltage Range                           | -0.5 to +18.0          | V           |
| $V_{in}, V_{out}$ | Input or Output Voltage Range (DC or Transient)   | -0.5 to $V_{DD} + 0.5$ | V           |
| $I_{in}, I_{out}$ | Input or Output Current (DC or Transient) per Pin | $\pm 10$               | mA          |
| $P_D$             | Power Dissipation, per Package (Note 1)           | 500                    | mW          |
| $T_A$             | Ambient Temperature Range                         | -55 to +125            | $^{\circ}C$ |
| $T_{stg}$         | Storage Temperature Range                         | -65 to +150            | $^{\circ}C$ |
| $T_L$             | Lead Temperature (8-Second Soldering)             | 260                    | $^{\circ}C$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}C$  From 65  $^{\circ}C$  To 125  $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

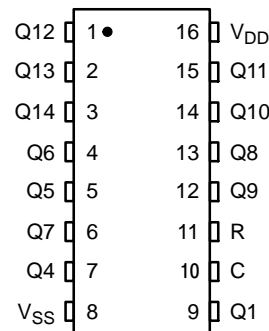


SOIC-16  
D SUFFIX  
CASE 751B

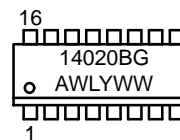


TSSOP-16  
DT SUFFIX  
CASE 948F

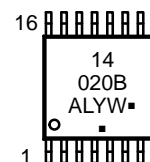
### PIN ASSIGNMENT



### MARKING DIAGRAMS



SOIC-16



TSSOP-16

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Indicator

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

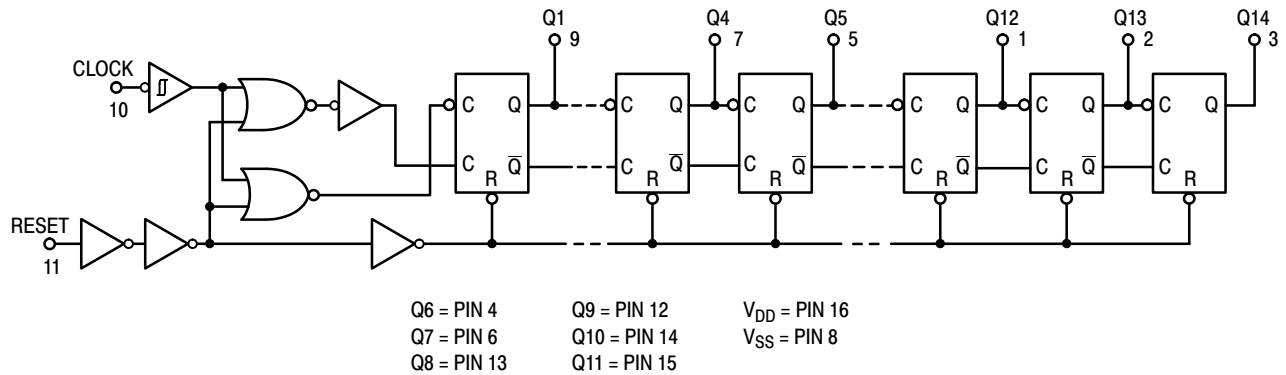
# MC14020B

## TRUTH TABLE

| Clock | Reset | Output State          |
|-------|-------|-----------------------|
|       | 0     | No Change             |
|       | 0     | Advance to Next State |
| X     | 1     | All Outputs are Low   |

X = Don't Care

## LOGIC DIAGRAM



## ORDERING INFORMATION

| Device         | Package              | Shipping <sup>†</sup>    |
|----------------|----------------------|--------------------------|
| MC14020BDR2G   | SOIC-16<br>(Pb-Free) | 2500 Units / Tape & Reel |
| NLV14020BDR2G* | SOIC-16<br>(Pb-Free) | 2500 Units / Tape & Reel |

## DISCONTINUED (Note 2)

|             |                       |                 |
|-------------|-----------------------|-----------------|
| MC14020BDG  | SOIC-16<br>(Pb-Free)  | 48 Units / Rail |
| MC14020BDTG | TSSOP-16<br>(Pb-Free) | 96 Units / Rail |

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

2. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# MC14020B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

| Characteristic  | Symbol  | V <sub>DD</sub><br>Vdc | -55 °C  |       | 25 °C |                 |      | 125 °C |       | Unit |   |
|---|---|------------------------|---|-------|-------|-----------------|------|--------|-------|------|---|
|   |   |                        | Min   | Max   | Min   | Typ<br>(Note 3) | Max  | Min    | Max   |      |   |
| Output Voltage<br>V <sub>in</sub> = V <sub>DD</sub> or 0  | "0" Level<br>V <sub>OL</sub>  | 5.0                    | -   | 0.05  | -     | 0               | 0.05 | -      | 0.05  | Vdc  |   |
|   |   | 10                     | -   | 0.05  | -     | 0               | 0.05 | -      | 0.05  |      |   |
|   |   | 15                     | -   | 0.05  | -     | 0               | 0.05 | -      | 0.05  |      |   |
|   | "1" Level<br>V <sub>in</sub> = 0 or V <sub>DD</sub>   | V <sub>OH</sub>        | 5.0   | 4.95  | -     | 4.95            | 5.0  | -      | 4.95  |      | - |
|   |   |                        | 10  | 9.95  | -     | 9.95            | 10   | -      | 9.95  |      | - |
|   |   |                        | 15  | 14.95 | -     | 14.95           | 15   | -      | 14.95 |      | - |
| Input Voltage<br>(V <sub>O</sub> = 4.5 or 0.5 Vdc)<br>(V <sub>O</sub> = 9.0 or 1.0 Vdc)<br>(V <sub>O</sub> = 13.5 or 1.5 Vdc)                       | "0" Level<br>V <sub>IL</sub>  | 5.0                    | -   | 1.5   | -     | 2.25            | 1.5  | -      | 1.5   | Vdc  |   |
|   |   | 10                     | -   | 3.0   | -     | 4.50            | 3.0  | -      | 3.0   |      |   |
|   |   | 15                     | -   | 4.0   | -     | 6.75            | 4.0  | -      | 4.0   |      |   |
|   | "1" Level<br>(V <sub>O</sub> = 0.5 or 4.5 Vdc)<br>(V <sub>O</sub> = 1.0 or 9.0 Vdc)<br>(V <sub>O</sub> = 1.5 or 13.5 Vdc) | V <sub>IH</sub>        | 5.0   | 3.5   | -     | 3.5             | 2.75 | -      | 3.5   |      | - |
|   |   |                        | 10  | 7.0   | -     | 7.0             | 5.50 | -      | 7.0   |      | - |
|   |   |                        | 15  | 11    | -     | 11              | 8.25 | -      | 11    |      | - |
| Output Drive Current<br>(V <sub>OH</sub> = 2.5 Vdc)<br>(V <sub>OH</sub> = 4.6 Vdc)<br>(V <sub>OH</sub> = 9.5 Vdc)<br>(V <sub>OH</sub> = 13.5 Vdc)   | Source<br>I <sub>OH</sub>   | 5.0                    | -3.0  | -     | -2.4  | -4.2            | -    | -1.7   | -     | mAdc |   |
|   |   | 5.0                    | -0.64   | -     | -0.51 | -0.88           | -    | -0.36  | -     |      |   |
|   |   | 10                     | -1.6  | -     | -1.3  | -2.25           | -    | -0.9   | -     |      |   |
|   | Sink<br>I <sub>OL</sub>   | 15                     | 5.0   | 0.64  | -     | 0.51            | 0.88 | -      | 0.36  |      | - |
|   |   |                        | 10  | 1.6   | -     | 1.3             | 2.25 | -      | 0.9   |      | - |
|   |   |                        | 15  | 4.2   | -     | 3.4             | 8.8  | -      | 2.4   |      | - |
| Input Current   | I <sub>in</sub>   | 15                     | -   | ±0.1  | -     | ±0.00001        | ±0.1 | -      | ±1.0  | µAdc |   |
| Input Capacitance<br>(V <sub>in</sub> = 0)  | C <sub>in</sub>   | -                      | -   | -     | -     | 5.0             | 7.5  | -      | -     | pF   |   |
| Quiescent Current<br>(Per Package)  | I <sub>DD</sub>   | 5.0                    | -   | 5.0   | -     | 0.005           | 5.0  | -      | 150   | µAdc |   |
|   |   | 10                     | -   | 10    | -     | 0.010           | 10   | -      | 300   |      |   |
|   |   | 15                     | -   | 20    | -     | 0.015           | 20   | -      | 600   |      |   |
| Total Supply Current (Notes 4 & 5)<br>(Dynamic plus Quiescent,<br>Per Package)<br>(C <sub>L</sub> = 50 pF on all outputs, all<br>buffers switching) | I <sub>T</sub>  | 5.0                    | I <sub>T</sub> = (0.42 µA/kHz)f + I <sub>DD</sub> |       |       |                 |      |        |       | µAdc |   |
|   |   | 10                     | I <sub>T</sub> = (0.85 µA/kHz)f + I <sub>DD</sub> |       |       |                 |      |        |       |      |   |
|   |   | 15                     | I <sub>T</sub> = (1.43 µA/kHz)f + I <sub>DD</sub> |       |       |                 |      |        |       |      |   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
- The formulas given are for the typical characteristics only at 25 °C.
- To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

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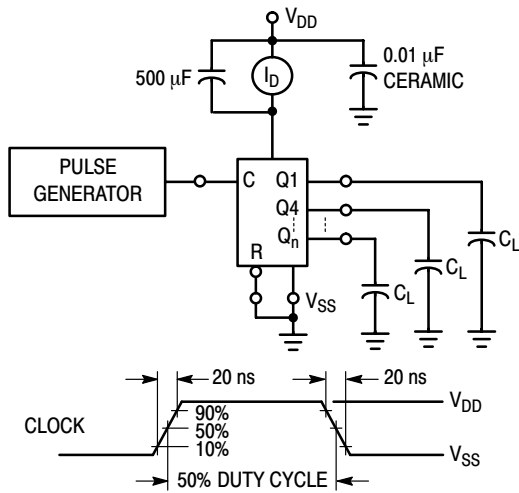
## SWITCHING CHARACTERISTICS (Note 6) ( $C_L = 50 \text{ pF}$ , $T_A = 25 \text{ }^\circ\text{C}$ )

| Characteristic   | Symbol                   | $V_{DD}$<br>Vdc | Min                | Typ<br>(Note 7)    | Max                  | Unit |
|--|--------------------------|-----------------|--------------------|--------------------|----------------------|------|
| Output Rise and Fall Time<br>$t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$<br>$t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$<br>$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$          | $t_{TLH}$ ,<br>$t_{THL}$ | 5.0<br>10<br>15 | –<br>–<br>–        | 100<br>50<br>40    | 200<br>100<br>80     | ns   |
| Propagation Delay Time<br>Clock to Q1<br>$t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 175 \text{ ns}$<br>$t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$<br>$t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$ | $t_{PLH}$ ,<br>$t_{PHL}$ | 5.0<br>10<br>15 | –<br>–<br>–        | 260<br>115<br>80   | 520<br>230<br>160    | ns   |
| Clock to Q14<br>$t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 1735 \text{ ns}$<br>$t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 772 \text{ ns}$<br>$t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 535 \text{ ns}$                       |                          | 5.0<br>10<br>15 | –<br>–<br>–        | 1820<br>805<br>560 | 3900<br>1725<br>1200 | ns   |
| Propagation Delay Time<br>Reset to $Q_n$<br>$t_{PHL} = (1.7 \text{ ns/pF}) C_L + 285 \text{ ns}$<br>$t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$<br>$t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$                                 | $t_{PHL}$                | 5.0<br>10<br>15 | –<br>–<br>–        | 370<br>155<br>115  | 740<br>310<br>230    | ns   |
| Clock Pulse Width  | $t_{WH}$                 | 5.0<br>10<br>15 | 500<br>165<br>125  | 140<br>55<br>38    | –<br>–<br>–          | ns   |
| Clock Pulse Frequency  | $f_{max}$                | 5.0<br>10<br>15 | 1.0<br>3.0<br>4.0  | 2.0<br>6.0<br>8.0  | –<br>–<br>–          | MHz  |
| Clock Rise and Fall Time   | $t_{TLH}$ , $t_{THL}$    | 5.0<br>10<br>15 | No Limit           |                    |                      | –    |
| Reset Pulse Width  | $t_{WL}$                 | 5.0<br>10<br>15 | 3000<br>550<br>420 | 320<br>120<br>80   | –<br>–<br>–          | ns   |
| Reset Recovery Time  | $t_{rec}$                | 5.0<br>10<br>15 | –<br>–<br>–        | 65<br>25<br>15     | 130<br>50<br>30      | ns   |

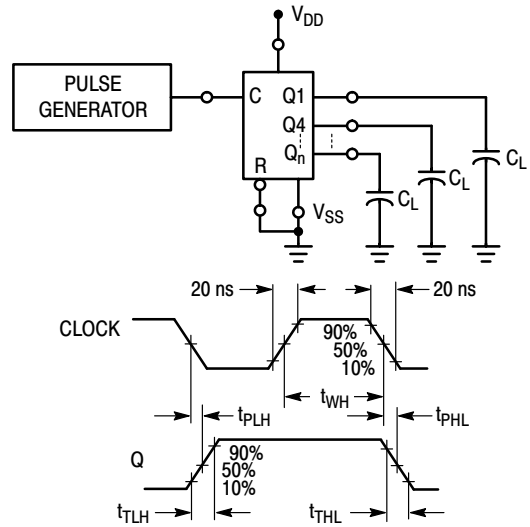
6. The formulas given are for the typical characteristics only at 25 °C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

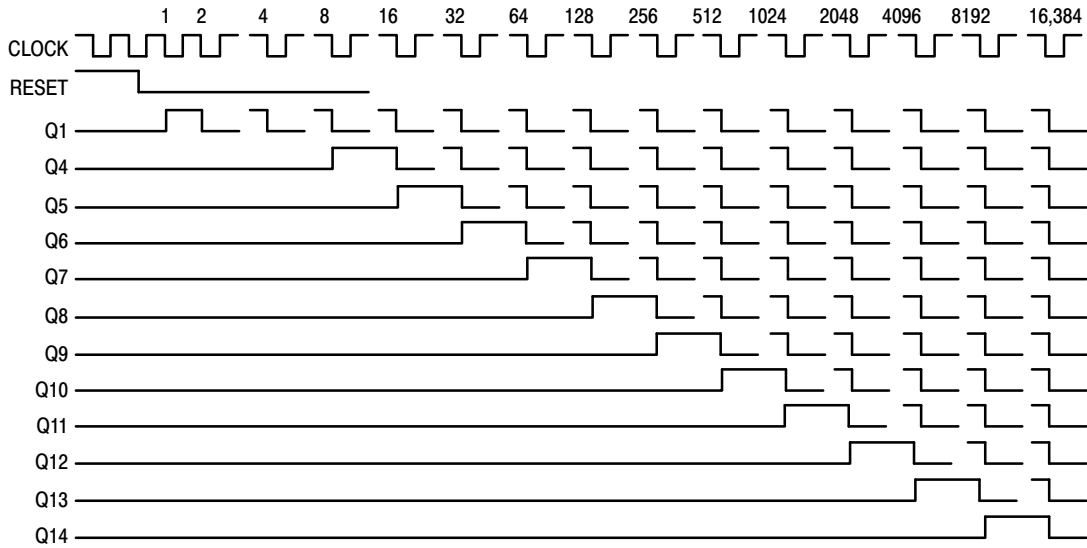
# MC14020B



**Figure 1. Power Dissipation Test Circuit and Waveform**



**Figure 2. Switching Time Test Circuit and Waveforms**



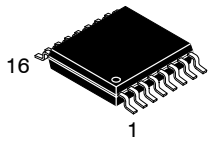
**Figure 3. Timing Diagram**

# MC14020B

## REVISION HISTORY

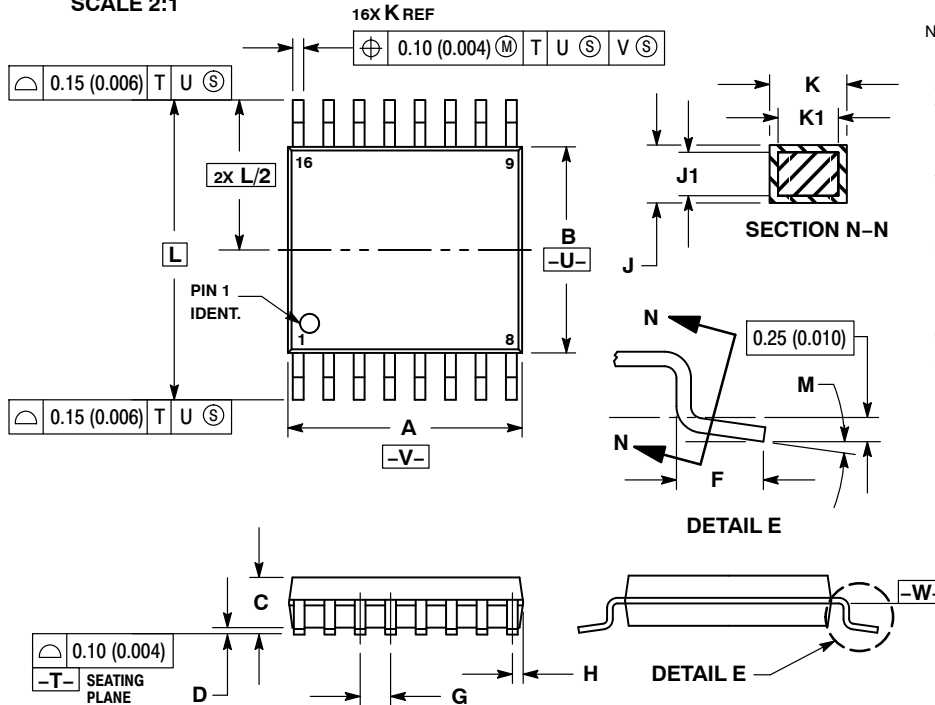
| Revision | Description of Changes   | Date      |
|----------|--|-----------|
| 10       | Rebranded the Data Sheet to <b>onsemi</b> format.<br>MC14020BDG and MC14020BDTG OPNs Marked as Discontinued. | 8/25/2025 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



TSSOP-16 WB  
CASE 948F  
ISSUE B

DATE 19 OCT 2006

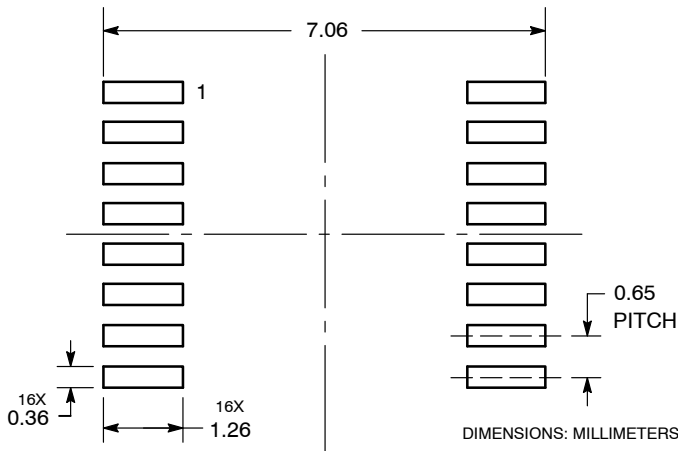


NOTES:

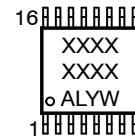
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



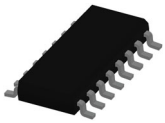
- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |             |  |
|------------------|-------------|--|
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| DESCRIPTION:     | TSSOP-16    | PAGE 1 OF 1  |

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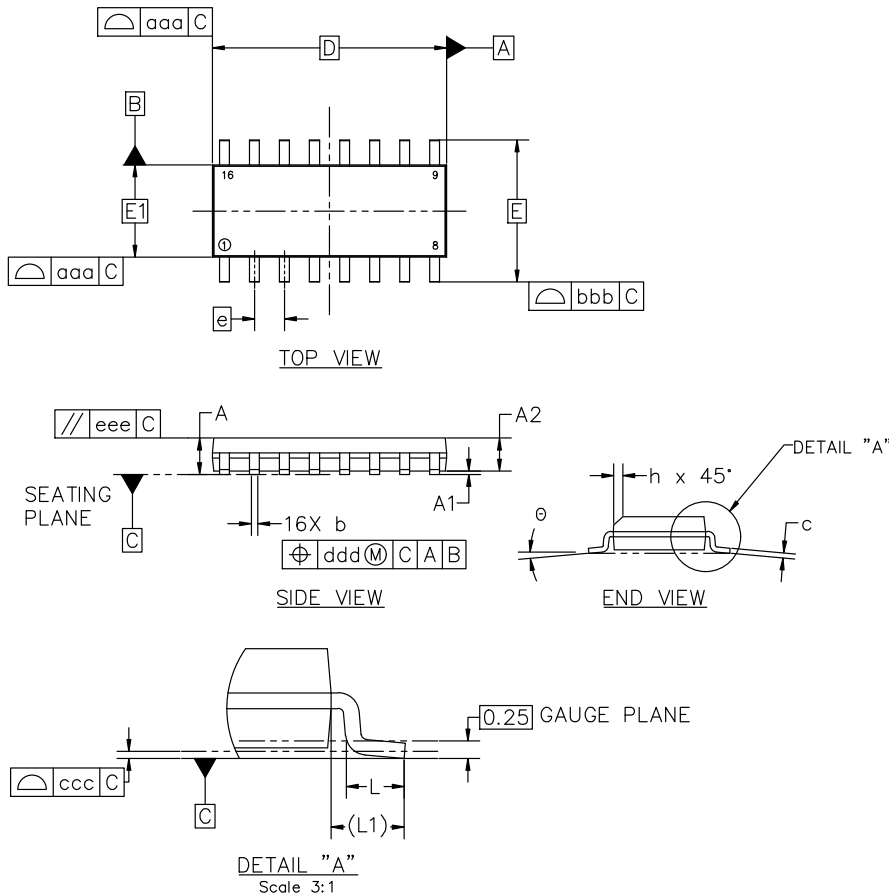


SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

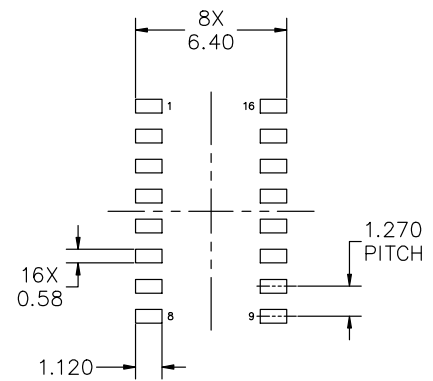
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS                    |          |      |      |
|--------------------------------|----------|------|------|
| DIM                            | MIN      | NOM  | MAX  |
| A                              | 1.35     | 1.55 | 1.75 |
| A1                             | 0.10     | 0.18 | 0.25 |
| A2                             | 1.25     | 1.37 | 1.50 |
| b                              | 0.35     | 0.42 | 0.49 |
| c                              | 0.19     | 0.22 | 0.25 |
| D                              | 9.90 BSC |      |      |
| E                              | 6.00 BSC |      |      |
| E1                             | 3.90 BSC |      |      |
| e                              | 1.27 BSC |      |      |
| h                              | 0.25     | ---  | 0.50 |
| L                              | 0.40     | 0.83 | 1.25 |
| L1                             | 1.05 REF |      |      |
| θ                              | 0°       | ---  | 7°   |
| TOLERANCE OF FORM AND POSITION |          |      |      |
| aaa                            | 0.10     |      |      |
| bbb                            | 0.20     |      |      |
| ccc                            | 0.10     |      |      |
| ddd                            | 0.25     |      |      |
| eee                            | 0.10     |      |      |



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

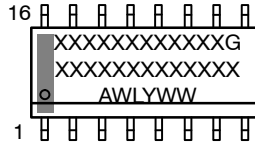
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|-------------------------|-------------------------------------|--|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42566B</b>                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-16 9.90X3.90X1.37 1.27P</b> | <b>PAGE 1 OF 2</b>   |

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**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

DATE 18 OCT 2024

**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

|   |   |   |   |
|---|---|---|---|
| <p><b>STYLE 1:</b></p> <p>PIN 1. COLLECTOR<br/> 2. BASE<br/> 3. EMITTER<br/> 4. NO CONNECTION<br/> 5. EMITTER<br/> 6. BASE<br/> 7. COLLECTOR<br/> 8. COLLECTOR<br/> 9. BASE<br/> 10. EMITTER<br/> 11. NO CONNECTION<br/> 12. EMITTER<br/> 13. BASE<br/> 14. COLLECTOR<br/> 15. EMITTER<br/> 16. COLLECTOR</p>                           | <p><b>STYLE 2:</b></p> <p>PIN 1. CATHODE<br/> 2. ANODE<br/> 3. NO CONNECTION<br/> 4. CATHODE<br/> 5. CATHODE<br/> 6. NO CONNECTION<br/> 7. ANODE<br/> 8. CATHODE<br/> 9. CATHODE<br/> 10. ANODE<br/> 11. NO CONNECTION<br/> 12. CATHODE<br/> 13. CATHODE<br/> 14. NO CONNECTION<br/> 15. ANODE<br/> 16. CATHODE</p> | <p><b>STYLE 3:</b></p> <p>PIN 1. COLLECTOR, DYE #1<br/> 2. BASE, #1<br/> 3. EMITTER, #1<br/> 4. COLLECTOR, #1<br/> 5. COLLECTOR, #2<br/> 6. BASE, #2<br/> 7. EMITTER, #2<br/> 8. COLLECTOR, #2<br/> 9. COLLECTOR, #3<br/> 10. BASE, #3<br/> 11. EMITTER, #3<br/> 12. COLLECTOR, #3<br/> 13. COLLECTOR, #4<br/> 14. BASE, #4<br/> 15. EMITTER, #4<br/> 16. COLLECTOR, #4</p>   | <p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR, DYE #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #3<br/> 6. COLLECTOR, #3<br/> 7. COLLECTOR, #4<br/> 8. COLLECTOR, #4<br/> 9. BASE, #4<br/> 10. EMITTER, #4<br/> 11. BASE, #3<br/> 12. EMITTER, #3<br/> 13. BASE, #2<br/> 14. EMITTER, #2<br/> 15. BASE, #1<br/> 16. EMITTER, #1</p> |
| <p><b>STYLE 5:</b></p> <p>PIN 1. DRAIN, DYE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. DRAIN, #3<br/> 6. DRAIN, #3<br/> 7. DRAIN, #4<br/> 8. DRAIN, #4<br/> 9. GATE, #4<br/> 10. SOURCE, #4<br/> 11. GATE, #3<br/> 12. SOURCE, #3<br/> 13. GATE, #2<br/> 14. SOURCE, #2<br/> 15. GATE, #1<br/> 16. SOURCE, #1</p> | <p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE<br/> 2. CATHODE<br/> 3. CATHODE<br/> 4. CATHODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. CATHODE<br/> 8. CATHODE<br/> 9. ANODE<br/> 10. ANODE<br/> 11. ANODE<br/> 12. ANODE<br/> 13. ANODE<br/> 14. ANODE<br/> 15. ANODE<br/> 16. ANODE</p>                                 | <p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE N-CH<br/> 2. COMMON DRAIN (OUTPUT)<br/> 3. COMMON DRAIN (OUTPUT)<br/> 4. GATE P-CH<br/> 5. COMMON DRAIN (OUTPUT)<br/> 6. COMMON DRAIN (OUTPUT)<br/> 7. COMMON DRAIN (OUTPUT)<br/> 8. SOURCE P-CH<br/> 9. SOURCE P-CH<br/> 10. COMMON DRAIN (OUTPUT)<br/> 11. COMMON DRAIN (OUTPUT)<br/> 12. COMMON DRAIN (OUTPUT)<br/> 13. GATE N-CH<br/> 14. COMMON DRAIN (OUTPUT)<br/> 15. COMMON DRAIN (OUTPUT)<br/> 16. SOURCE N-CH</p> |   |

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| <b>DESCRIPTION:</b>     | <b>SOIC-16 9.90X3.90X1.37 1.27P</b> | <b>PAGE 2 OF 2</b>  |

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