onsemi

Quad Analog Switch/Quad Multiplexer

MC14066B

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

Features

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON}, Use The HC4066 High-Speed CMOS Device
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

SOIC-14 **D SUFFIX** **CASE 751A**	**SOEIAJ-14** **F SUFFIX** **CASE 965**	**TSSOP-14** **DT SUFFIX** **CASE 948G**

PIN ASSIGNMENT

IN 1	1	14	V$_{DD}$
OUT 1	2	13	CONTROL 1
OUT 2	3	12	CONTROL 4
IN 2	4	11	IN 4
CONTROL 2	5	10	OUT 4
CONTROL 3	6	9	OUT 3
V$_{SS}$	7	8	IN 3

MARKING DIAGRAMS

14 14066BG AWLYWW 1

SOIC-14

14 MC14066B ALYWG 1

SOEIAJ-14

14 14 066B ALYW▪
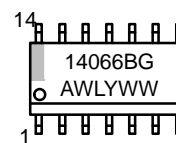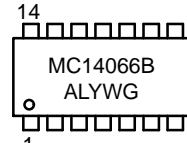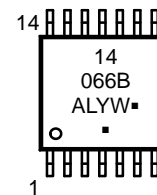
TSSOP-14

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb-Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (Voltages Referenced to V$_{SS}$)

Symbol	Parameter	Value	Unit
V$_{DD}$	DC Supply Voltage Range	−0.5 to +18.0	V
V$_{in}$, V$_{out}$	Input or Output Voltage Range (DC or Transient)	−0.5 to V$_{DD}$ + 0.5	V
I$_{in}$	Input Current (DC or Transient) per Control Pin	±10	mA
I$_{SW}$	Switch Through Current	±25	mA
P$_D$	Power Dissipation, per Package (Note 1)	500	mW
T$_A$	Ambient Temperature Range	−55 to +125	°C
T$_{stg}$	Storage Temperature Range	−65 to +150	°C
T$_L$	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
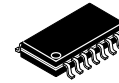1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65 °C To 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V$_{in}$ and V$_{out}$ should be constrained to the range V$_{SS}$ ≤ (V$_{in}$ or V$_{out}$) ≤ V$_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V$_{SS}$ or V$_{DD}$). Unused outputs must be left open.

ORDERING INFORMATION
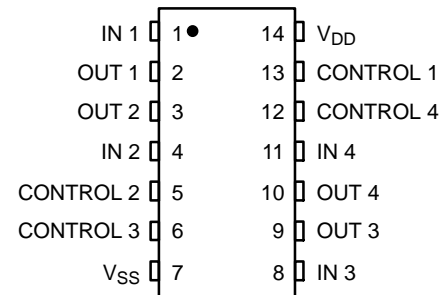
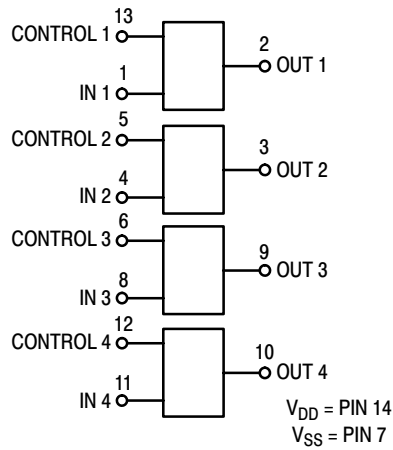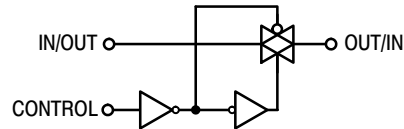See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.
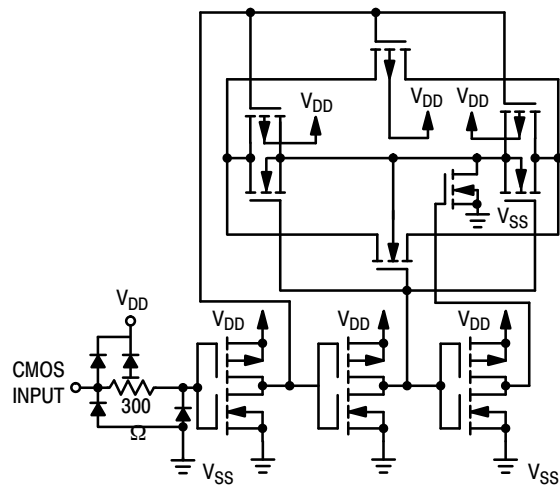
MC14066B

BLOCK DIAGRAM

CONTROL 1 — 13
IN 1 — 1
OUT 1 — 2

CONTROL 2 — 5
IN 2 — 4
OUT 2 — 3

CONTROL 3 — 6
IN 3 — 8
OUT 3 — 9

CONTROL 4 — 12
IN 4 — 11
OUT 4 — 10

V_{DD} = PIN 14
V_{SS} = PIN 7

LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)

IN/OUT   OUT/IN

CONTROL

Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)

MC14066B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	−55 °C Min	−55 °C Max	25 °C Min	25 °C Typ (Note 2)	25 °C Max	125 °C Min	125 °C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{SS} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500$ mV [3]	– – –	0.25 0.5 1.0	– – –	0.005 0.010 0.015	0.25 0.5 1.0	– – –	7.5 15 30	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	$T_A = 25$ °C only The channel component, $(V_{in} − V_{out})/R_{on}$, is not included.)	Typical			(0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.36 µA/kHz) f + I_{DD}				µA
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
High-Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Capacitance	C_{in}	–		–	–	–	5.0	7.5	–	–	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	$V_{p–p}$
Recommended Static or Dynamic Voltage Across the Switch (Note 3) (Figure 1)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0 V, No Load	–	–	–	10	–	–	–	µV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq 500$ mV [3], $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	– – –	800 400 220	– – –	250 120 80	1050 500 280	– – –	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		– – –	70 50 45	– – –	25 10 10	70 50 45	– – –	135 95 65	Ω
Off-Channel Leakage Current (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	–	±100	–	±0.05	±100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	Switch Off	–	–	–	10	15	–	–	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	– –		–	–	–	0.47	–	–	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
3. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (Note 4) (C_L = 50 pF, T_A = 25 °C unless otherwise noted.)

Characteristic		Symbol	V_{DD} Vdc	Min	Typ (Note 5)	Max	Unit
Propagation Delay Times V_{SS} = 0 Vdc Input to Output (R_L = 10 kΩ) t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		t_{PLH}, t_{PHL}	 5.0 10 15	 – – –	 20 10 7.0	 40 20 15	ns
Control to Output (R_L = 1 kΩ) (Figure 2) Output "1" to High Impedance		t_{PHZ}	 5.0 10 15	 – – –	 40 35 30	 80 70 60	ns
Output "0" to High Impedance		t_{PLZ}	5.0 10 15	– – –	40 35 30	80 70 60	ns
High Impedance to Output "1"		t_{PZH}	5.0 10 15	– – –	60 20 15	120 40 30	ns
High Impedance to Output "0"		t_{PZL}	5.0 10 15	– – –	60 20 15	120 40 30	ns
Second Harmonic Distortion V_{SS} = – 5 Vdc (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)		–	5.0	–	0.1	–	%
Bandwidth (Switch ON) (Figure 3) V_{SS} = – 5 Vdc (R_L = 1 kΩ, 20 Log (V_{out}/V_{in}) = – 3 dB, C_L = 50 pF, V_{in} = 5 $V_{p–p}$)		–	5.0	–	65	–	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = – 5 Vdc (V_{in} = 5 $V_{p–p}$, R_L = 1 kΩ, f_{in} = 1.0 MHz) (Figure 3)		–	5.0	–	– 50	–	dB
Channel Separation (Figure 4) V_{SS} = – 5 Vdc (V_{in} = 5 $V_{p–p}$, R_L = 1 kΩ, f_{in} = 8.0 MHz) (Switch A ON, Switch B OFF)		–	5.0	–	– 50	–	dB
Crosstalk, Control Input to Signal Output (Figure 5) V_{SS} = – 5 Vdc (R_1 = 1 kΩ, R_L = 10 kΩ, Control t_{TLH} = t_{THL} = 20 ns)		–	5.0	–	300	–	$mV_{p–p}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. The formulas given are for the typical characteristics only at 25 °C.
5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TEST CIRCUITS
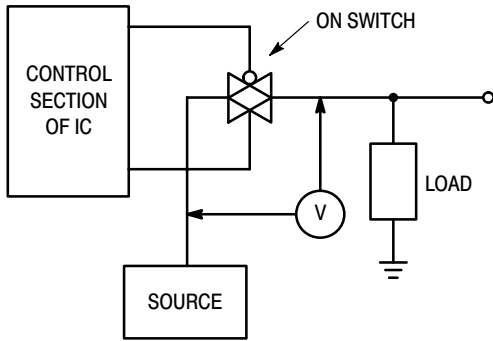
Figure 1. ΔV Across Switch
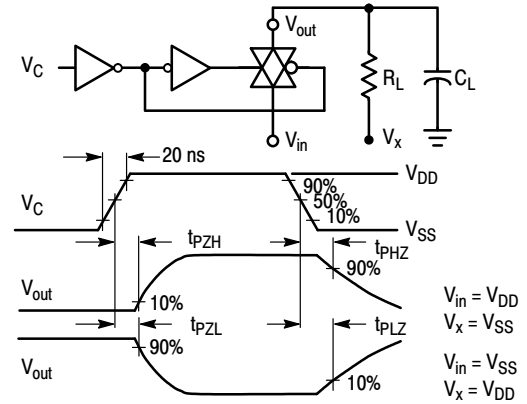
Figure 2. Turn-On Delay Time Test Circuit and Waveforms

$V_C = V_{DD}$ FOR BANDWIDTH TEST
$V_C = V_{SS}$ FOR FEEDTHROUGH TEST
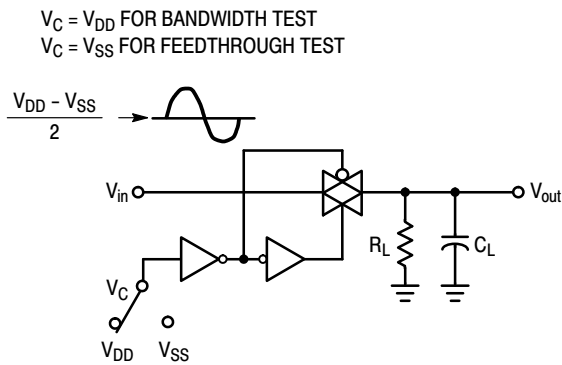
Figure 3. Bandwidth and Feedthrough Attenuation
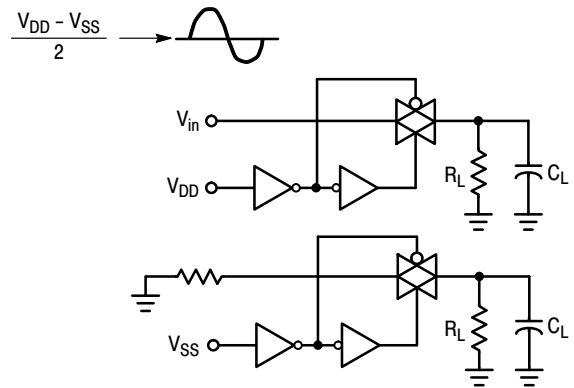
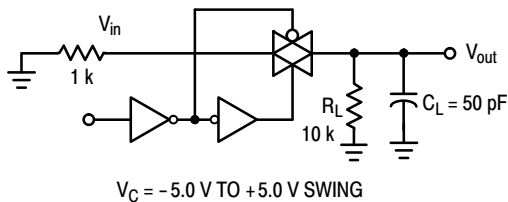**Figure 4. Channel Separation**

$V_C = -5.0$ V TO $+5.0$ V SWING

Figure 5. Crosstalk, Control to Output
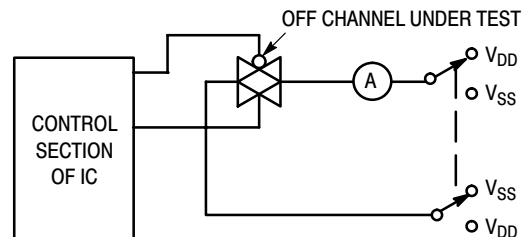
Figure 6. Off Channel Leakage

MC14066B
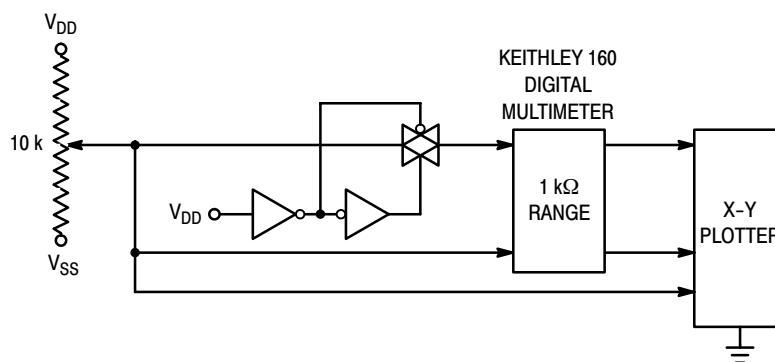
Figure 7. Channel Resistance (R$_{ON}$) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS
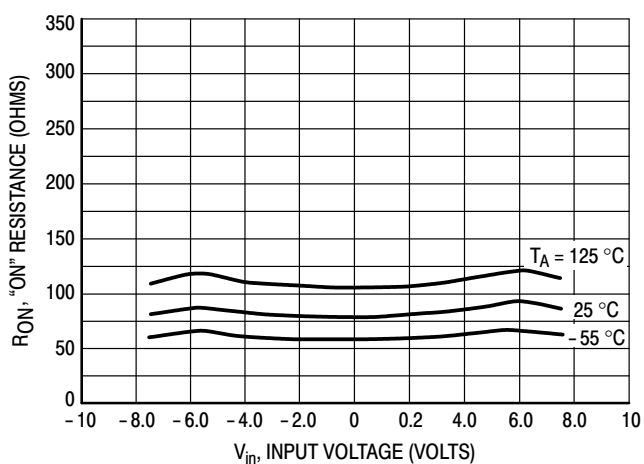
Figure 8. V$_{DD}$ = 7.5 V, V$_{SS}$ = − 7.5 V
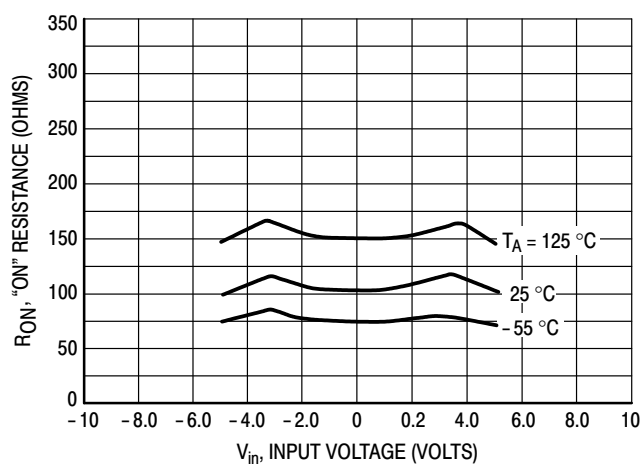
Figure 9. V$_{DD}$ = 5.0 V, V$_{SS}$ = − 5.0 V
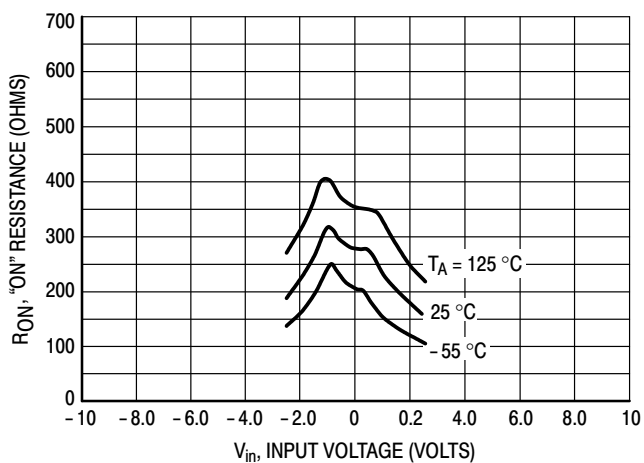
Figure 10. V$_{DD}$ = 2.5 V, V$_{SS}$ = − 2.5 V
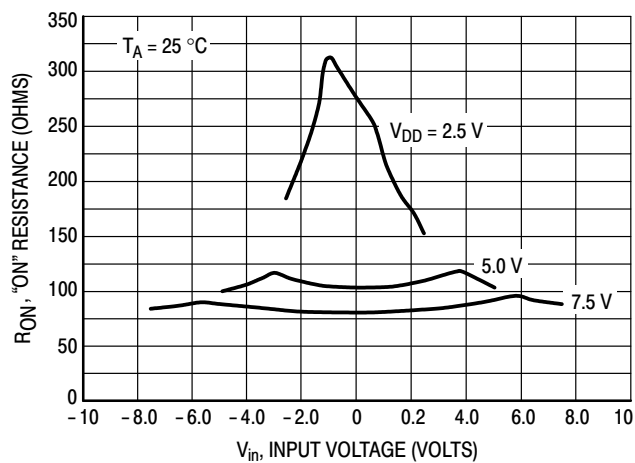
Figure 11. Comparison at 25 °C, V$_{DD}$ = −V$_{SS}$

MC14066B

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V digital control signal is used to directly control a 5 V peak-to-peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage, the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V peak-to-peak signal which allows no margin at either peak. If voltage transients above

V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.
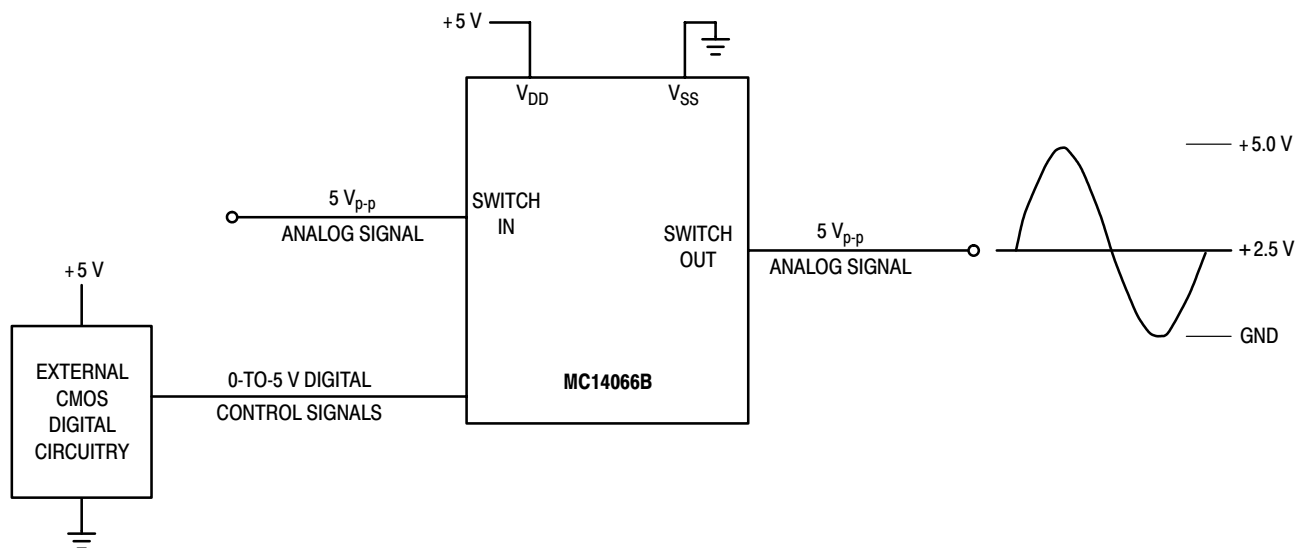
Figure A. Application Example
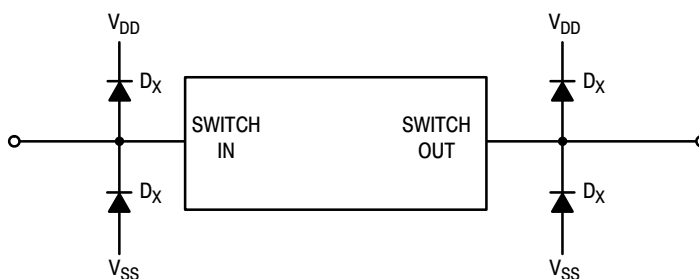
Figure B. External Germanium or Schottky Clipping Diodes

ORDERING INFORMATION

Device	Package	Shipping[†]
MC14066BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14066BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14066BDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC14066BDTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV14066BDTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 6)

NLV14066BDG*	SOIC-14 (Pb-Free)	55 Units / Rail
MC14066BFELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

MC14066B
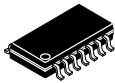
SOEIAJ–14
CASE 965–01
ISSUE B

DATE 29 FEB 2008
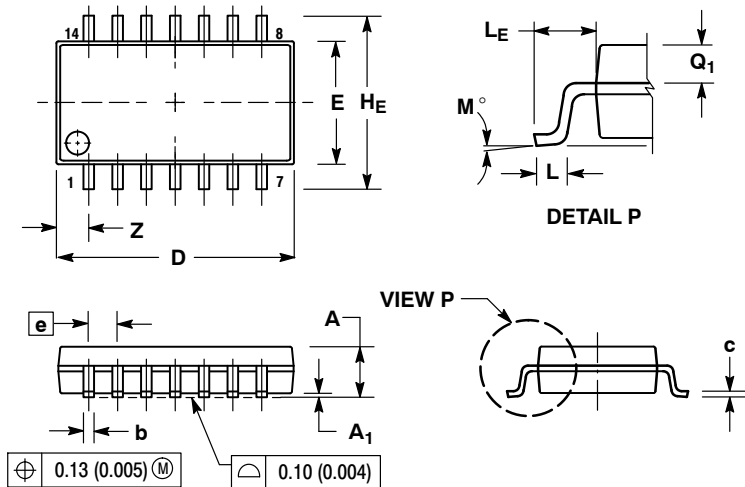
SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DETAIL P

VIEW P

⊕ | 0.13 (0.005) Ⓜ

△ | 0.10 (0.004)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A$_1$	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H$_E$	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L$_E$	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q$_1$	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

DOCUMENT NUMBER:	98ASH70108A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	14 LD SOEIAJ		PAGE 1 OF 1

SOIC−14 NB
CASE 751A−03
ISSUE L

14
1

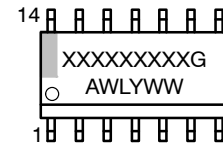**SCALE 1:1**

DATE 03 FEB 2016
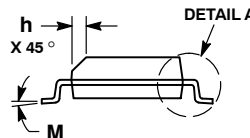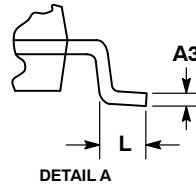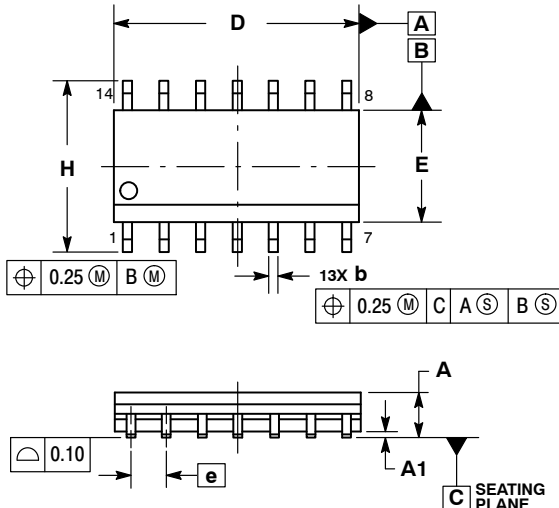
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °
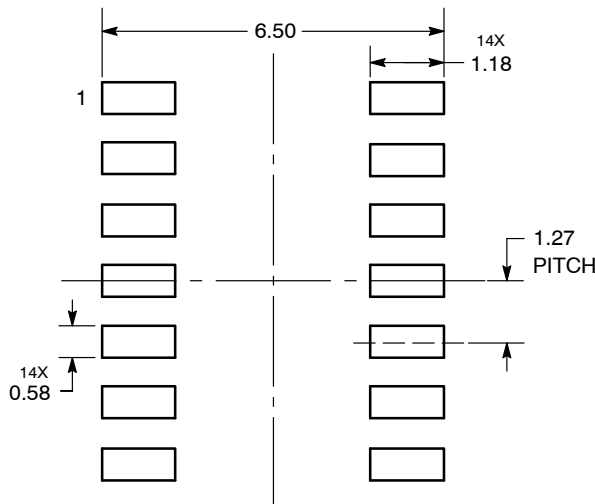
DETAIL A

SEATING PLANE

SOLDERING FOOTPRINT*

6.50

14X
1.18

1.27
PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

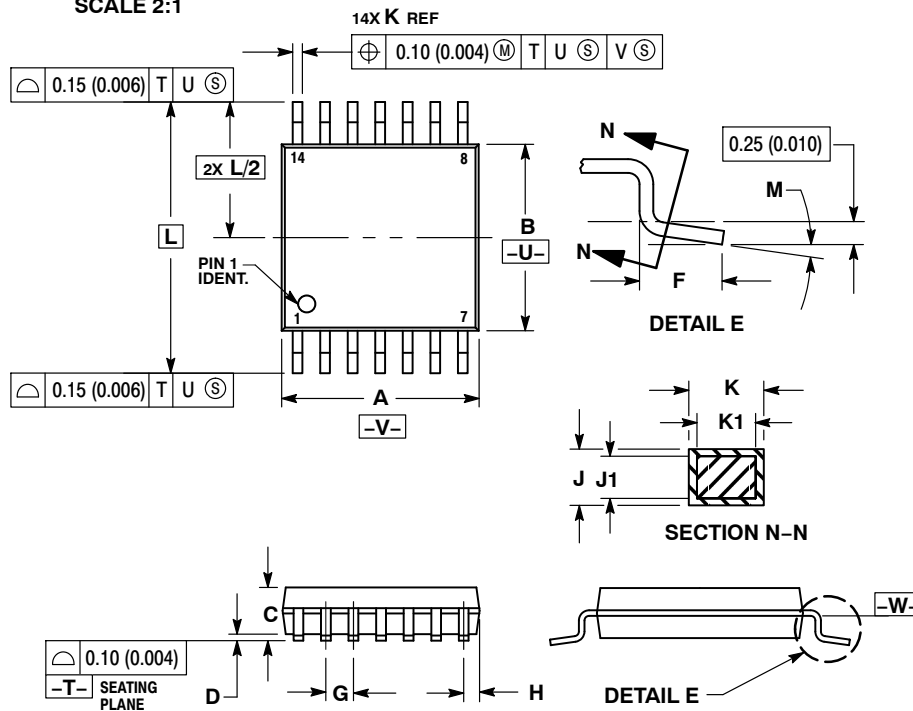| DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X K REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

⌒ | 0.15 (0.006) T U Ⓢ

2X L/2

L

PIN 1
IDENT.

14 8

B
−U−

1 7

A
−V−

⌒ | 0.15 (0.006) T U Ⓢ

N

0.25 (0.010)

M

N

F

DETAIL E

K

K1

J J1
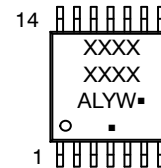
SECTION N−N

C

⌒ | 0.10 (0.004)
−T− SEATING
PLANE

D G H

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***
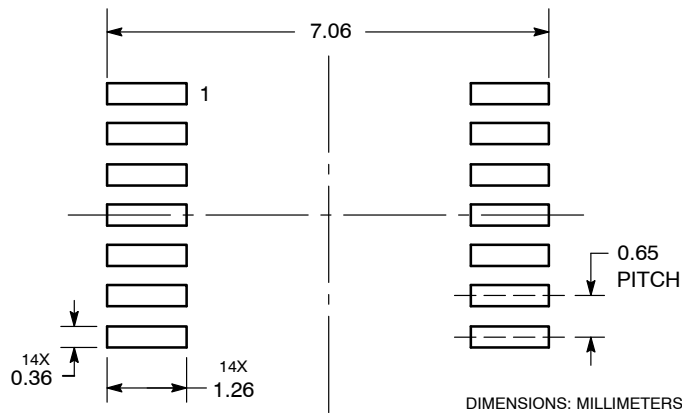
7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

14

XXXX
XXXX
ALYW▪

1

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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