

8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter

with LSTTL-Compatible Inputs

MC74VHC259

The MC74VHC259 is an 8-bit Addressable Latch fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL devices while maintaining CMOS low power dissipation.

The VHC259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table.. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the VHC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74VHC259 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC259 to be used to interface 5 V circuits to 3 V circuits.

- High Speed: $t_{PD} = 7.6 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC} @ \text{Load}$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V
- These Devices are Pb-Free and are RoHS Compliant

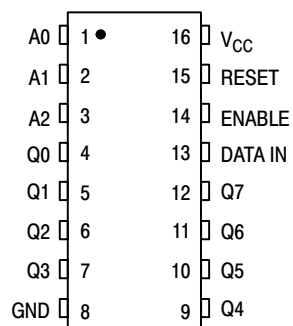
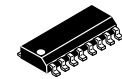
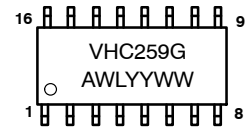


Figure 1. Pin Assignment

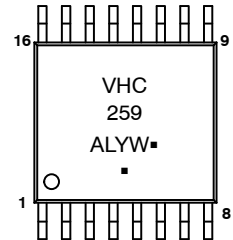
MARKING DIAGRAMS



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC259DR2G	SOIC-16	2500 Units/Reel
MC74VHC259DTR2G	TSSOP-16	2500 Units/Reel

DISCONTINUED (Note 1)

MC74VHC259DG	SOIC-16	48 Units/Rail
MC74VHC259DTG	TSSOP-16	96 Units/Rail

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your onsemi representative for information. The most current information on these devices may be available on www.onsemi.com.

MC74VHC259

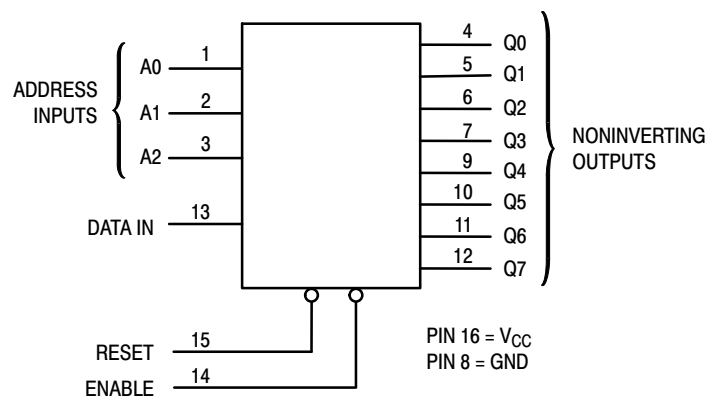


Figure 2. Logic Diagram

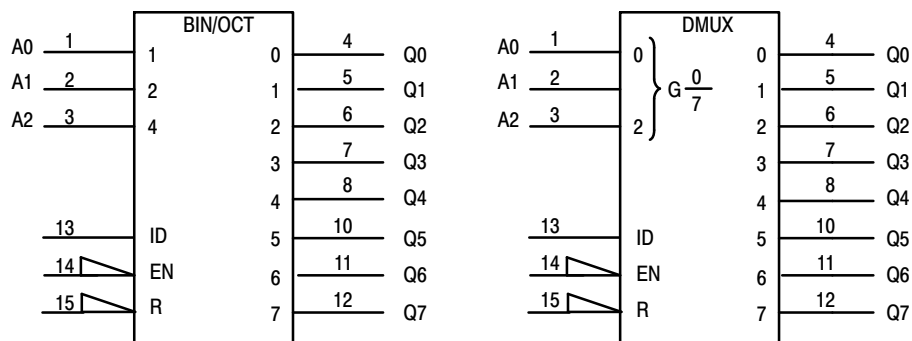


Figure 3. IEC Logic Symbol

LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

MC74VHC259

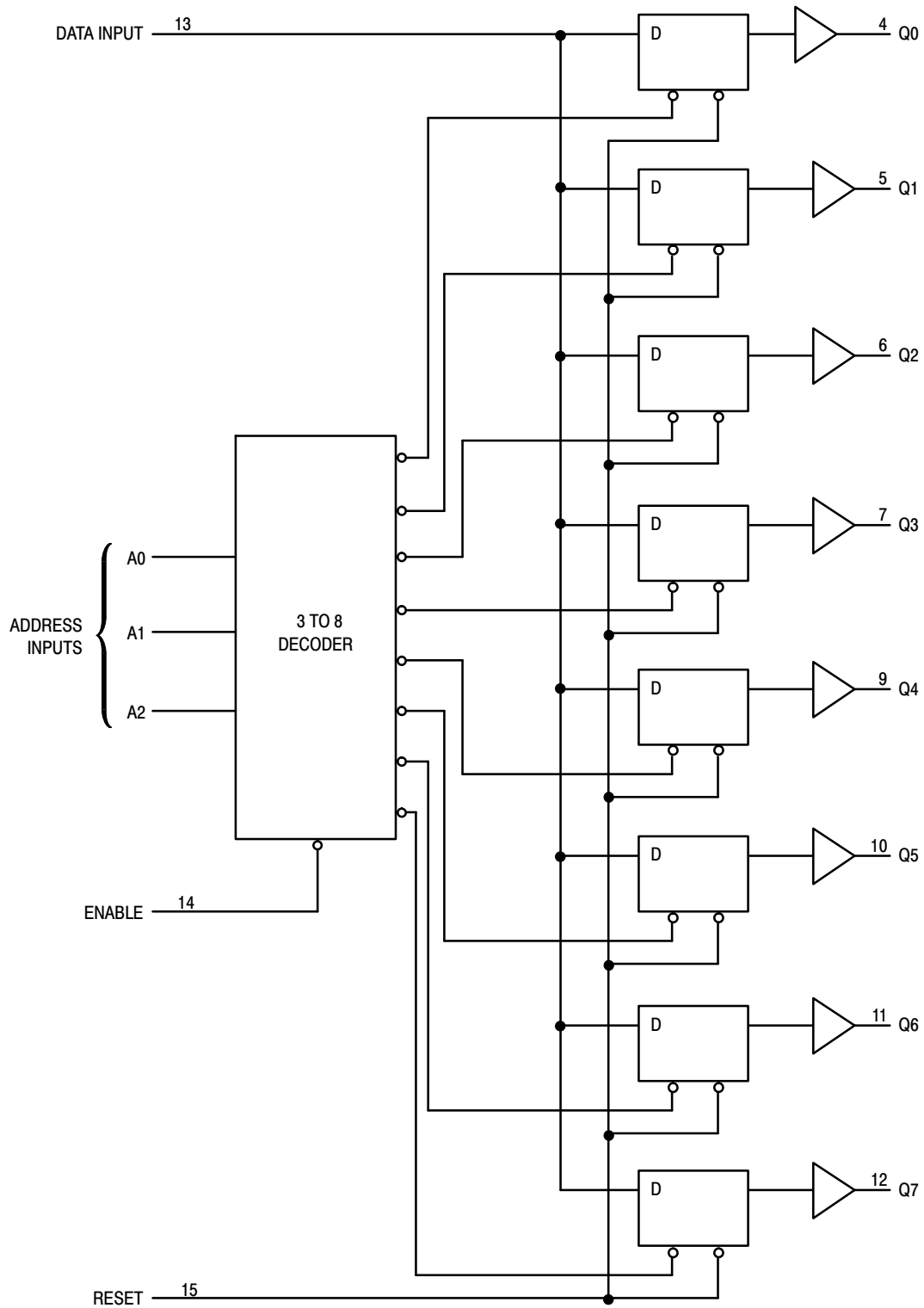


Figure 4. Expanded Logic Diagram

MC74VHC259

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage	−0.5 to +7.0	V
V _{IN}	Digital Input Voltage	−0.5 to +7.0	V
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	−20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{OUT}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air SOIC Package TSSOP	200 180	mW
T _{STG}	Storage Temperature Range	−65 to +150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1.) Machine Model (Note 2.) Charged Device Model (Note 3.)	>2000 >200 >2000	V
I _{LATCH-UP}	Latch-Up Performance Above V _{CC} and Below GND at 125°C (Note 4.)	± 300	mA
θ _{JA}	Thermal Resistance, Junction to Ambient SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range, all Package Types	−55	125	°C
t _r , t _f	Input Rise or Fall Time V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

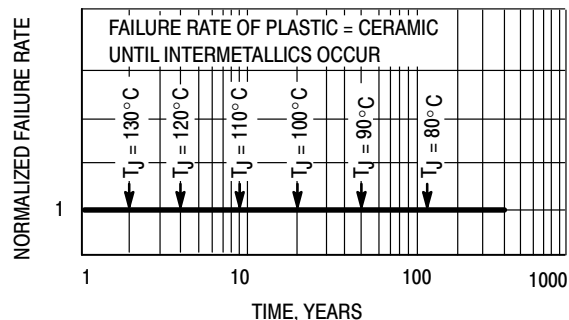


Figure 5. Failure Rate vs. Time Junction Temperature

MC74VHC259

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.5 V _{CCX} 0.7			1.5 V _{CCX} 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.5 V _{CCX} 0.3		0.5 V _{CCX} 0.3	V
V _{OH}	Maximum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5	2.58 3.94			2.48 3.8		V
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5		0.36 0.36			0.44 0.44	V
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Data to Output (Figures 6 and 11)	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 7 and 11)	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Enable to Output (Figures 8 and 11)	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t _{PHL}	Maximum Propagation Delay, Reset to Output (Figures 9 and 11)	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
C _{IN}	Maximum Input Capacitance			6	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 2)	Typical @ 25°C, V _{CC} = 5.0V	pF
		30	

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC259

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = \leq 85^\circ\text{C}$		$T_A = \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_w	Minimum Pulse Width, Reset or Enable (Figure 10)	$V_{CC} = 3.3 \pm 0.3\text{V}$	5.0			5.5		5.5		ns
		$V_{CC} = 5.0 \pm 0.5\text{V}$	5.0			5.5		5.5		
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 10)	$V_{CC} = 3.3 \pm 0.3\text{V}$	4.5			4.5		4.5		ns
		$V_{CC} = 5.0 \pm 0.5\text{V}$	3.0			3.0		3.0		
t_h	Minimum Hold Time, Enable to Address or Data (Figure 8 or 9)	$V_{CC} = 3.3 \pm 0.3\text{V}$	2.0			2.0		2.0		ns
		$V_{CC} = 5.0 \pm 0.5\text{V}$	2.0			2.0		2.0		
t_r, t_f	Maximum Input, Rise and Fall Times (Figure 6)	$V_{CC} = 3.3 \pm 0.3\text{V}$			400		300		300	ns
		$V_{CC} = 5.0 \pm 0.5\text{V}$			200		100		100	

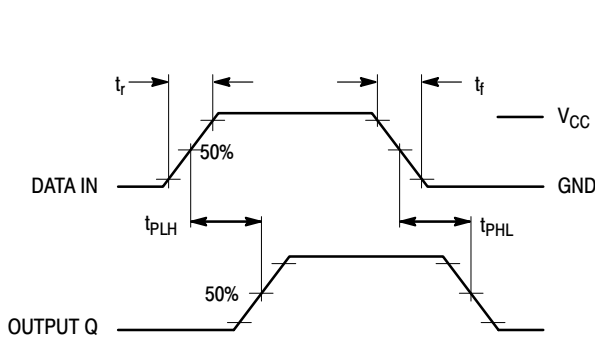


Figure 6. Switching Waveform

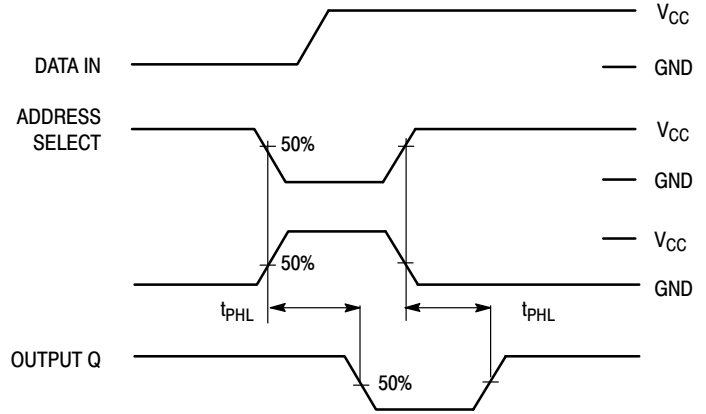


Figure 7. Switching Waveform

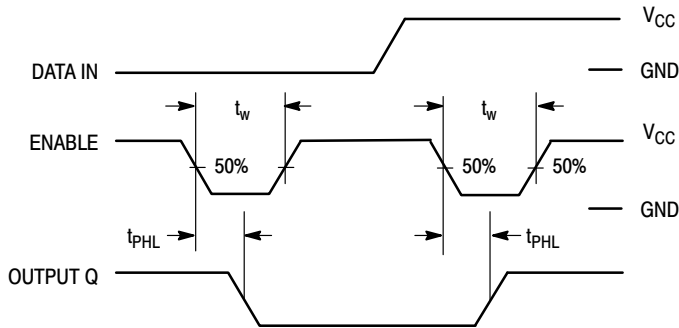


Figure 8. Switching Waveform

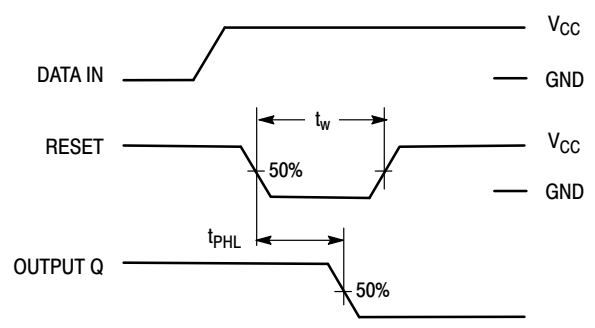


Figure 9. Switching Waveform

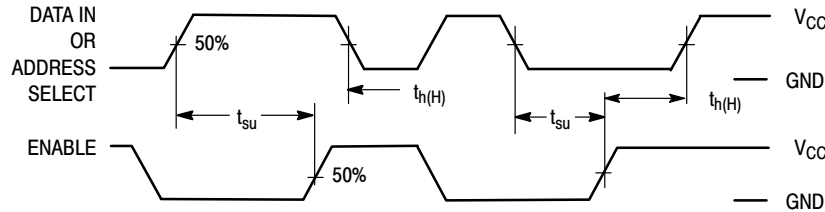
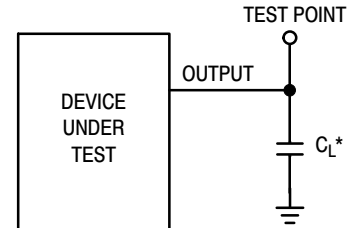
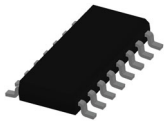


Figure 10. Switching Waveform



*Includes all probe and jig capacitance

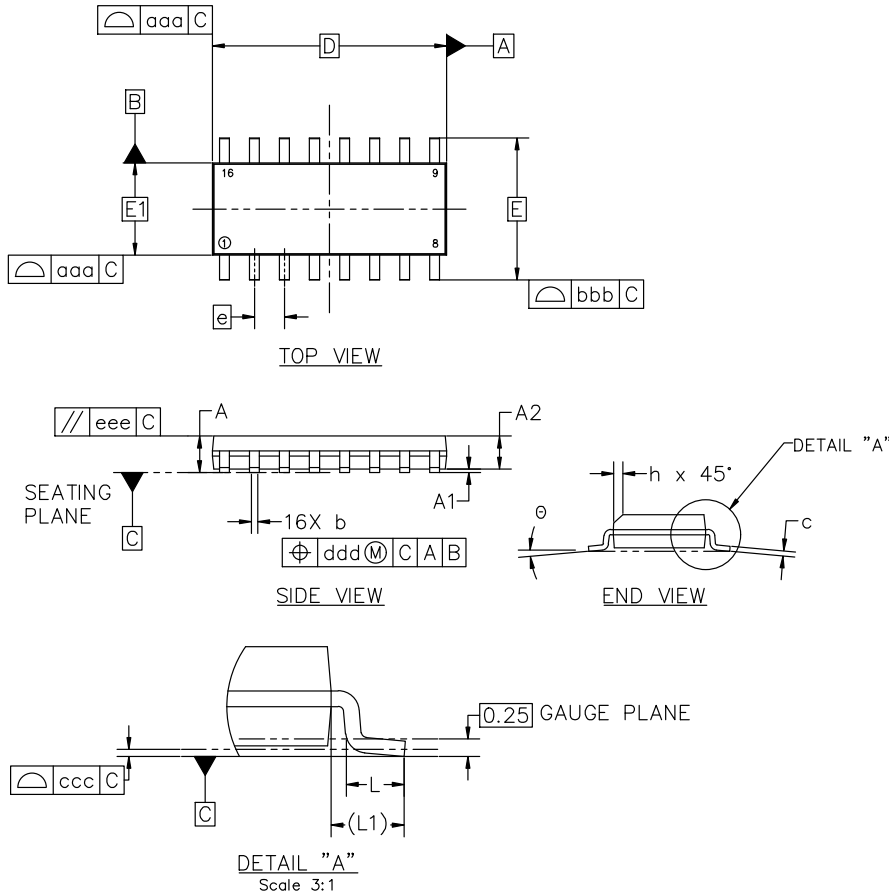
Figure 11. Test Circuit


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

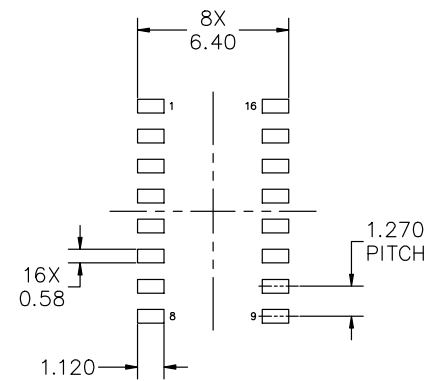
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

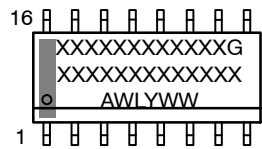
DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*

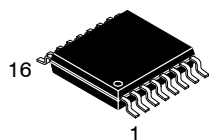


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

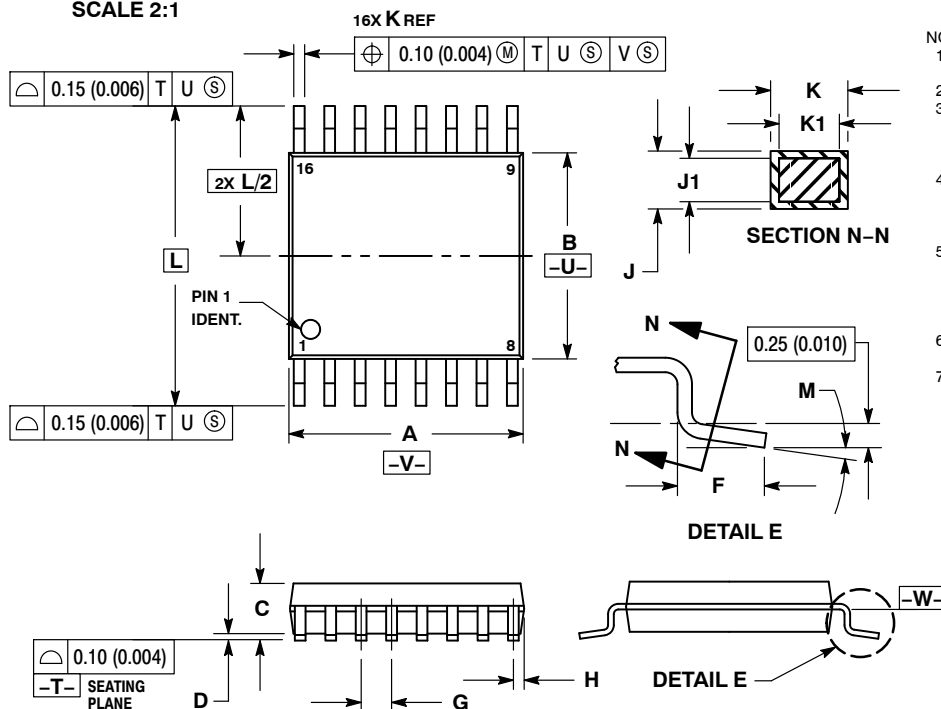
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 2 OF 2
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.		

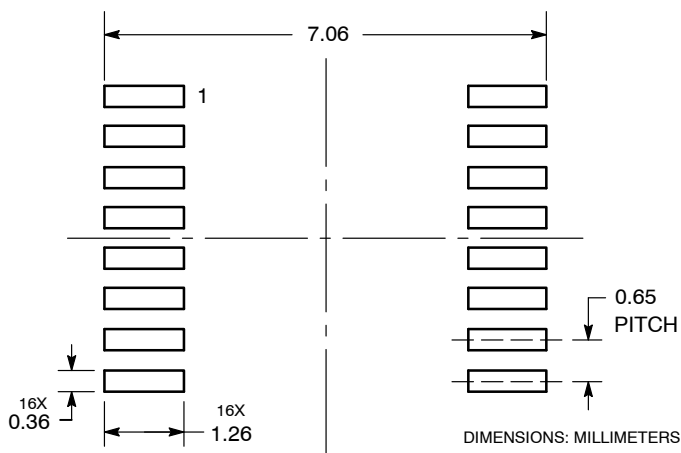

TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

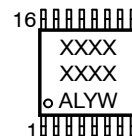

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales