Octal D-Type Flip-Flop with 3-State Output

MC74VHC374, MC74VHCT374A

The MC74VHC374/MC74VHCT374A is an advanced high speed CMOS octal flip−flop with 3−state output fabricated with silicon gate CMOS technology. The device achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The 8−bit D−type flip−flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The MC74VHC374 inputs are compatible with standard CMOS levels while the MC74VHCT374A inputs are compatible with TTL levels. The MC74VHCT374A can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The MC74VHC374 and MC74VHCT374A input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT374A output structures provide protection when V_{CC} = 0 V. These output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: f_{max} = 185 MHz (Typ) at V_{CC} = 5.0 V
  f_{max} = 140 MHz (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28%
- Power Down Protection Provided
- Balanced Propagation Delays
- Designed for: 2.0 V to 5.5 V (VHC)
  4.5 V to 5.5 V (VHCT)
- Low Noise: V_{OLP} = 0.9 V (Max) (VHC)
  V_{OLP} = 1.1 V (Max) (VHCT)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- Chip Complexity: 276 FETs or 69 Equivalent Gates
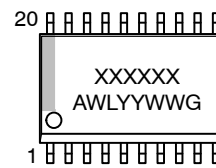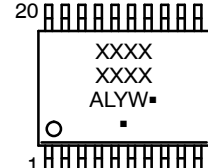- These Devices are Pb−Free, Halogen Free and are RoHS Compliant
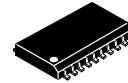
SOIC−20
DW SUFFIX
CASE 751D

TSSOP−20
DT SUFFIX
CASE 948E

MARKING DIAGRAMS

SOIC−20

XXXXXX
AWLYYWWG

TSSOP−20

XXXX
XXXX
ALYW■

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

$\overline{OE}$	1	20	V_{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	CP

FUNCTION TABLE

INPUTS			OUTPUT
OE	CP	D	Q
L	⤒	H	H
L	⤒	L	L
L	L, H, ⤓	X	No Change
H	X	X	Z

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.
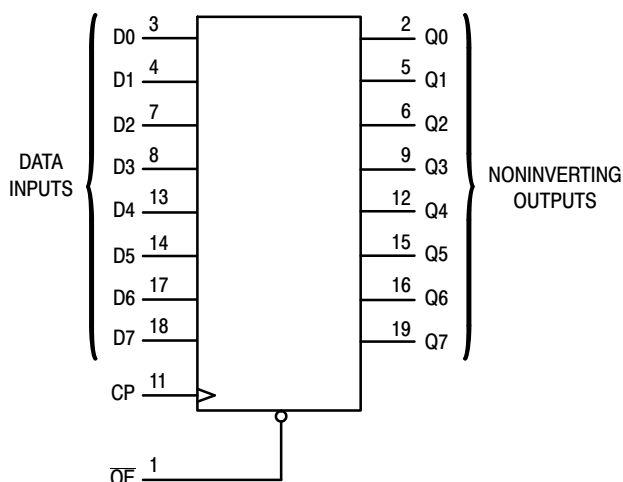
MC74VHC374, MC74VHCT374A

Figure 1. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage (MC74VHC)		−0.5 to V_{CC} + 0.5	V
	DC Output Voltage (MC74VHCT)	Active Mode (High or Low State)	−0.5 to V_{CC} + 0.5	
		Tristate Mode (Note 1)	−0.5 to +6.5	
		Power−Off Mode (V_{CC} = 0 V)	−0.5 to +6.5	
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current	MC74VHC374	±20	mA
		MC74VHCT374A	−20	
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC−20W	96	°C/W
		TSSOP−20	150	
P_D	Power Dissipation in Still Air at 25°C	SOIC−20W	1302	mW
		TSSOP−20	833	
MSL	Moisture Sensitivity	SOIC−20W	Level 3	–
		All Other Packages	Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.374 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74VHC					
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 5)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	20	
MC74VHCT					
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{IN}	DC Input Voltage (Note 5)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State)	0	V_{CC}	V
		Tristate Mode	0	5.5	
		Power−Off Mode (V_{CC} = 0 V)	0	5.5	
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74VHC374)

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = − 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = − 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = − 4 mA I_{OH} = − 8 mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			±0.25		±2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74VHC374, MC74VHCT374A

AC ELECTRICAL CHARACTERISTICS (MC74VHC374)

Symbol	Parameter	Test Conditions		$T_A = 25°C$			$T_A = -40$ to $85°C$		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$ pF $C_L = 50$ pF	80 55	130 85		70 50		ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$ pF $C_L = 50$ pF	130 85	185 120		110 75		
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$ pF $C_L = 50$ pF		8.1 10.6	12.7 16.2	1.0 1.0	15.0 18.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$ pF $C_L = 50$ pF		5.4 6.9	8.1 10.1	1.0 1.0	9.5 11.5	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$ pF $C_L = 50$ pF		7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$ pF $C_L = 50$ pF		5.1 6.6	7.6 9.6	1.0 1.0	9.0 11.0	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Q	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 50$ pF		10.2	14.0	1.0	16.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 50$ pF		6.1	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 50$ pF (Note 6)			1.5		1.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 50$ pF (Note 6)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)				6				pF

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 7)	32	pF

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (MC74VHC374) (C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.6	−0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (MC74VHC374)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = − 40 to 85°C	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V		5.0 5.0	5.5 5.0	ns
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V		4.5 3.0	4.5 3.0	ns
t_h	Minimum Hold Time, D to CP	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V		2.0 2.0	2.0 2.0	ns
t_r, t_f	Maximum Input Rise and Fall Times	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V				ns

MC74VHC374, MC74VHCT374A

DC ELECTRICAL CHARACTERISTICS (MC74VHCT374A)

Symbol	Parameter	Test Conditions	V_CC V	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40 to 85°C Min	T_A = −40 to 85°C Max	Unit
V_{IH}	Minimum High−Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low−Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High−Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -50\ \mu A$	4.5	4.4	4.5		4.4		V
		$I_{OH} = -8$ mA	4.5	3.94			3.80		
V_{OL}	Maximum Low−Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 50\ \mu A$	4.5		0.0	0.1		0.1	V
		$I_{OL} = 8$ mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5$ V or GND	0 to 5.5			±0.1		±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5			±0.25		±2.5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: $V_{IN} = 3.4$ V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5$ V	0			0.5		5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHCT374A)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40 to 85°C Min	T_A = −40 to 85°C Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF	90 85	140 130		80 95		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OE}$ to Q	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF		7.0	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 8)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum 3−State Output Capacitance (Output in High−Impedance State)			9				pF

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 9)	25	pF

8. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
9. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

MC74VHC374, MC74VHCT374A

NOISE CHARACTERISTICS (MC74VHCT374A) (C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Parameter	T_A = 25°C Typ	T_A = 25°C Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (MC74VHCT374A)

Symbol	Parameter	Test Conditions	T_A = 25°C Typ	T_A = 25°C Limit	T_A = − 40 to 85°C Limit	Unit
t_w	Minimum Pulse Width, CP	V_{CC} = 5.0 ± 0.5 V		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns
t_h	Minimum Hold Time, D to CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns

MC74VHC374, MC74VHCT374A
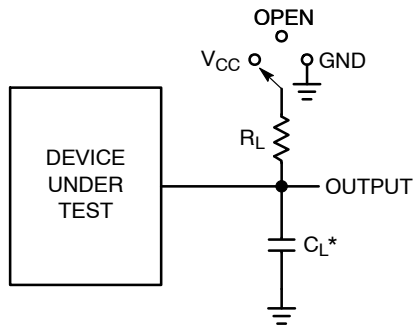
*C_L Includes probe and jig capacitance
Input signal $t_R = t_F = 3$ ns

Figure 2. Test Circuits

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

SWITCHING WAVEFORMS
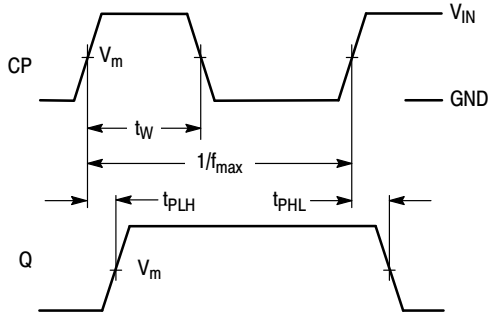
Figure 3.
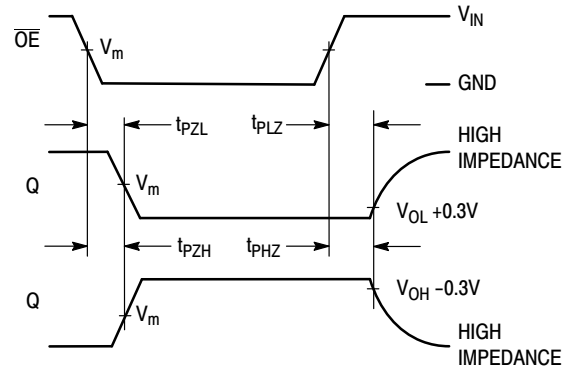
Figure 4.
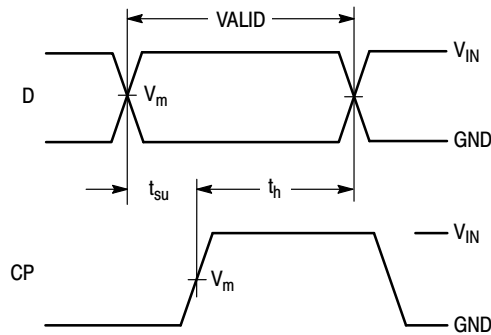
Figure 5.

Device	V_{IN}, V	V_m, V
MC74VHC374	V_{CC}	50% x V_{CC}
MC74VHCT374A	3 V	1.5 V

MC74VHC374, MC74VHCT374A
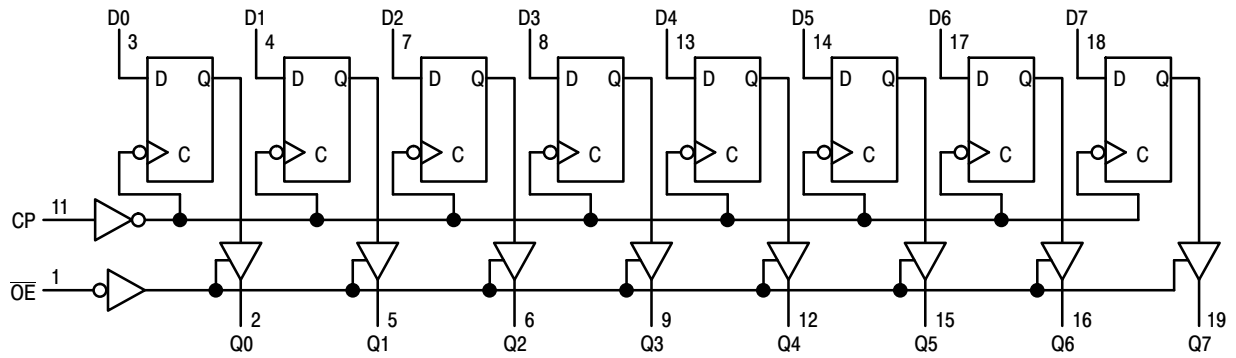
Figure 6. Expanded Logic Diagram
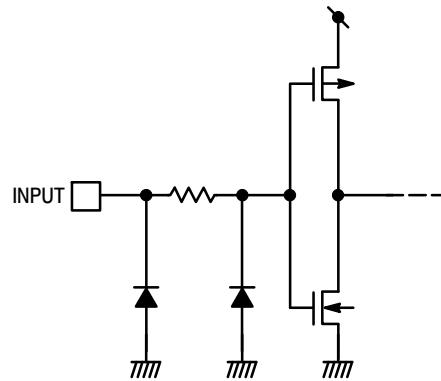
Figure 7. Input Equivalent Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74VHC374DWR2G	VHC374G	SOIC−20W	1000 / Tape & Reel
MC74VHC374DTR2G	VHC 374	TSSOP−20	2500 / Tape & Reel
MC74VHCT374ADWR2G	VHCT374AG	SOIC−20W	1000 / Tape & Reel
MC74VHCT374ADTR2G	VHCT 374A	TSSOP−20	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

onsemi
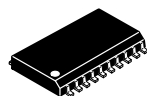
SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

SCALE 1:1
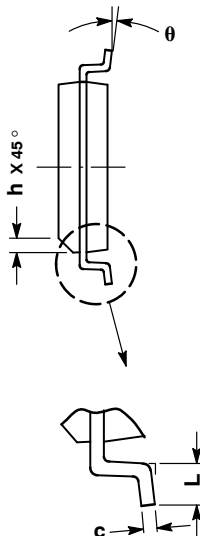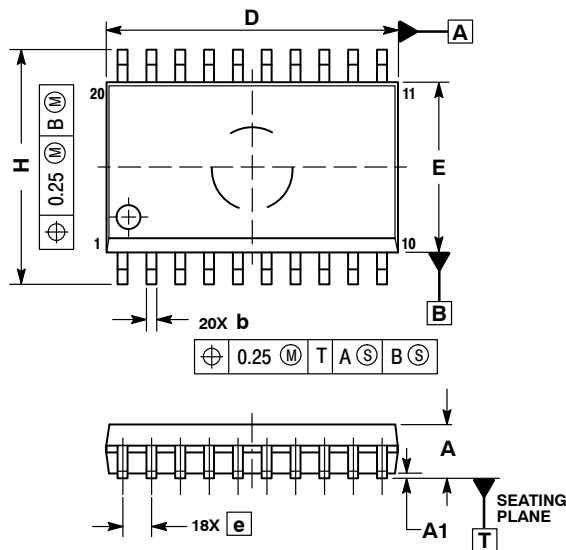
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

RECOMMENDED
SOLDERING FOOTPRINT*

20X 0.52
20X 1.30
11.00
1.27
PITCH
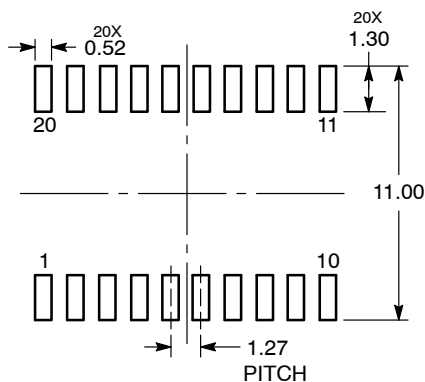
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXXXXXXX
XXXXXXXXXX
AWLYYWWG
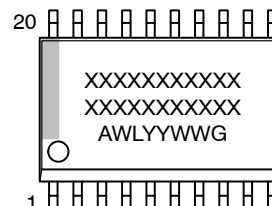
XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−20 WB		PAGE 1 OF 1

onsemi

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016
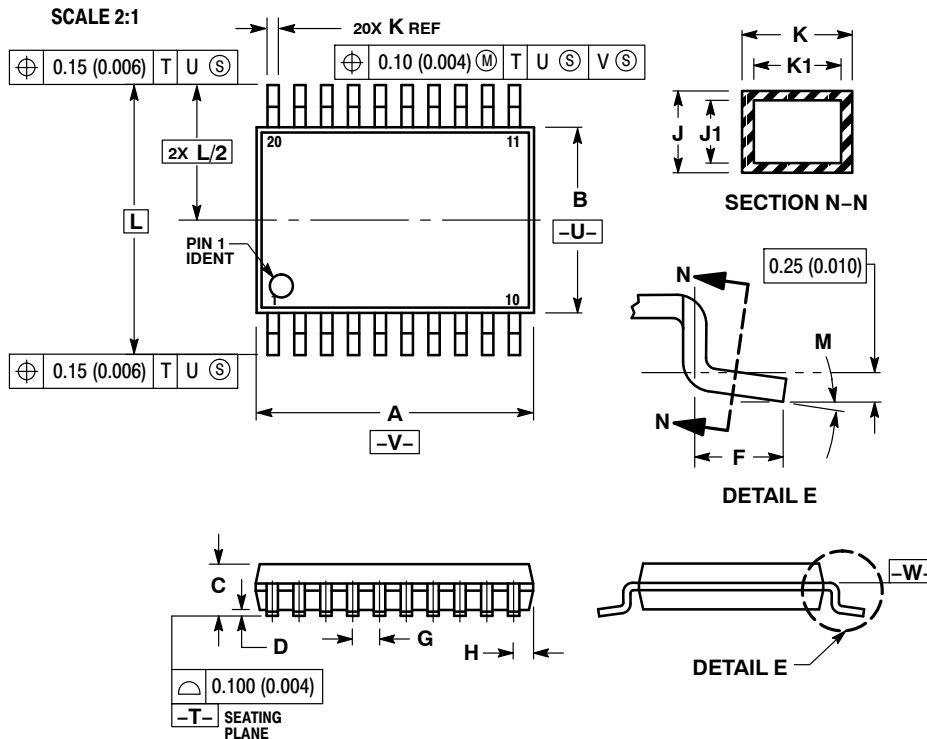
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SCALE 2:1

$\oplus$ | 0.15 (0.006) | T | U | $\textcircled{S}$

$\oplus$ | 0.10 (0.004) | $\textcircled{M}$ | T | U | $\textcircled{S}$ | V | $\textcircled{S}$

20X **K** REF

2X **L/2**

L

PIN 1 IDENT

$\oplus$ | 0.15 (0.006) | T | U | $\textcircled{S}$

A
−V−

20 11

10

B

−U−

SECTION N−N

K
K1

J **J1**

0.25 (0.010)

N

N

M

F

DETAIL E

C

D **G** **H**

$\triangle$ | 0.100 (0.004)

−T− SEATING PLANE

−W−

DETAIL E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*
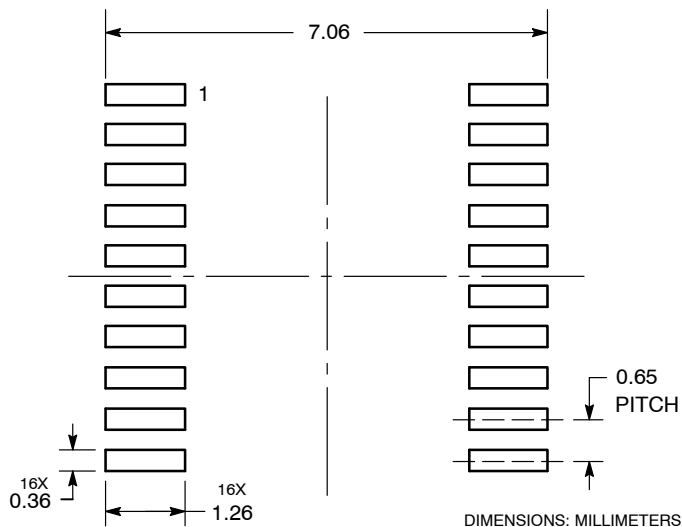
7.06

1

16X
0.36

16X
1.26

0.65 PITCH

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

XXXX
XXXX
ALYW■
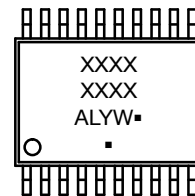
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■ ", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSSOP−20 WB		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊