## MC74VHC540

## Octal Bus Buffer

## Inverting

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND-ed active-low output enables. When either $\overline{\mathrm{OE} 1}$ or $\overline{\mathrm{OE} 2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V , allowing the interface of 5.0 V systems to 3.0 V systems.

## Features

- High Speed: $\mathrm{t}_{\mathrm{PD}}=3.7 \mathrm{~ns}(\mathrm{Typ})$ at $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$
- Low Power Dissipation: $\mathrm{I}_{\mathrm{CC}}=4.0 \mu \mathrm{~A}$ (Max) at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$
- High Noise Immunity: $\mathrm{V}_{\mathrm{NIH}}=\mathrm{V}_{\mathrm{NIL}}=28 \% \mathrm{~V}_{\mathrm{CC}}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: Volp $=1.2 \mathrm{~V}(\mathrm{Max})$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- These Devices are $\mathrm{Pb}-$ Free and are RoHS Compliant


Figure 1. Logic Diagram

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http://onsemi.com


## PIN ASSIGNMENT



## FUNCTION TABLE

| Inputs |  |  | Output $\bar{Y}$ |
| :---: | :---: | :---: | :---: |
| OE1 | OE2 | A |  |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
| :---: | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage | -0.5 to +7.0 | V |
| $\mathrm{~V}_{\text {in }}$ | DC Input Voltage | -0.5 to +7.0 | V |
| $\mathrm{~V}_{\text {out }}$ | DC Output Voltage | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{I}_{\mathrm{IK}}$ | Input Diode Current | -20 | mA |
| $\mathrm{I}_{\mathrm{OK}}$ | Output Diode Current | $\pm 20$ | mA |
| $\mathrm{I}_{\text {out }}$ | DC Output Current, per Pin | $\pm 25$ | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | DC Supply Current, $\mathrm{V}_{\mathrm{CC}}$ and GND Pins | $\pm 75$ | mA |
| $\mathrm{P}_{\mathrm{D}}$ | Power Dissipation in Still Air, $\quad$SOIC Packagest | 500 | mW |
|  |  | TSSOP Packaget | 450 |
| $\mathrm{~T}_{\text {stg }}$ | Storage Temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.
$\dagger$ Derating - SOIC Packages: $-7 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ from $65^{\circ}$ to $125^{\circ} \mathrm{C}$
TSSOP Package: $-6.1 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ from $65^{\circ}$ to $125^{\circ} \mathrm{C}$


## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage | 2.0 | 5.5 | V |
| $\mathrm{~V}_{\text {in }}$ | DC Input Voltage | 0 | 5.5 | V |
| $\mathrm{~V}_{\text {out }}$ | DC Output Voltage | 0 | $\mathrm{~V}_{\mathrm{CC}}$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature, All Package Types | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise and Fall Time <br> (Figure 1) | $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$ | 0 | 100 |
|  | $\mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ | 0 | 20 |  |

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $\underset{\mathbf{V}}{\mathrm{V}_{\mathrm{cc}}}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  | $\mathrm{T}_{\mathrm{A}}=-55$ to $125^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max | Min | Max |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High-Level Input Voltage |  | $\begin{gathered} 2.0 \\ 3.0 \text { to } \\ 5.5 \end{gathered}$ | $\begin{gathered} 1.50 \\ V_{C C} \times 0.7 \end{gathered}$ |  |  | $\begin{gathered} 1.50 \\ V_{C C} \times 0.7 \end{gathered}$ |  | V |
| VIL | Maximum Low-Level Input Voltage |  | $\begin{gathered} 2.0 \\ 3.0 \text { to } \\ 5.5 \end{gathered}$ |  |  | $\begin{gathered} 0.50 \\ v_{C C} \times 0.3 \end{gathered}$ |  | $\begin{gathered} 0.50 \\ v_{C C} \times 0.3 \end{gathered}$ | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum High-Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{IOH}_{\mathrm{OH}}=-50 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 2.9 \\ & 4.4 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 4.5 \end{aligned}$ |  | $\begin{aligned} & 1.9 \\ & 2.9 \\ & 4.4 \end{aligned}$ |  | V |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{I}_{\mathrm{OH}}=-4 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-8 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 2.58 \\ & 3.94 \end{aligned}$ |  |  | $\begin{aligned} & 2.48 \\ & 3.80 \end{aligned}$ |  |  |
| $\mathrm{V}_{\text {OL }}$ | Maximum Low-Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{IOL}_{\mathrm{OL}}=50 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 4.5 \end{aligned}$ |  | $\begin{aligned} & 0.0 \\ & 0.0 \\ & 0.0 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ |  | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | V |
|  |  | $\begin{aligned} \mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} & \\ \mathrm{I}_{\mathrm{OL}} & =4 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{OL}} & =8 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 4.5 \end{aligned}$ |  |  | $\begin{aligned} & 0.36 \\ & 0.36 \end{aligned}$ |  | $\begin{aligned} & 0.44 \\ & 0.44 \end{aligned}$ |  |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $\underset{\mathbf{v}}{\mathrm{v}_{\mathrm{cc}}}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  | $\mathrm{T}_{\mathrm{A}}=-55$ to $125^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max | Min | Max |  |
| $\mathrm{l}_{\text {in }}$ | Maximum Input Leakage Current | $\mathrm{V}_{\text {in }}=5.5 \mathrm{~V}$ or GND | 0 to 5.5 |  |  | $\pm 0.1$ |  | $\pm 1.0$ | $\mu \mathrm{A}$ |
| loz | Maximum Three-State Leakage Current | $\begin{aligned} & \mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\text {IH }} \\ & \mathrm{V}_{\text {out }}=\mathrm{V}_{\mathrm{CC}} \text { or } G N D \end{aligned}$ | 5.5 |  |  | $\pm 0.25$ |  | $\pm 2.5$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ | Maximum Quiescent Supply Current | $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {CC }}$ or GND | 5.5 |  |  | 4.0 |  | 40.0 | $\mu \mathrm{A}$ |

AC ELECTRICAL CHARACTERISTICS (Input $\mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=3.0 \mathrm{~ns}$ )

| Symbol | Parameter | Test Conditions |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  | $\mathrm{T}_{\mathrm{A}}=-55$ to $125^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max | Min | Max |  |
| $\begin{aligned} & \text { tpLH, } \\ & \mathrm{t}_{\text {PHL }} \end{aligned}$ | Maximum Propagation Delay, A to $\bar{Y}$ <br> (Figures 1 and 3) | $\mathrm{V}_{\mathrm{CC}}=3.3 \pm 0.3 \mathrm{~V}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | $\begin{aligned} & 4.8 \\ & 7.3 \end{aligned}$ | $\begin{gathered} 7.0 \\ 10.5 \end{gathered}$ | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{gathered} 8.5 \\ 12.0 \end{gathered}$ | ns |
|  |  | $\mathrm{V}_{\mathrm{CC}}=5.0 \pm 0.5 \mathrm{~V}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | $\begin{aligned} & \hline 3.7 \\ & 5.2 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \hline 6.0 \\ & 8.0 \end{aligned}$ |  |
| $\begin{aligned} & \text { tpZL, } \\ & \text { tpZH } \end{aligned}$ | Output Enable TIme, OEn to $\bar{Y}$ <br> (Figures 2 and 4) | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=3.3 \pm 0.3 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega \end{aligned}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | $\begin{aligned} & 6.8 \\ & 9.3 \end{aligned}$ | $\begin{aligned} & 10.5 \\ & 14.0 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 16.0 \end{aligned}$ | ns |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \pm 0.5 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega \end{aligned}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | $\begin{aligned} & 4.7 \\ & 6.2 \end{aligned}$ | $\begin{aligned} & 7.2 \\ & 9.2 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{gathered} 8.5 \\ 10.5 \end{gathered}$ |  |
| $\begin{aligned} & \text { tpLZ, } \\ & \text { tpHZ } \end{aligned}$ | Output Disable Time, OEn to $\bar{Y}$ <br> (Figures 2 and 4) | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=3.3 \pm 0.3 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega \end{aligned}$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  | 11.2 | 15.4 | 1.0 | 17.5 | ns |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \pm 0.5 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega \end{aligned}$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  | 6.0 | 8.8 | 1.0 | 10.0 |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{OSLH}}, \\ & \mathrm{t}_{\mathrm{OSHL}} \end{aligned}$ | Output to Output Skew | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=3.3 \pm 0.3 \mathrm{~V} \\ & \text { (Note 1) } \end{aligned}$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  | 1.5 |  |  | ns |
|  |  | $\begin{aligned} & \mathrm{V}_{C C}=5.0 \pm 0.5 \mathrm{~V} \\ & \text { (Note 1) } \end{aligned}$ | $C_{L}=50 \mathrm{pF}$ |  |  | 1.0 |  |  | ns |
| $\mathrm{C}_{\text {in }}$ | Maximum Input Capacitance |  |  |  | 4 | 10 |  | 10 | pF |
| Cout | Maximum Three-State Output Capacitance (Output in High Impedance State) |  |  |  | 6 |  |  |  | pF |


|  |  | Typical @ 25 ${ }^{\circ} \mathbf{C}, \mathbf{\mathbf { V } _ { \mathbf { C C } } = \mathbf { 5 . 0 V }}$ |  |
| :--- | :--- | :---: | :---: |
| $\mathrm{C}_{\text {PD }}$ | Power Dissipation Capacitance (Note 2) | 17 | pF |

1. Parameter guaranteed by design. $\mathrm{t}_{\mathrm{OSLH}}=\left|\mathrm{t}_{\text {PLHm }}-\mathrm{t}_{\text {PLHn }}\right|, \mathrm{t}_{\mathrm{OSHL}}=\left|\mathrm{t}_{\text {PHLm }}-\mathrm{t}_{\text {PHLn }}\right|$.
2. $\mathrm{C}_{P D}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $\mathrm{I}_{\mathrm{CC}(\mathrm{OPR})}=\mathrm{C}_{\mathrm{PD}} \bullet \mathrm{V}_{\mathrm{CC}} \bullet \mathrm{f}_{\mathrm{in}}+\mathrm{I}_{\mathrm{CC}} / 8$ (per bit). $\mathrm{C}_{P D}$ is used to determine the no-load dynamic power consumption; $\mathrm{P}_{\mathrm{D}}=\mathrm{C}_{P D} \bullet \mathrm{~V}_{\mathrm{CC}}{ }^{2} \bullet \mathrm{f}_{\text {in }}+\mathrm{I}_{\mathrm{CC}} \bullet \mathrm{V}_{\mathrm{CC}}$.

NOISE CHARACTERISTICS (Input $\mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=3.0 \mathrm{~ns}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ )

| Symbol | Parameter | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Typ | Max |  |
| V OLP | Quiet Output Maximum Dynamic $\mathrm{V}_{\text {OL }}$ | 0.9 | 1.2 | V |
| $\mathrm{V}_{\text {OLV }}$ | Quiet Output Minimum Dynamic $\mathrm{V}_{\mathrm{OL}}$ | -0.9 | -1.2 | V |
| $\mathrm{V}_{\text {IHD }}$ | Minimum High Level Dynamic Input Voltage |  | 3.5 | V |
| $\mathrm{V}_{\text {ILD }}$ | Maximum Low Level Dynamic Input Voltage |  | 1.5 | V |

## MC74VHC540

## SWITCHING WAVEFORMS



Figure 2.

## TEST CIRCUITS


*Includes all probe and jig capacitance
Figure 4.

*Includes all probe and jig capacitance
Figure 5.

INPUT EQUIVALENT CIRCUIT


## MC74VHC540

ORDERING INFORMATION

| Device | Package | Shipping $^{\dagger}$ |
| :--- | :---: | :---: |
| MC74VHC540DWR2G | SOIC-20 <br> (Pb-Free) | 1000 Units / Tape \& Reel |
| MC74VHC540DTR2G | TSSOP-20 <br> (Pb-Free) | 2500 Units / Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.


SCALE 1:1


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES

PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR

PROTRUSION. ALLOWABLE PROTRUSION
PROTRUSION. ALLOWABLE PROTRUSIO
SHALL BE 0.13 TOTAL IN EXCESS OF B
SHALL BE 0.13 TOTAL IN EXCESS OF B
DIMENSION AT MAXIMUM MATERIAL
CONDITION.

|  | MILLIMETERS |  |
| :---: | :---: | :---: |
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 | BSC |
| H | 10.05 | 10.55 |
| $\mathbf{h}$ | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| $\boldsymbol{\theta}$ | $0^{\circ}$ | $7{ }^{\circ}$ |

\section*{MARKING DIAGRAM* <br>  <br> 

| XXXXX | $=$ Specific Device Code |
| :--- | :--- |
| A | $=$ Assembly Location |
| WL | $=$ Wafer Lot |
| YY | $=$ Year |
| WW | $=$ Work Week |
| G | $=$ Pb-Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-\mathrm{Free}$ indicator, " G " or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

[^0]TSSOP-20 WB
CASE 948E
ISSUE D
DATE 17 FEB 2016

SCALE 2:1


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
CONTROLLING DIMENSION: MILLIMETER
2. DIMENSION A DOES NOT INCLUDE MOLD

FLASH, PROTRUSIONS OR GATE BURRS.
FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH OR GATE BURRS SHALL NO
EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE

INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. SHALL NOT EXCEED $0.25(0.010)$ PER SIDE
5. DIMENSION K DOES NOT INCLUDE

DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC |  | 0.026 BSC |  |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 | BSC | 0.252 BSC |  |
| M | 0 | $0^{\circ}$ | $8^{\circ}$ | 0 |

GENERIC MARKING DIAGRAM* НРННННННН

|  | XXXX |
| :---: | :---: |
|  | XXXX |
|  | ALYW. |
| $\bigcirc$ | - |

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

- = Pb-Free Package
(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-$ Free indicator, " G " or microdot " $\mathrm{\nabla}$ ", may or may not be present.
DIMENSIONS: MILLIMETERS

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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | TSSOP-20 WB | PAGE 1 OF 1 |

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