MLD1N06CL

Power MOSFET 1 Amp, 62 Volts, Logic Level

N−Channel DPAK

The MLD1N06CL is designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontrol unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in−rush current or a shorted load condition could occur.

This Logic Level Power MOSFET features current limiting for short circuit protection, integrated Gate−Source clamping for ESD protection and integral Gate−Drain clamping for over−voltage protection and technology for low on−resistance. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal Gate−Source and Gate−Drain clamps allow the device to be applied without use of external transient suppression components. The Gate−Source clamp protects the MOSFET input from electrostatic voltage stress up to 2.0 kV. The Gate−Drain clamp protects the MOSFET drain from the avalanche stress that occurs with inductive loads. Their unique design provides voltage clamping that is essentially independent of operating temperature.

Features

- Pb−Free Package is Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	Clamped	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	Clamped	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±10	Vdc
Drain Current − Continuous − Single Pulse	I_D I_{DM}	Self−limited 1.8	Adc Apk
Total Power Dissipation	P_D	40	W
Operating and Storage Temperature Range	T_J, T_{stg}	−50 to 150	°C
Electrostatic Discharge Voltage (Human Model)	ESD	2.0	kV

THERMAL CHARACTERISTICS

Thermal Resistance Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 3.12 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR−4 board using the minimum recommended pad size.
2. When surface mounted to an FR−4 board using the 0.5 sq.in. drain pad size.

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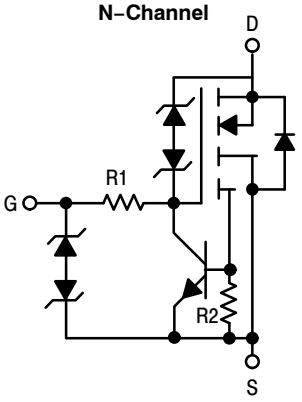
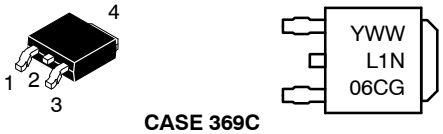
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
62 V (Clamped)	750 mΩ	1.0 A

N−Channel



MARKING DIAGRAM



CASE 369C
DPAK
STYLE 2

Y = Year
WW = Work Week
L1N06C = Device Code
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MLD1N06CLT4	DPAK	2500 Tape & Reel
MLD1N06CLT4G	DPAK (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

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UNCLAMPED DRAIN−TO−SOURCE AVALANCHE CHARACTERISTICS

Rating	Symbol	Value	Unit
Single Pulse Drain−to−Source Avalanche Energy Starting T_J = 25°C	E_{AS}	80	mJ

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Internally Clamped) (I_D = 20 mAdc, V_{GS} = 0 Vdc) (I_D = 20 mAdc, V_{GS} = 0 Vdc, T_J = 150°C)	$V_{(BR)DSS}$	 59 59	 62 62	 65 65	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 45 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 45 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	 − −	 0.6 6.0	 5.0 20	μAdc
Gate−Source Leakage Current (V_G = 5.0 Vdc, V_{DS} = 0 Vdc) (V_G = 5.0 Vdc, V_{DS} = 0 Vdc, T_J = 150°C)	I_{GSS}	 − −	 0.5 1.0	 5.0 20	μAdc
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (I_D = 250 μAdc, V_{DS} = V_{GS}) (I_D = 250 μAdc, V_{DS} = V_{GS}, T_J = 150°C)	$V_{GS(th)}$	 1.0 0.6	 1.5 –	 2.0 1.6	Vdc
Static Drain−to−Source On−Resistance (I_D = 1.0 Adc, V_{GS} = 4.0 Vdc) (I_D = 1.0 Adc, V_{GS} = 5.0 Vdc) (I_D = 1.0 Adc, V_{GS} = 4.0 Vdc, T_J = 150°C) (I_D = 1.0 Adc, V_{GS} = 5.0 Vdc, T_J = 150°C)	$R_{DS(on)}$	 − − − −	 0.63 0.59 1.1 1.0	 0.75 0.75 1.9 1.8	Ω
Static Source−to−Drain Diode Voltage (I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	−	1.1	1.5	Vdc
Static Drain Current Limit (V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc) (V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc, T_J = 150°C)	$I_{D(lim)}$	 2.0 1.1	 2.3 1.3	 2.75 1.8	Adc
Forward Transconductance (I_D = 1.0 Adc, V_{DS} = 10 Vdc)	g_{FS}	1.0	1.4	−	mhos
RESISTIVE SWITCHING CHARACTERISTICS (Note 4)					
Turn−On Delay Time	(V_{DD} = 25 Vdc, I_D = 1.0 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_{GS} = 50 Ω)	$t_{d(on)}$	−	1.2	2.0	μs
Rise Time		t_r	−	4.0	6.0	
Turn−Off Delay Time		$t_{d(off)}$	−	4.0	6.0	
Fall Time		t_f	−	3.0	5.0	
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from drain lead 0.25″ from package to center of die)	L_D	−	4.5	−	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	−	7.5	−	nH

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

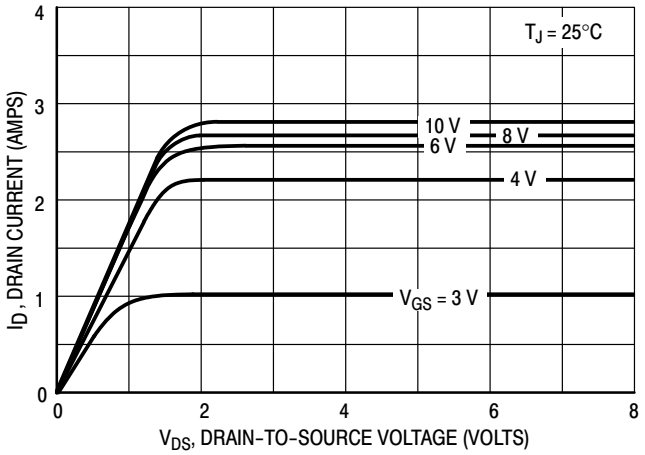


Figure 1. Output Characteristics

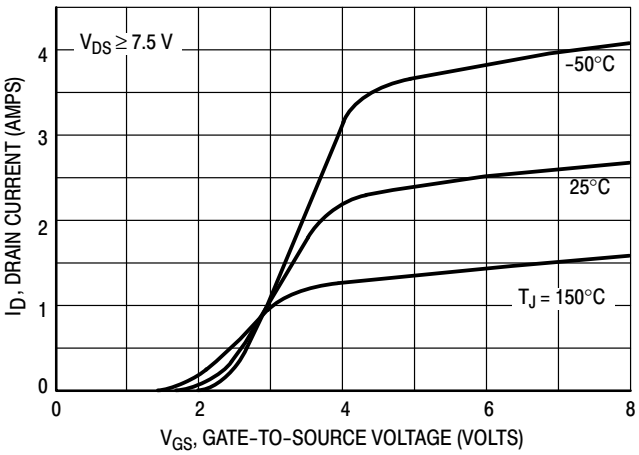


Figure 2. Transfer Function

THE CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on−chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The device functions can now provide an economical alternative to smart power ICs for power applications requiring low on−resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in−rush current or a shorted load condition could occur.

OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLD1N06CL can withstand a shorted load powered by an automotive battery (10 to 14 V) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current−limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on−chip circuitry of the MLD1N06CL offers an integrated means of protecting the MOSFET component from high in−rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate−to−source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 A at 25°C to about 1.3 A at 150°C.

Since the MLD1N06CL continues to conduct current and dissipate power during a shorted load condition, it is important to provide sufficient heatsinking to limit the device junction temperature to a maximum of 150°C.

The metal current sense resistor R2 adds about 0.4 Ω to the power MOSFET's on−resistance, but the effect of temperature on the combination is less than on a standard MOSFET due to the lower temperature coefficient of R2. The on−resistance variation with temperature for gate voltages of 4 and 5 V is shown in Figure 5.

Back−to−back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on−chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

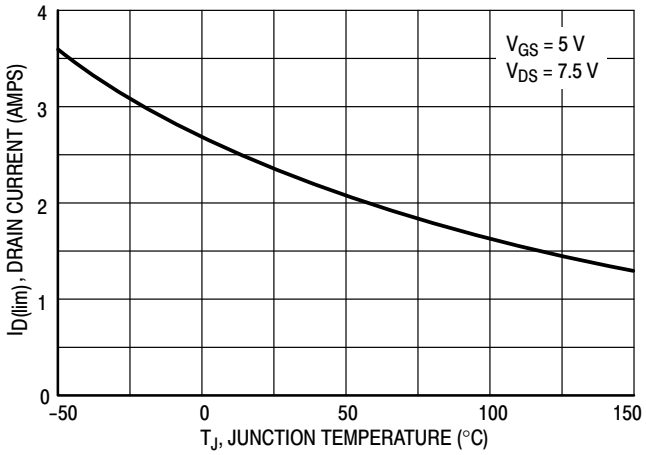


Figure 3. $I_{D(lim)}$ Variation With Temperature

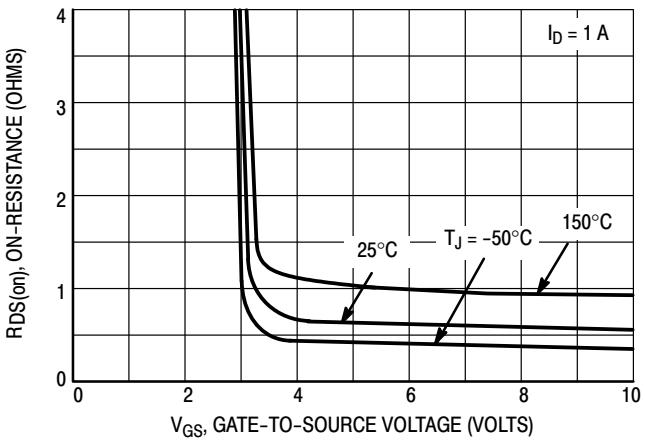


Figure 4. $R_{DS(on)}$ Variation With Gate−To−Source Voltage

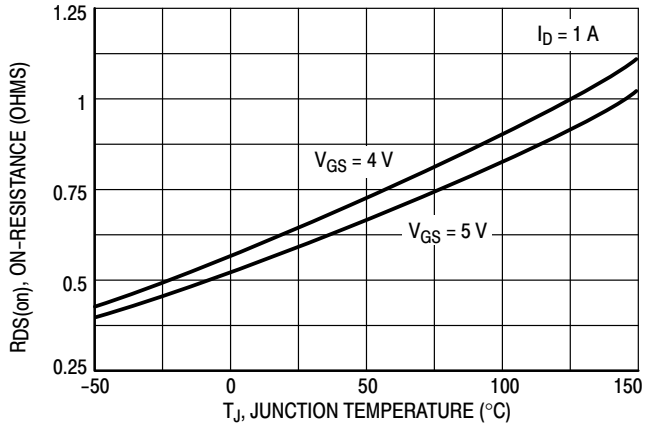


Figure 5. On−Resistance Variation With Temperature

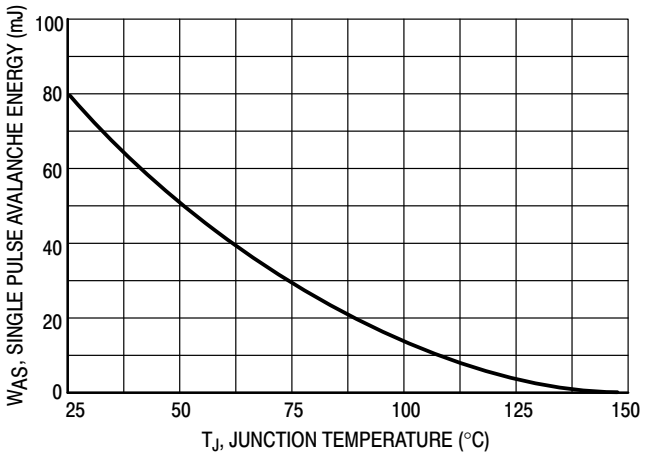


Figure 6. Single Pulse Avalanche Energy versus Junction Temperature

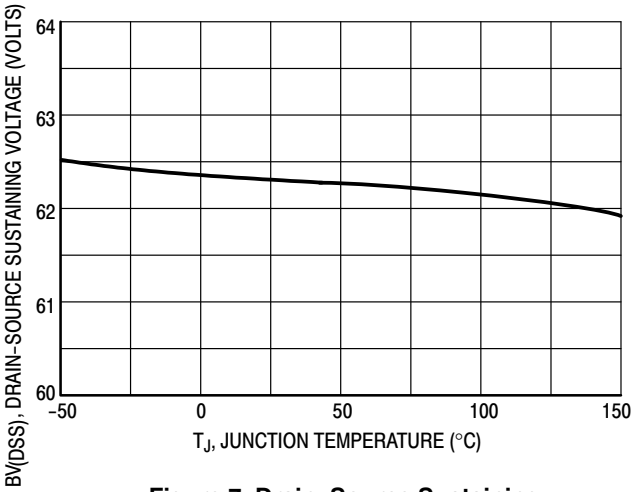


Figure 7. Drain−Source Sustaining Voltage Variation With Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance − General Data and Its Use” provides detailed instructions.

MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain−to−source voltage that can be continuously applied across the MLD1N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)} (R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of V_{DS} applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

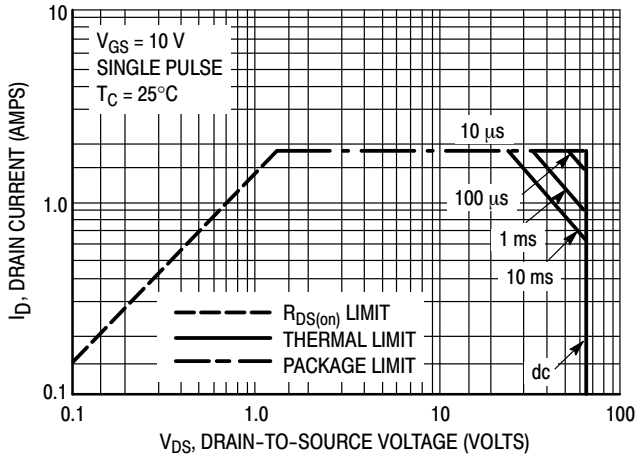


Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLD1N06CL)

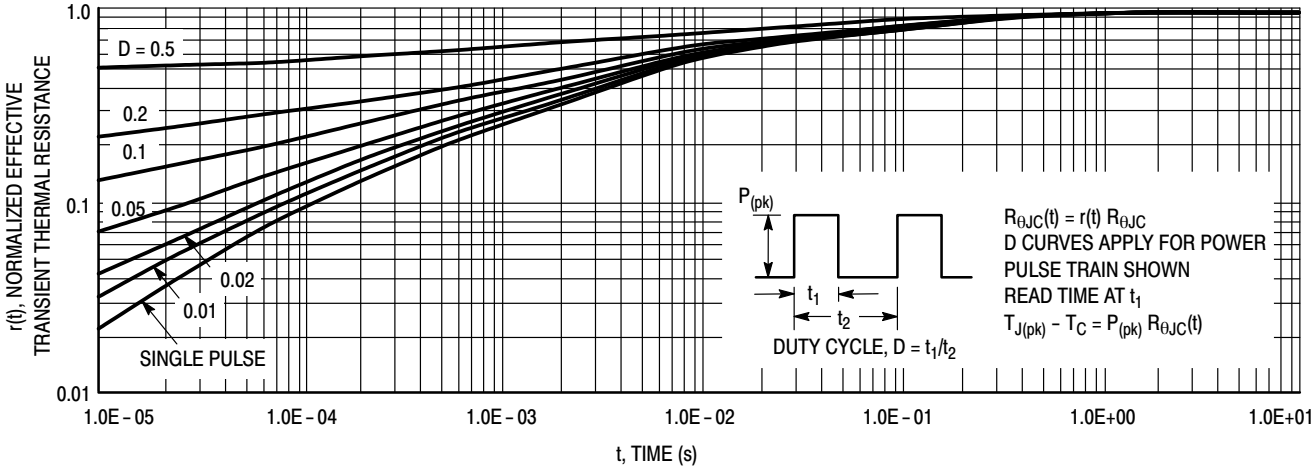


Figure 9. Thermal Response (MLD1N06CL)

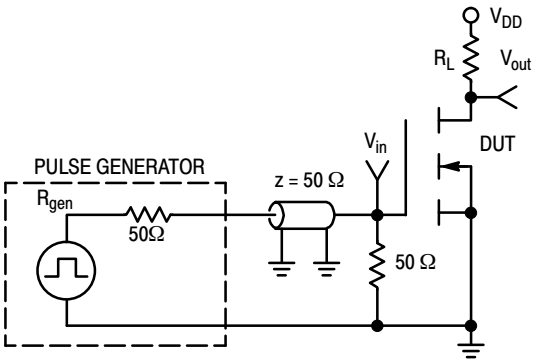


Figure 10. Switching Test Circuit

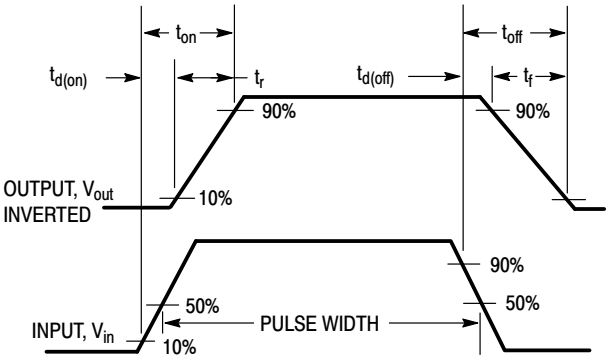


Figure 11. Switching Waveforms

ACTIVE CLAMPING

The technology can provide on−chip realization of the popular gate−to−source and gate−to−drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back−to−back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back−to−back diode element provides a temperature compensated voltage element of about 7.2 V. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

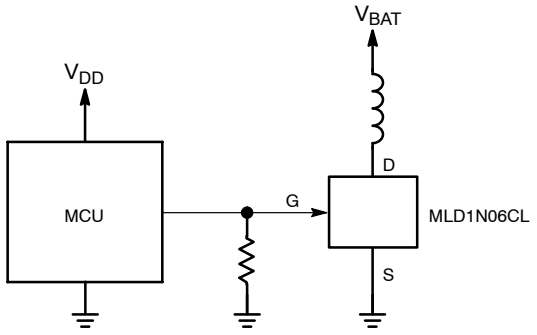
To achieve high gate−to−drain clamp voltages, several voltage elements are strung together; the MLD1N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 V gate−to−source voltage clamp. For the MLD1N06CL, the integrated gate−to−source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

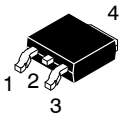
The avalanche voltage of the gate−to−drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain−to−source voltage exceeds this avalanche voltage, the resulting gate−to−drain Zener current builds a gate voltage across the gate−to−source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate−to−drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain−to−source sustaining voltage (Figure 7) effectively removes the possibility of drain−to−source avalanche in the power device.

The gate−to−drain voltage clamp technique is particularly useful for snubbing loads where the inductive energy would otherwise avalanche the power device. An improvement in ruggedness of at least four times has been observed when inductive energy is dissipated in the gate−to−drain clamped conduction mode rather than in the more stressful gate−to−source avalanche mode.

TYPICAL APPLICATIONS: INJECTOR DRIVER, SOLENOIDS, LAMPS, RELAY COILS

The MLD1N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.

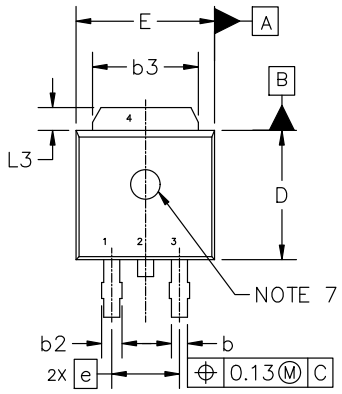




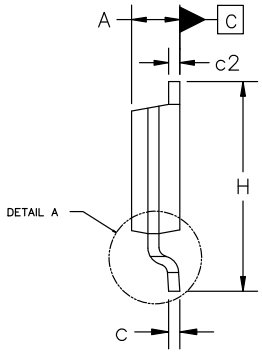
DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

SCALE 1:1

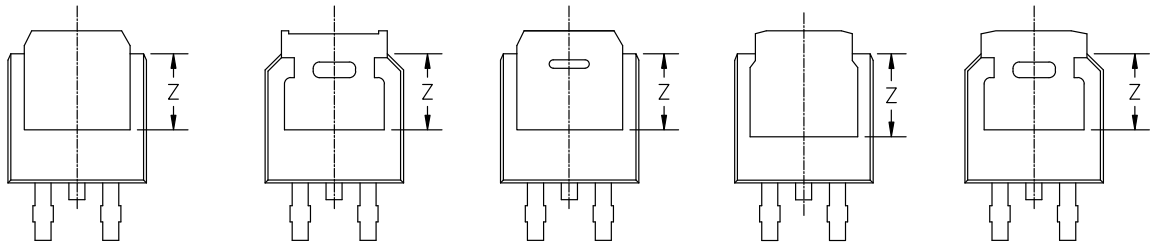


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−

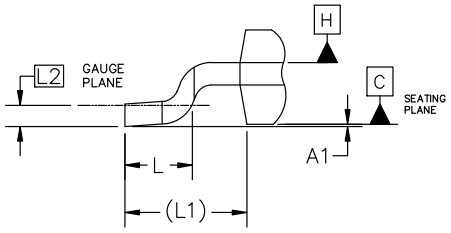


BOTTOM VIEW

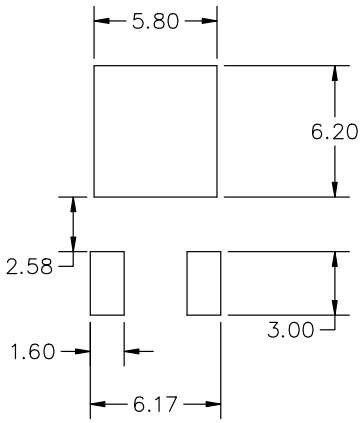
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

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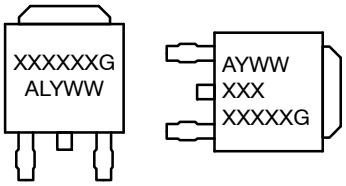
DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 13 MAY 2026

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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