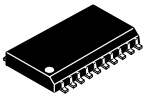
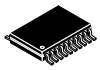
Inverting Octal 3-STATE Buffer

MM74HC240



SOIC−20 WB
CASE 751D−05



TSSOP−20 WB
CASE 948E

General Description

The MM74HC240 3−STATE buffer utilizes advanced silicon−gate CMOS technology. It possesses high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. It has a fanout of 15 LS−TTL equivalent inputs.

The MM74HC240 is an inverting buffer and has two active LOW enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical Propagation Delay: 12 ns
- 3−STATE Outputs for Connection to System Buses
- Wide Power Supply Range: 2–6 V
- Low Quiescent Supply Current: 160 μA (74 Series)
- Output Current: 6 mA
- These are Pb−Free Devices

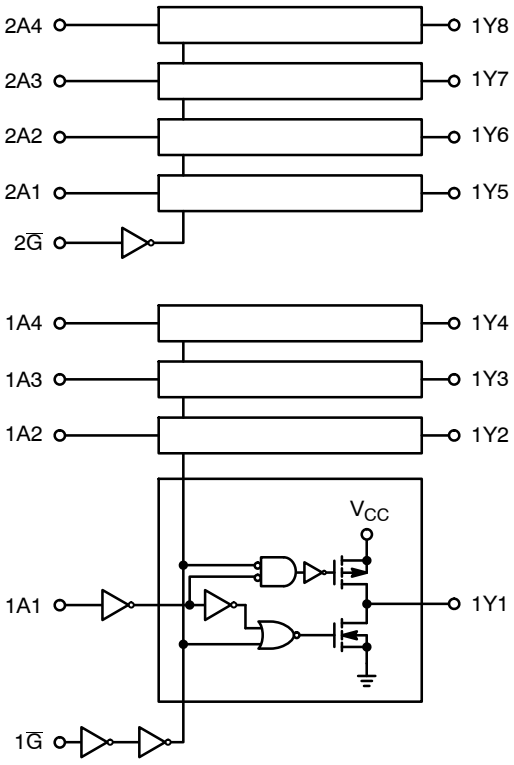
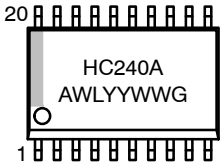
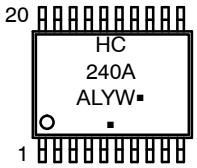


Figure 1. Logic Diagram

MARKING DIAGRAMS



(SOIC−20 WB)

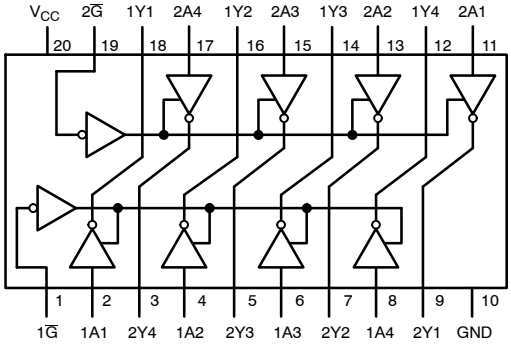


(TSSOP−20 WB)

HC240A	= Specific Device Code
A	= Assembly Location
L/WL	= Wafer Lot
Y/YY	= Year
W/WW	= Work Week
▪ or G	= Pb−Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



(Top View)

TRUTH TABLE

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = HIGH Level
L = LOW Level
Z = HIGH Impedance

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC VCC or GND Current, per Pin	±70	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
P_D	Power Dissipation (Note 2) S. O. Package Only	 600 500	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating − plastic “N” package: 12 mW/°C from 65°C to 85°C.

RECOMMENDED OPERATIONG CONDITIONS (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	 − − −	 1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	−40°C ≤ T_A ≤ 85°C	−55°C ≤ T_A ≤ 125°C	Unit
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0 4.5 6.0	− − −	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0 4.5 6.0	− − −	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0 mA $\|I_{OUT}\|$ ≤ 7.8 mA	 4.5 6.0	 4.2 5.7	 3.98 5.48	 3.84 5.34	 3.7 5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0 mA $\|I_{OUT}\|$ ≤ 7.8 mA	 4.5 6.0	 0.2 0.2	 0.26 0.26	 0.33 0.33	 0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0	−	±0.1	±1.0	±1.0	μA

DC ELECTRICAL CHARACTERISTICS (Note 3) (continued)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	−40°C ≤ T_A ≤ 85°C	−55°C ≤ T_A ≤ 125°C	Unit
				Typ	Guaranteed Limits		
I_{OZ}	Maximum 3−STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}, G = V_{IL}	6.0	–	±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0	–	8.0	80	160	μA

3. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	R_L = 1 kΩ, C_L = 45 pF	14	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	R_L = 1 kΩ, C_L = 5 pF	13	25	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.0 V to 6.0 V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified))

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	−40°C ≤ T_A ≤ 85°C	−55°C ≤ T_A ≤ 125°C	Unit
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF C_L = 150 pF	2.0 2.0	55 80	100 150	126 190	149 224	ns
		C_L = 50 pF C_L = 150 pF	4.5 4.5	12 22	20 30	25 38	30 45	ns
		C_L = 50 pF C_L = 150 pF	6.0 6.0	11 28	17 26	21 32	25 38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF C_L = 150 pF	 2.0 2.0	 75 100	 150 200	 189 252	 224 298	ns
		C_L = 50 pF C_L = 150 pF	4.5 4.5	15 20	30 40	38 50	45 60	ns
		C_L = 50 pF C_L = 150 pF	6.0 6.0	13 17	26 34	32 43	38 51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0 4.5 6.0	75 15 13	150 30 26	189 38 32	224 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0 4.5 6.0	– – –	60 12 10	75 15 13	90 18 15	ns
C_{PD}	Power Dissipation Capacitance (Note 4)	(per buffer) $\overline{G}$ = V_{IH} $\overline{G}$ = V_{IL}	 – –	 12 50	 – –	 – –	 – –	pF
C_{IN}	Maximum Input Capacitance		–	5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		–	10	20	20	20	pF

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \cdot V_{CC}^2 \cdot f + I_{CC} \cdot V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \cdot V_{CC} \cdot f + I_{CC}$.

ORDERING INFORMATION

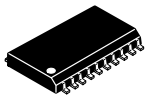
Device	Package	Shipping†
MM74HC240WM	SOIC−20 WB (Pb−Free)	38 Units / Tube
MM74HC240WMX	SOIC−20 WB (Pb−Free)	1000 Units / Tape & Reel
MM74HC240MTCX	TSSOP−20 WB (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

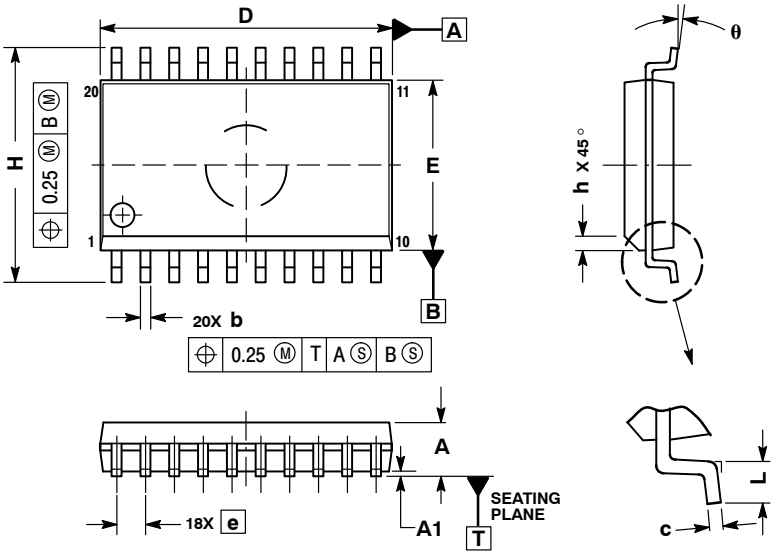
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



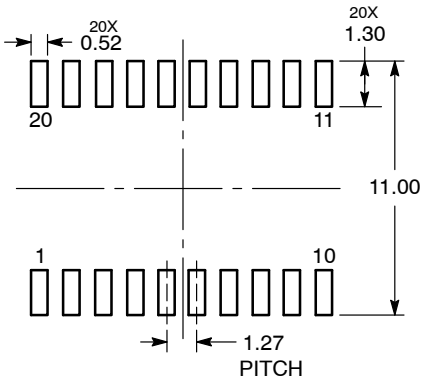
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

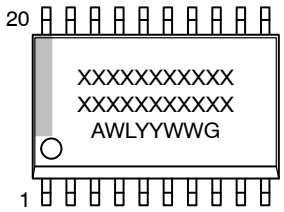
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

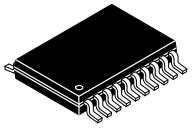
DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−20 WB**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

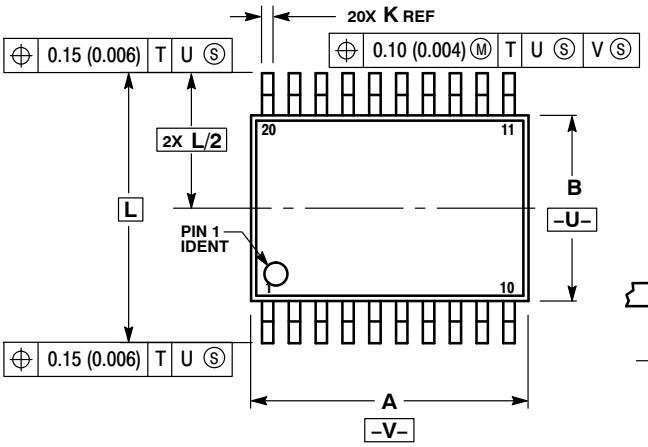
ON Semiconductor®

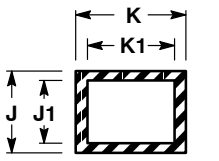
TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

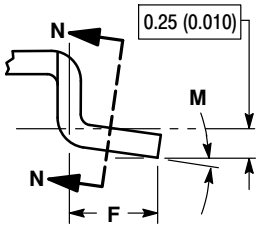


SCALE 2:1

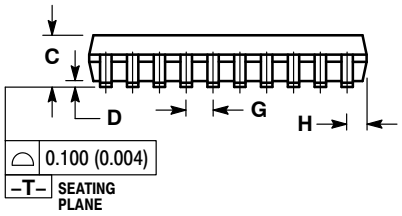


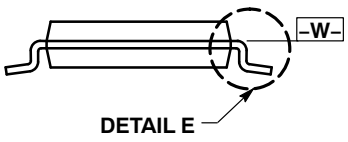


SECTION N−N



DETAIL E

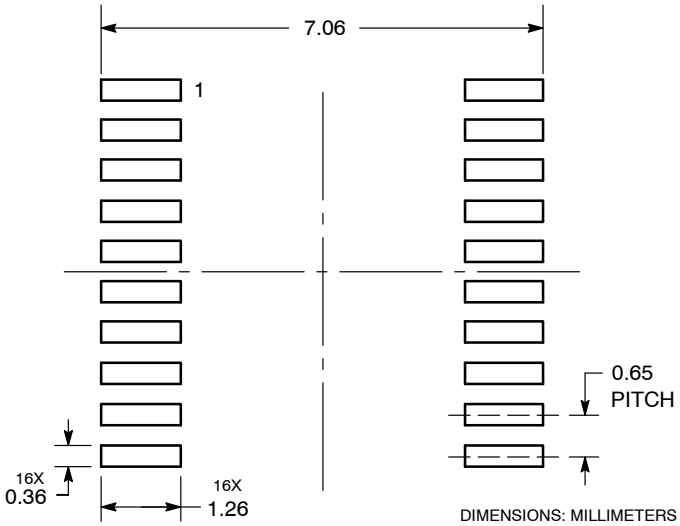




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

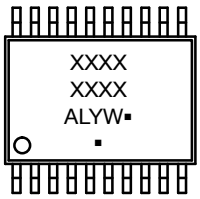
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSSOP−20 WB	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales