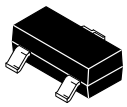
Switch – N-Channel

MMBF5103

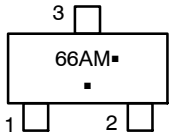


SOT–23
CASE 318–08

Features

- This Device is Designed for Low Level Analog Switching, Sample and Hold Circuits and Chopper Stabilized Amplifiers
- Sourced from Process 51
- See J111 for Characteristics
- This is a Pb–Free and Halide Free Device

MARKING DIAGRAM



1. Drain
2. Source
3. Gate

66A = Specific Device Code
M = Date Code
▪ = Pb–Free Package

ABSOLUTE MAXIMUM RATINGS

(Values are at T_A = 25°C unless otherwise noted.) (Notes 1 and 2)

Symbol	Parameter	Value	Unit
V_{DG}	Drain–Gate Voltage	40	V
V_{GS}	Gate–Source Voltage	–40	V
I_{GF}	Forward Gate Current	50	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady–state limits. **onsemi** should be consulted on applications involving pulsed or low–duty–cycle operations.

ORDERING INFORMATION

Device	Package	Shipping
MMBF5103	SOT–23 (Pb–Free / Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS (Values are at T_A = 25°C unless otherwise noted.) (Note 3)

Symbol	Parameter	Value	Unit
P_D	Total Device Dissipation	350	mW
	Derate Above 25°C	2.8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient	357	°C/W

3. Device mounted on FR–4 PCB 36 mm × 18 mm × 1.5 mm; mounting pad for the collector lead minimum 6 cm^2.

ELECTRICAL CHARACTERISTICS Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Max	Unit
OFF CHARACTERISTICS					
$V_{(BR)GSS}$	Gate–Source Breakdown Voltage	I_G = 1.0 μA, V_{DS} = 0	–40	–	V
I_{GSS}	Gate Reverse Current	V_{GS} = –15 V, V_{DS} = 0	–	–200	pA
		V_{GS} = –15 V, V_{DS} = 0, T_A = 125°C	–	–500	nA
V_{GS}(off)	Gate–Source Cut–Off Voltage	V_{DS} = 20 V, I_D = 1.0 nA	–1.2	–2.7	V
V_{GS}(f)	Gate–Source Forward Voltage	I_G = 1.0 mA, V_{DS} = 0	–	1.0	V
ON CHARACTERISTICS					
I_{DSS}	Zero–Gate Voltage Drain Current (Note 4)	V_{DS} = 15 V, V_{GS} = 0	10	40	mA
SMALL SIGNAL CHARACTERISTICS					
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz	–	16	pF
C_{rss}	Reverse Transfer Capacitance	V_{GS} = –15 V, f = 1.0 MHz	–	6.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse test with PW = 300 μs, 1% duty cycle.

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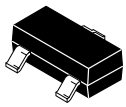
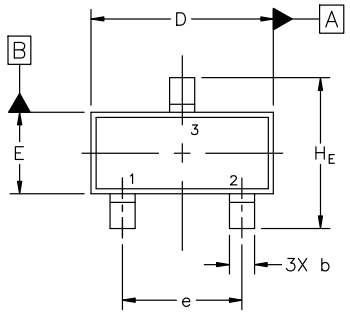


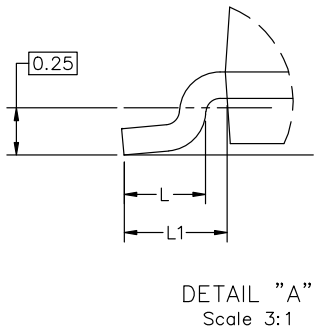
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

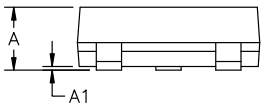
DATE 14 AUG 2024



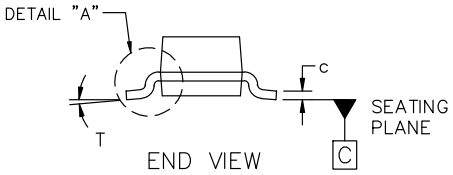
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

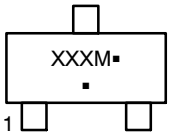


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

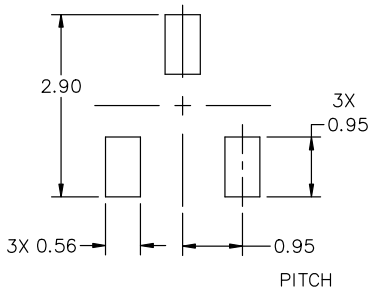
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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