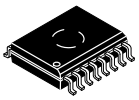
Isolated Dual Channel IGBT Gate Driver

NCD57530, NCV57530, NCD57540, NCV57540



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SOIC−16 WB
CASE 752AJ

NCx575y0 are high−current two channel isolated IGBT gate drivers with 5 kV_{rms} internal galvanic isolation from input to each output and functional isolation between the two output channels. The device accepts 3.3 V to 20 V bias voltage and signal levels on the input side and up to 32 V bias voltage on the output side. The device accepts complementary inputs and offers separate pins for Disable (NCx57540) or Enable (NCx57530) and Dead Time control for system design convenience. Drivers are available in CASE 752AJ SOIC−16 wide body package with increased insulation between channels (less pin 12 & 13) .

Features

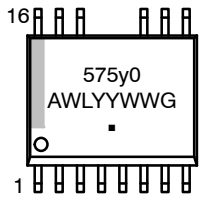
- High Peak Output Current (±6.5 A)
- Configurable as a Dual Low−Side or Dual High−Side or Half−Bridge Driver
- Programmable Overlap or Dead Time control
- Disable Pin to Turn Off Outputs for Power Sequencing (NCx57540)
- Enable Pin for Independent Driver Control (NCx57530)
- IGBT Gate Clamping during Short Circuit
- Short Propagation Delays with Accurate Matching
- Tight UVLO Thresholds on all Power Supplies
- 3.3 V, 5 V, and 15 V Logic Input
- 5 kV_{rms} Galvanic Isolation from Input to each Output and 1.5 kV_{rms} Differential Voltage between Output Channels
- 1200 V Working Voltage (per VDE0884−11 Requirements)
- High Common Mode Transient Immunity
- Case 752AJ for Improved Insulation Between Output Channels
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Typical Applications

- EV Chargers
- Motor Control
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- Solar Inverters
- Automotive Applications

MARKING DIAGRAMS

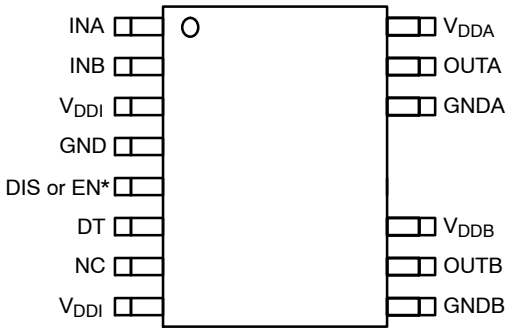
CASE 752AJ



575y0	= Specific Device Code
y	= 3 or 4
A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Package

(See page 21)

PIN CONNECTIONS



NCx575y0
x = D or V
y = 3 or 4

* depends on variant

ORDERING INFORMATION

See detailed ordering and shipping information on page 21 of this data sheet.

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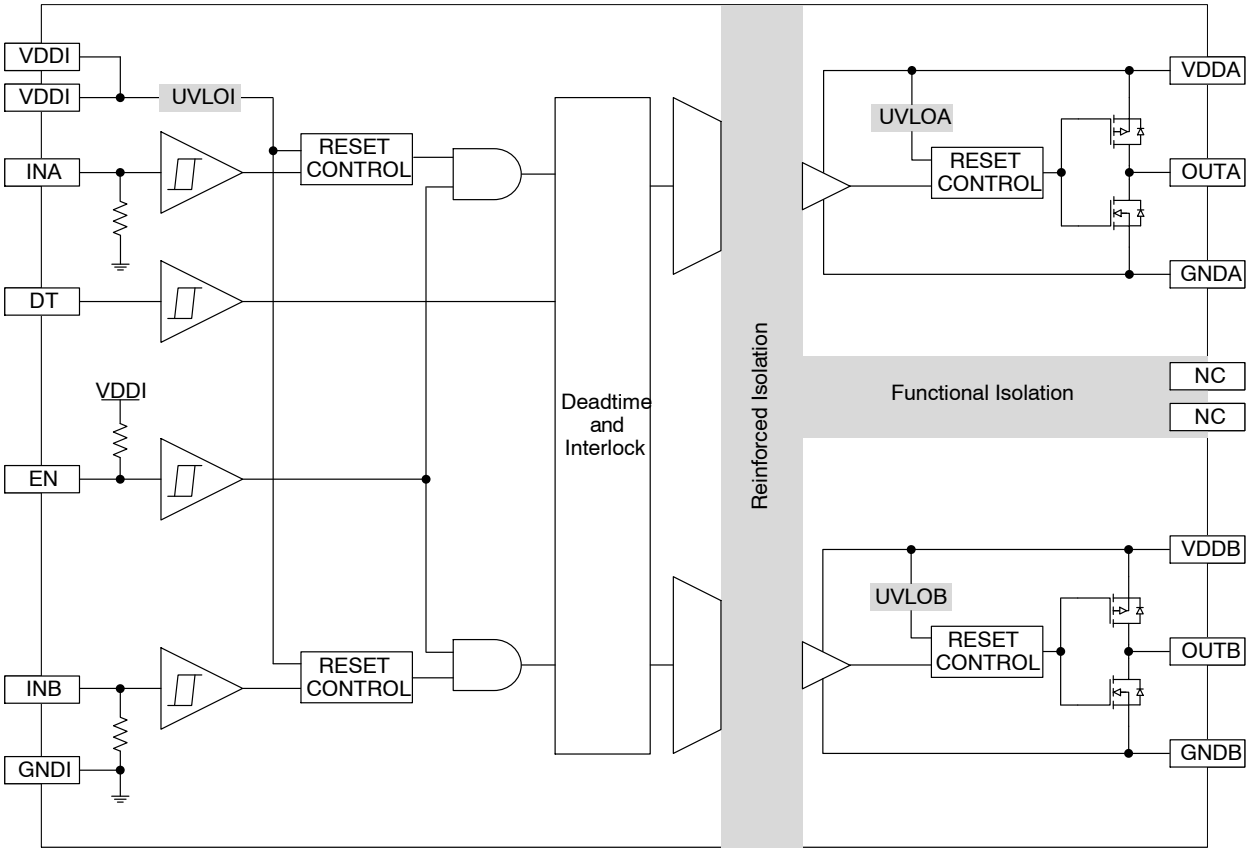
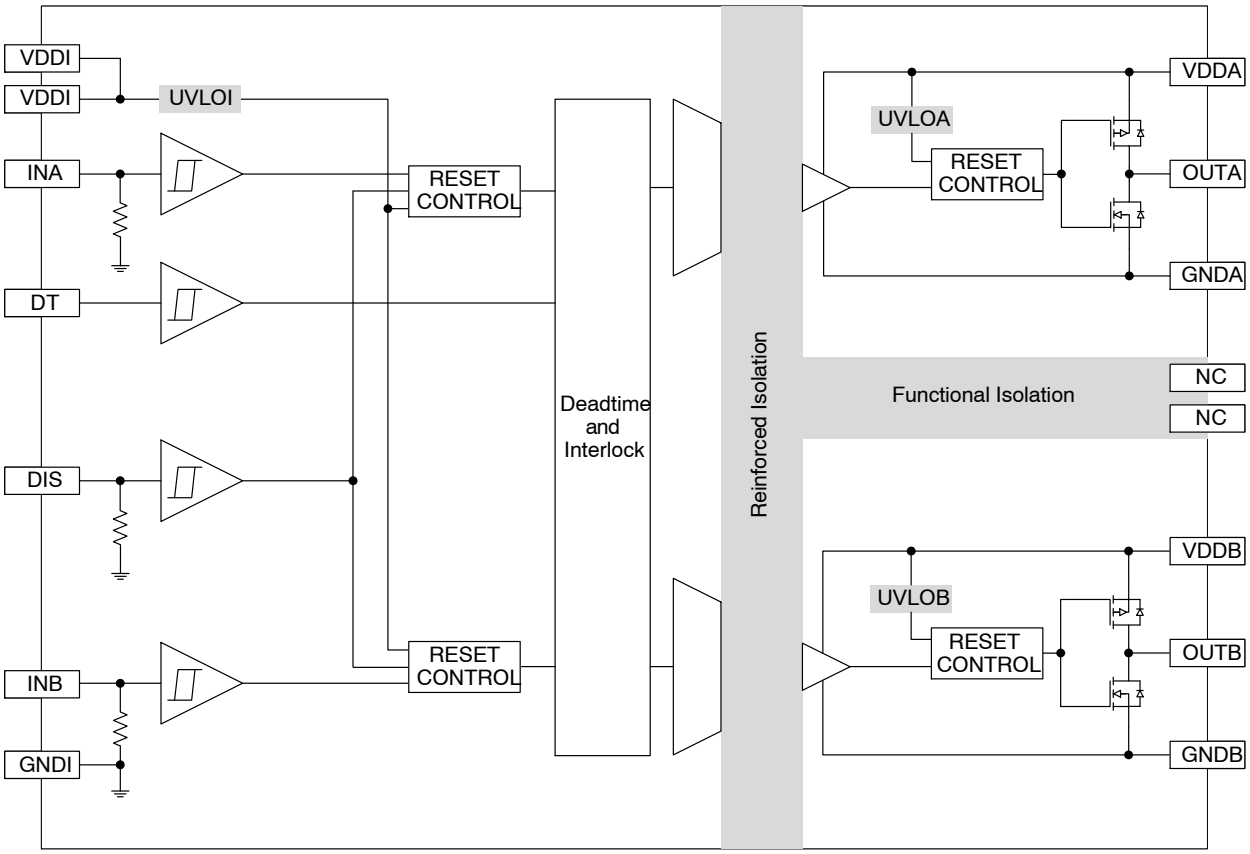
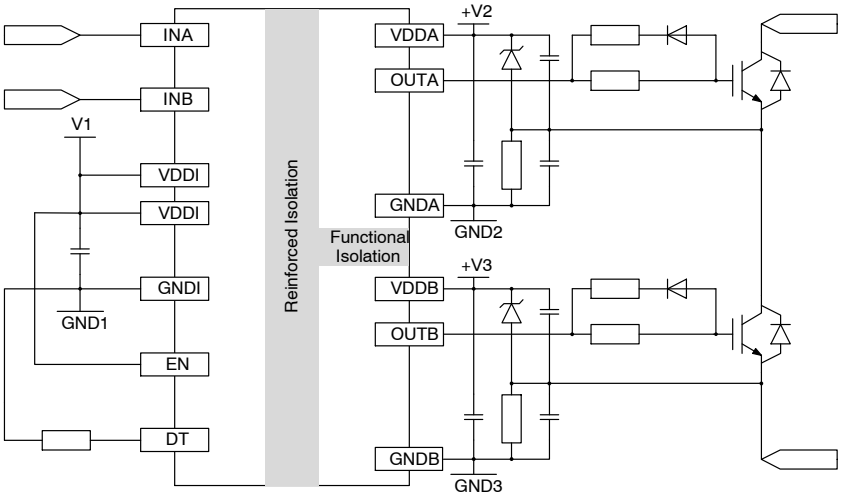


NCx57530

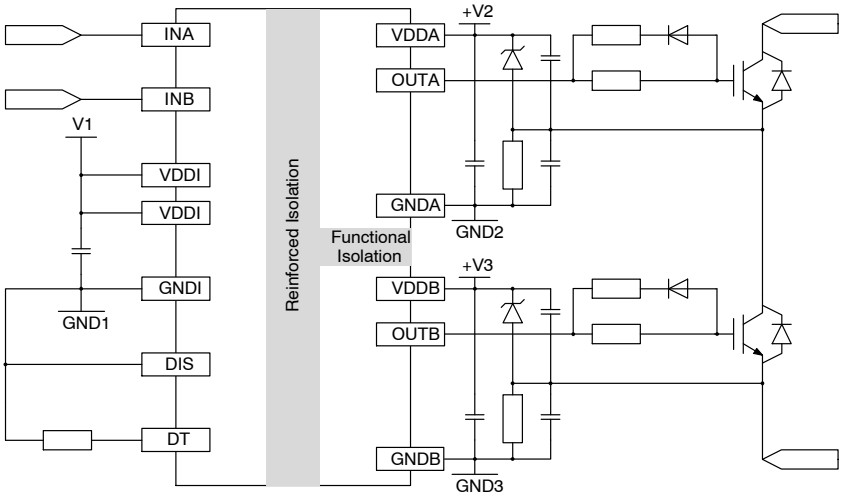


NCx57540

Figure 1. Simplified Block Diagram

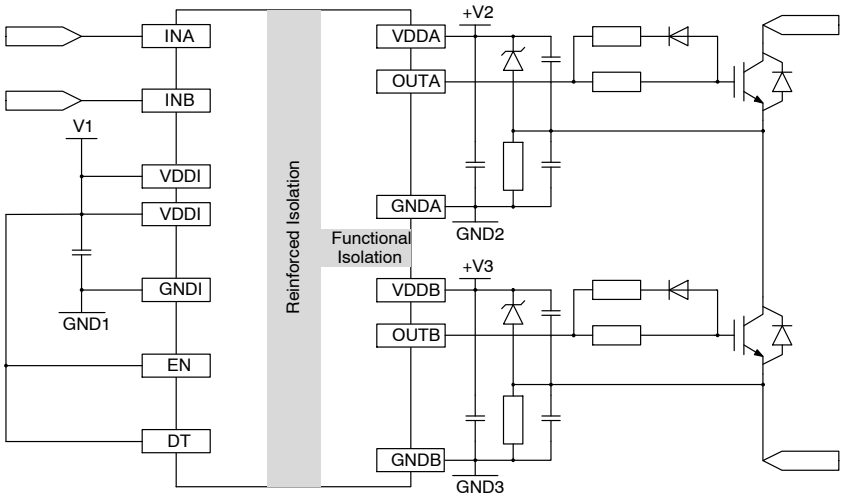


NCx57530

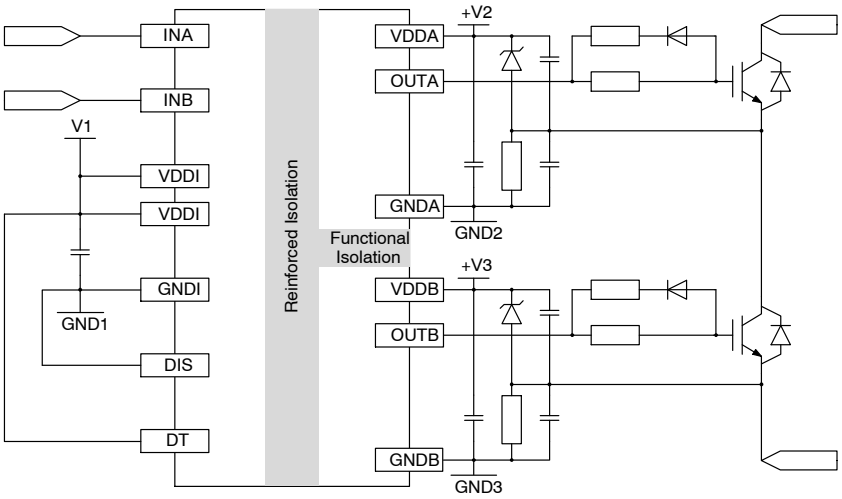


NCx57540

Figure 2. Typical Application, High and Low Side IGBT Gate Drive (Dead Time added)



NCx57530



NCx57540

Figure 3. Typical Application, Two Channels IGBT Gate Drive (no added Dead Time)

Table 1. FUNCTION DESCRIPTION

Pin Name	No.	I/O	Description
INA	1	Input	A non-inverting gate driver input that defines OUTA. It has an equivalent pull−down resistor of 125 kΩ to ensure that output is low in the absence of an input signal. A positive or negative going pulse with pulse width longer than maximum value of t_{MIN2} is required at INA before OUTA reacts. The input logic levels scale with V_{DDI} up to V_{DDI} = 5 V. With V_{DDI} above 5 V the input logic levels stay the same as for V_{DDI} = 5 V. Maximum voltage on this pin is V_{DDI}.
INB	2	Input	A non−inverting gate driver input that defines OUTB. It has an equivalent pull−down resistor of 125 kΩ to ensure that output is low in the absence of an input signal. A positive or negative going pulse with pulse width longer than maximum value of t_{MIN2} is required at INB before OUTB reacts. The input logic levels scale with V_{DDI} up to V_{DDI} = 5 V. With V_{DDI} above 5 V the input logic levels stay the same as for V_{DDI} = 5 V. Maximum voltage on this pin is V_{DDI}.
V_{DDI}	3, 8	Power	Low voltage side power supply. A good quality bypassing capacitor is required from this pin to GND and should be placed close to the pins for best results. The under voltage lockout (UVLOI) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLOI-OUT-ON}$ is present. Please see Figure 7 and 8 for more details.
GNDI	4	Power	Low voltage side ground.
DIS	5	Input	A high level on disable pin turns both OUTA and OUTB low simultaneously regardless of the states of INA, INB and DT. Minimum pulse width filter and propagation delays apply. It has an equivalent pull−down resistor of 125 kΩ to ensure that OUTA and OUTB react to INA, INB and DT in the absence of an input signal. The input logic levels scale with V_{DDI} up to V_{DDI} = 5 V. With V_{DDI} above 5 V the input logic levels stay the same as for V_{DDI} = 5 V. Maximum voltage on this pin is V_{DDI}.
EN	5	Input	Enable input allows additional gating of OUT, and can be used when the driver output needs to be turned off independent of the Microcontroller input. A low level on enable pin turns both OUTA and OUTB low simultaneously regardless of the states of INA, INB and DT. It has an equivalent pull−up resistor of 125 kΩ to ensure that OUTA and OUTB react to INA, INB and DT in the absence of an input signal. The input logic levels scale with V_{DDI} up to V_{DDI} = 5 V. With V_{DDI} above 5 V the input logic levels stay the same as for V_{DDI} = 5 V. Maximum voltage on this pin is V_{DDI}.
DT	6	Input	A deadtime pin is used to configure the two outputs sequence. The deadtime (t_{DT}) and interlocking logic between INA and INB is defined by the value of the external resistor (R_{DT}) connected between DT pin and GNDI. The deadtime can be estimated as t_{DT} (ns) ≈ 10 x R_{DT} (kΩ). If DT pin is pulled up to VDDI for disabling the deadtime and interlocking logic the OUTA and OUTB can be high simultaneously. Minimum deadtime will be observed between OUTA and OUTB when DT pin is left floating. Allowed resistance between this pin and GNDI is in range of 5 to 500 kΩ. Maximum voltage on this pin is V_{DDI}. Corresponding waveforms are on Figure 4.
GNDB	9	Power	Ground for channel B.
OUTB	10	Output	Output of channel B on the high voltage side. It has galvanic isolation from low voltage side and from channel A. OUTB provides the appropriate drive voltage and source/sink current to the IGBT gate. OUTB is actively pulled low during startup, when DIS is high and under UVLOB, UVLOI condition. There is interlocking logic that prevents OUTA and OUTB cross conduction when DT pin is not connected to V_{DDI}.
V_{DDB}	11	Power	High voltage side power supply for channel B. A good quality bypassing capacitor is required from this pin to GNDB and should be placed close to the pins for best results. The under voltage lockout (UVLOB) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLOB-OUT-ON}$ is present. Please see Figure 9 and 10 for more details.
NC	7,12*, 13*	–	Not connected internally. (* Presence of pins depends on the type of case, see Page 21.)
GNDA	14	Power	Ground for channel A.
OUTA	15	Output	Output of channel A on the high voltage side. It has galvanic isolation from low voltage side and from channel B. OUTA provides the appropriate drive voltage and source/sink current to the IGBT gate. OUTA is actively pulled low during startup, when DIS is high and under UVLOA, UVLOI condition. There is interlocking logic that prevents OUTA and OUTB cross conduction when DT pin is not connected to V_{DDI}.
V_{DDA}	16	Power	High voltage side power supply for channel A. A good quality bypassing capacitor is required from this pin to GNDA and should be placed close to the pins for best results. The under voltage lockout (UVLOA) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLOA-OUT-ON}$ is present. Please see Figure 9 and 10 for more details.

Table 2. SAFETY AND INSULATION RATINGS

Symbol	Parameter		Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I–IV	–
		< 300 V_{RMS}	I–IV	–
		< 450 V_{RMS}	I–IV	–
		< 600 V_{RMS}	I–IV	–
		< 1000 V_{RMS}	I–III	–
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	–
	Climatic Classification		40/125/21	–
	Pollution Degree (DIN VDE 0110/1.89)		2	–
V_{PR}	Input−to−Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC		2250	V_{PK}
V_{IORM}	Maximum Working Insulation Voltage		1200	V_{PK}
V_{IOWM}	Maximum Working Insulation Voltage		870	V_{RMS}
V_{IOTM}	Highest Allowable Over Voltage		8400	V_{PK}
E_{CR}	External Creepage		8.0	mm
E_{CL}	External Clearance		8.0	mm
DTI	Insulation Thickness		17.3	μm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature		150	°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power		264	mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power		1136	mW
R_{IO}	Insulation Resistance at TS, V_{IO} = 500 V		10^9	Ω

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1) Over operating free−air temperature range unless otherwise noted

Symbol	Parameter	Minimum	Maximum	Unit
V_{DDI}–GNDI	Supply voltage, low voltage side	−0.3	22	V
V_{DDA}–GNDA	Supply voltage, high voltage side, channel A	−0.3	36	V
V_{DDB}–GNDB	Supply voltage, high voltage side, channel B	−0.3	36	V
V_{OUTA}	Gate driver output voltage, channel A	GNDA − 0.3	V_{DDA} + 0.3	V
V_{OUTB}	Gate driver output voltage, channel B	GNDB − 0.3	V_{DDB} + 0.3	V
I_{PK-SRC}	Gate−driver output sourcing current (maximum pulse width = 10 μs, minimum period = 5 ms, V_{DDA} – GNDA = V_{DDB} – GNDB = 15 V)	–	6.5	A
I_{PK-SNK}	Gate−driver output sinking current (maximum pulse width = 10 μs, minimum period = 5 ms, V_{DDA} – GNDA = V_{DDB} – GNDB = 15 V)	–	6.5	A
t_{CLP}	Maximum Short Circuit Clamping Time (I_{OUTA_CLAMP} = I_{OUTB_CLAMP} = 500 mA)	–	10	μs
V_{LIM}–GNDI	Voltage at INA, INB, DIS, DT	−0.3	V_{DDI} + 0.3	V
PD	Power Dissipation (Note 3)	–	1060	mW
T_J(max)	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
ESDHBM	ESD Capability, Human Body Model (Note 4)	–	±4	kV
ESDCDM	ESD Capability, Charged Device Model (Note 4)	–	±2	kV
MSL	Moisture Sensitivity Level	–	1	–
T_{SLD}	Lead Temperature Soldering Reflow, Pb−Free Versions (Note 5)	–	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. The minimum value is verified by characterization with a single pulse of 100 mA for 100 μs.
3. The value is estimated for ambient temperature 25°C and junction temperature 150°C, 650 mm^2, 1 oz copper, 2 surface layers and 2 internal power plane layers. Power dissipation is affected by the PCB design and ambient temperature.

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 25°C.
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 4. THERMAL CHARACTERISTICS

Parameter	Conditions	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air	100 mm², 2 oz Copper, 1 Surface Layer	$R_{\theta JA}$	81	°C/W
	100 mm², 2 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers		57	

Table 5. RECOMMENDED OPERATING RANGES (Note 6)

Symbol	Parameter	Minimum	Maximum	Unit
V_{DDI}−GNDI	Supply voltage, low voltage side	UVLOI	20	V
V_{DDA}−GNDA	Supply voltage, high voltage side, channel A	UVLOA	32	V
V_{DDB}−GNDB	Supply voltage, high voltage side, channel B	UVLOB	32	V
V_{IN}	Logic Input Voltage at INA, INB, DIS, DT	GNDI	V_{DDI}	V
$\lvert dV_{ISO}/dt \rvert$	Common Mode Transient Immunity (CMTI)	100	–	kV/μs
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 6. ISOLATION CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ISO, INPUT TO OUTPUT}$	Input−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} 10 A, 50 Hz (Notes 7, 8, 9)	5000	–	–	V_{RMS}
$V_{ISO, OUTPUT TO OUTPUT}$	Output−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} 10 A, 50 Hz (Notes 7, 8, 9)	1500	–	–	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 7)	10^{11}	–	–	Ω

7. Device is considered a two−terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
8. 5,000 V_{RMS} for 1−minute duration is equivalent to 6,000 V_{RMS} for 1−second duration.
9. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN VDE V 0884−11 Safety and Insulation Ratings Table.

Table 7. ELECTRICAL CHARACTERISTICS V_{DDI} = 5V, V_{DDA} = V_{DDB} = 15 V

For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOLTAGE SUPPLY						
$V_{UVLOI−OUT−ON}$	V_{DDI} Supply Under Voltage Output Enabled		–	–	3.1	V
$V_{UVLOI−OUT−OFF}$	V_{DDI} Supply Under Voltage Output Disabled		2.4	–	–	V
$V_{UVLOI−HYST}$	V_{DDI} Supply Voltage Output Enabled/Disabled Hysteresis		0.1	–	–	V
$V_{UVLOA−OUT−ON}$ $V_{UVLOB−OUT−ON}$	V_{DDA}/V_{DDB} Supply Under Voltage Output Enabled		12.4	12.9	13.4	V
$V_{UVLOA−OUT−OFF}$ $V_{UVLOB−OUT−OFF}$	V_{DDA}/V_{DDB} Supply Under Voltage Output Disabled		11.5	12	12.5	V
$V_{UVLOA/B−HYST}$	V_{DDA}/V_{DDB} Supply Voltage Output Enabled/Disabled Hysteresis		0.8	1.0	–	V
$I_{QDDI−0}$	Low Voltage Side Quiescent Current	V_{INA} = V_{INB} = 0 V	–	–	2	mA

Table 7. ELECTRICAL CHARACTERISTICS (continued) V_{DDI} = 5V, V_{DDA} = V_{DDB} = 15 V
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOLTAGE SUPPLY						
$I_{QDDI-50}$	Low Voltage Side Operating Current at 50% Duty Cycle	INA PWM, INB Low (or INA Low, INB PWM), f = 200 kHz	–	–	4	mA
$I_{QDDI-100}$	Low Voltage Side Operating Current at 100% Duty Cycle	INA or INB High	–	–	6.5	mA
I_{QDDA-0}, I_{QDDB-0}	High Voltage Side Quiescent Current	V_{INA} = V_{INB} = 0 V, Current per Channel	–	–	2	mA
$I_{QDDA-50}$, $I_{QDDB-50}$	High Voltage Side Operating Current at 50% Duty Cycle	Current per Channel, f = 200 kHz, C_G = 1 nF (see Figure 18)	–	–	10	mA
$I_{QDDA-100}$, $I_{QDDB-100}$	High Voltage Side Operating Current at 100% Duty Cycle	Current per Channel	–	–	2	mA
LOGIC INPUT						
V_{INAL}, V_{INBL}, V_{DISL}, V_{ENL}	Low Level Input Voltage	Level scale for V_{DDI} = 3.3 to 5 V for V_{DDI} > 5 V is the same as for V_{DDI} = 5 V	–	–	0.3 × V_{DDI}	V
V_{INAH}, V_{INBH}, V_{DISH}, V_{ENH}	High Level Input Voltage	Level scale for V_{DDI} = 3.3 to 5 V for V_{DDI} > 5 V is the same as for V_{DDI} = 5 V	0.7 × V_{DDI}	–	–	V
$V_{INA-HYS}$, $V_{INB-HYS}$, $V_{DIS-HYS}$, V_{EN-HYS}	Input Hysteresis	Level scale for V_{DDI} = 3.3 to 5 V for V_{DDI} > 5 V is the same as for V_{DDI} = 5 V	–	0.15 × V_{DDI}	–	V
V_{INAN}, V_{INBN}, V_{DISN}, V_{ENN} (Note 10)	Negative Input Transient	50 ns	–5	–	–	V
I_{INAH}, I_{INBH}, I_{DISH}	Logic “1” Input Bias Current	V_{INA} = V_{INB} = V_{DIS} = V_{DDI} = 3.3 V	–	50	–	μA
I_{INAH}, I_{INBH}, I_{DISH}	Logic “1” Input Bias Current	V_{INA} = V_{INB} = V_{DIS} = V_{DDI} = 20 V	–	50	–	μA
I_{INAL}, I_{INBL}, I_{DISL}	Logic “0” Input Bias Current	V_{INA} = V_{INB} = V_{DIS} = 0 V	–	1	–	μA
I_{ENH}	Logic “1” Input Bias Current	V_{INA} = V_{INB} = V_{EN} = V_{DDI} = 3.3 V	–	1	–	μA
I_{ENH}	Logic “1” Input Bias Current	V_{INA} = V_{INB} = V_{EN} = V_{DDI} = 20 V	–	1	–	μA
I_{ENL}	Logic “0” Input Bias Current	V_{INA} = V_{INB} = V_{EN} = V_{DDI} = 0 V	–	50	–	μA
DRIVER OUTPUT						
V_{OUTAL1}, V_{OUTBL1} V_{OUTAL2}, V_{OUTBL2}	Output Low State	I_{SINK} = 200 mA, T_A = 25°C I_{SINK} = 200 mA, T_A = –40°C to 125°C	–	0.1	0.22 0.5	V
V_{OUTAH1}, V_{OUTBH1} V_{OUTAH2}, V_{OUTBH2}	Output High State	I_{SRC} = 200 mA, T_A = 25°C I_{SRC} = 200 mA, T_A = –40°C to 125°C	14.7 14.2	14.8	–	V
$I_{PK-SNK1}$	Peak Driver Current, Sink (Note 10)		–	6.5	–	A
$I_{PK-SNK2}$	Peak Miller Plateau Current, Sink (Note 10)	V_{OUTA} = V_{OUTB} = 6 V (near IGBT Miller Plateau)	–	6	–	A
$I_{PK-SRC1}$	Peak Driver Current, Source (Note 10)		–	6.5	–	A
$I_{PK-SRC2}$	Peak Miller Plateau Current, Source (Note 7)	V_{OUTA} = V_{OUTB} = 9 V (near IGBT Miller Plateau)	–	6	–	A
IGBT SHORT CIRCUIT CLAMPING						
$V_{CLAMP-OUTA}$, $V_{CLAMP-OUTB}$	Clamping Voltage ($V_{CLAMP-OUTA}$ – V_{DDA}), ($V_{CLAMP-OUTB}$ – V_{DDB})	I_{OUTA} = I_{OUTB} = 500 mA (pulse test, t_{CLPmax} = 10 μs) (see Figure 30)	–	1	1.3	V

Table 7. ELECTRICAL CHARACTERISTICS (continued) V_{DDI} = 5V, V_{DDA} = V_{DDB} = 15 V
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTIC						
$t_{PD-ON-A}$	OUTA High Propagation Delay	C_{LOAD} = 10 nF, V_{INAH} to 10% of Output Change for PW > 150 ns	40	60	90	ns
$t_{PD-OFF-A}$	OUTA Low Propagation Delay	C_{LOAD} = 10 nF, V_{INAL} to 90% of Output Change for PW > 150 ns	40	60	90	ns
$t_{DISTORT-A}$	Propagation Delay Distortion (Channel A) ($t_{PD-ON-A} - t_{PD-OFF-A}$)	PW >150 ns	−20	0	20	ns
$t_{PD-ON-B}$	OUTB High Propagation Delay	C_{LOAD} = 10 nF, V_{INBH} to 10% of Output Change for PW > 150 ns	40	60	90	ns
$t_{PD-OFF-B}$	OUTB Low Propagation Delay	C_{LOAD} = 10 nF, V_{INBL} to 90% of Output Change for PW > 150 ns	40	60	90	ns
$t_{DISTORT-B}$	Propagation Delay Distortion (Channel B) ($t_{PD-ON-B} - t_{PD-OFF-B}$)	PW >150 ns	−20	0	20	ns
$t_{DISTORT-ON}$	Rising Edge Propagation Delay Distortion ($t_{PD-ON-A} - t_{PD-ON-B}$)	PW >150 ns	−20	0	20	ns
$t_{DISTORT-OFF}$	Falling Edge Propagation Delay Distortion ($t_{PD-OFF-A} - t_{PD-OFF-B}$)	PW >150 ns	−20	0	20	ns
t_{RISE}	Rise Time for Both Channel A and B	C_{LOAD} = 1 nF, 10% to 90% of Output Change	–	12	–	ns
t_{FALL}	Fall Time for Both Channel A and B	C_{LOAD} = 1 nF, 90% to 10% of Output Change	–	10	–	ns
t_{DT}	Deadtime between channels	DT pin Float	–	<20	–	ns
		R_{DT} = 500 kΩ	–	5	–	μs
		R_{DT} = 20 kΩ	–	200	–	ns
t_{DIS}	Disable Delay (NCx57540 only)		–	60	–	ns
t_{EN}	Enable Delay (NCx57530 only)		–	60	–	ns
t_{MIN1}	Input Pulse Width for no output	Positive pulse (L−H−L), T_A = 25°C	–	–	10	ns
		Negative pulse (H−L−H), T_A = 25°C	–	–	10	ns
t_{MIN2}	Input Pulse Width for guaranteed output	Positive pulse (L−H−L), T_A = 25°C	40	–	–	ns
		Negative pulse (H−L−H), T_A = 25°C	40	–	–	ns
t_{UVF}	UVLOI/UVLOA/UVLOB Fall Delay	(Note 10)	–	1.5	–	μs
t_{UVR}	UVLOI/UVLOA/UVLOB Rise Delay	(Note 10)	10	20	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Values based on design and/or characterization.
11. PW = Pulse Width

Modes of Operation

The NCx575y0 can operate in 2 distinct modes:

1. The low−side, high−side half−bridge driver with programmable dead−time.
2. The two independent (potentially overlapping) channels with two inputs.

1st mode – half−bridge driver with two inputs and adjustable dead−time is for applications where you have high−side and low−side PWM available. The driver provides interlock function to prevent activation of high−side and low−side outputs at the same time. In addition the driver generates dead−time which is adjustable by DT pin.

The typical application schematics are on Figure 2 and Figure 3.

- The dead−time is set by resistor R_{DT} connected between DT pin and GNDI. Adjusting dead−time is described in the section Dead−time (DT).

2nd mode – driver with two independent channels and two inputs is different from previous mode because it allows for completely independent and even overlapping PWMs to drive the outputs individually.

- DT pin has to be connected to V_{DDI}. This disables the interlock function and dead−time generator and allows the overlapping PWMs. So the channel A and B can be driven completely independently.

Dead−Time (DT)

The dead−time pin is controlling the integrated interlock and dead−time generator.

- If DT pin is connected to V_{DDI} the interlock and dead−time generator are disabled. The channels A and B are completely independent.
- If DT pin is floating the interlock is enabled but dead−time generator is disabled. There is a minimal dead−time shorter than 20 ns.
- If there is a resistor R_{DT} connected between the DT pin and GNDI the interlock and dead−time generator are both enabled. The dead−time can be adjusted in range from 200 ns ($R_{DT} \approx 20$ kΩ) to 5 µs ($R_{DT} \approx 500$ kΩ). Dead−time can be estimated by the equation t_{DT} (ns) ≈ 10 x R_{DT} (kΩ). With high R_{DT} values the potential noise pick−up on high impedance of R_{DT} should be considered. R_{DT} should be as close to driver pins as possible and the loop should be minimized.
- If R_{DT} is below 20 kΩ the DT is not closely following the equation but dead−times lower than 200 ns could be achieved. The lowest allowed value of R_{DT} = 5 kΩ which reduces the dead−time to about 70 ns.

The Figures 2 and 3 illustrate the behavior of the NCx575y0 in 1st mode (high−side, low−side half−bridge driver with two inputs). The outputs for various input PWM combinations are shown in Figure 4.

The dead−time is a time from low−side output going low to high−side output going high or from high−side output going low to low side output going high. The overlap is a situation where both signals are high at the same time. Overlap causes cross conduction in the half−bridge and must be avoided.

In the “Non−overlap and Dead−time are met” column in Fig. 4, the channel A PWM, INA (high−side), and channel B PWM, INB (low−side), are not overlapping and have sufficient dead−time. Therefore, the driver does not apply corrections to the signals and passes them as they are to their respective output.

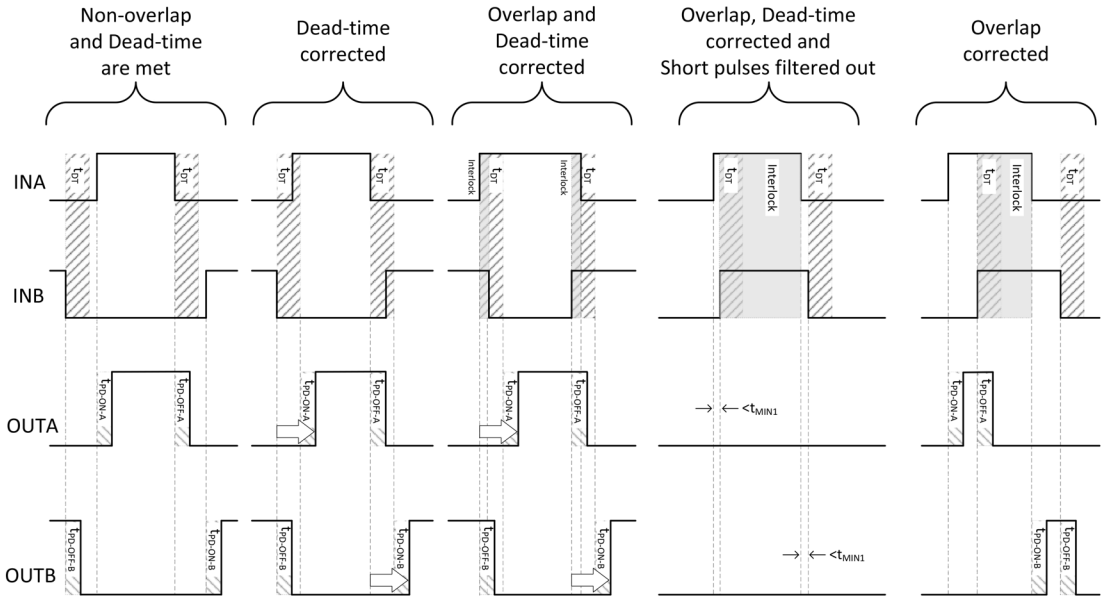


Figure 4. Deadtime, Interlock and Output Minimum Pulse Width

In the “Dead−time corrected” column, the high−side and low−side signals are not overlapping but the dead−time value is less than the value set through the DT pin. Consequently, the driver increases the dead−time value to the value set by the DT pin.

In the “Overlap and Dead−time corrected” column, the high−side and low−side input signals are high at the same time (overlapping). This condition could cause cross−conduction in the half−bridge. Therefore, the driver’s interlock function trims signal OUTB which is going low when INA goes high, and not when INB goes low. The driver also inserts the dead−time set through DT pin, thus the output pulses are not overlapping and cross−conduction in the half−bridge is avoided.

In the “Overlap, Dead−time corrected and Short pulses filtered out” column, the high−side and low side signals are overlapping and could cause cross−conduction in the half−bridge. Therefore, the driver’s interlock function trims the output signals and a short spike remains on each output signal. If the spike is shorter than tMIN1 (Minimum pulse width filtering time), it will be suppressed and no output is generated.

In the “Overlap corrected” column the dead−time is met but the signals are overlapping so just the non−overlapping parts pass to the output.

Inputs INA, INB, DIS, EN

Unused inputs INA, INB, DIS should be tied to GNDI. Unused EN should be tied to V_{DDI}.

Disable (DIS) Pin (NCx57540)

DIS (disable) pin allows to deactivate both outputs independently of inputs INA, INB, DT.

If the pin is set high both OUTA and OUTB are set low immediately.

If DIS is set low, the outputs OUTA/OUTB are restored after rising edge is detected on the INA/INB respectively.

It has an internal pull−down resistor of 125 kΩ to ensure that OUTA and OUTB react to INA, INB and DT in the absence of an external signal. External pull−down resistor 10−47 kΩ is recommended to prevent unwanted DIS activation by external interference. Direct connection to GNDI is recommended if the pin is not used.

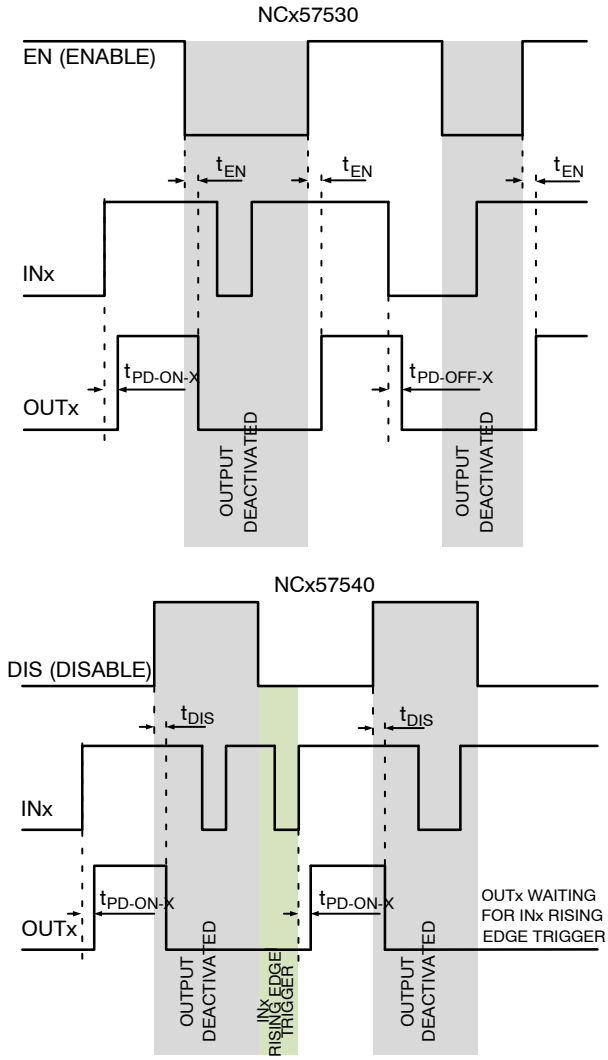


Figure 5. Disable Function

Enable (EN) Pin (NCx57530)

EN (Enable) is a useful feature as it allows to deactivate both outputs independently of inputs INA, INB, DT. If EN is set to high both OUTA and OUTB work depending on INA and INB. If EN is set to low, the outputs OUTA/OUTB are set to low immediately, then if EN is set to high, OUTA/OUTB follows INA/INB immediately (see Figure 5). It has an internal pull−up resistor of 125 kΩ to ensure that OUTA and OUTB react to INA, INB and DT in the absence of an external signal. External pull−up resistor 10−47 kΩ is recommended to prevent unwanted EN activation by external interference. Direct connection to VDDI is recommended if the pin is not used.

Input Voltage Levels

The NCx575y0 has a two modes for high and low levels on all input pins:

1. For V_{DDI} from 3.3 to 5 V the high and low input levels are scaling with the V_{DDI} as stated in the Electrical characteristics table. Low input level is $0.3 \times V_{DDI}$, high input level is $0.7 \times V_{DDI}$.
2. For V_{DDI} above 5 V the high and low input levels clamp at the same value as for V_{DDI} = 5 V. That means the low input level is $0.3 \times 5 = 1.5$ V and the high input level is $0.7 \times 5 = 3.5$ V.

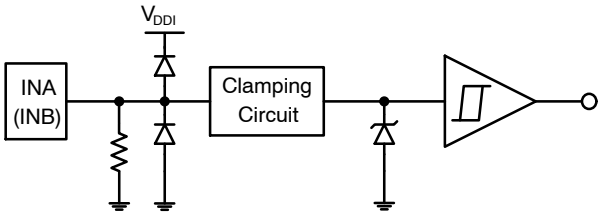


Figure 6. Input Pin Structure

Edge Triggered Inputs

The INA, INB and DIS inputs are activated by a signal edge (edge triggered), not with signal level. This means that after power cycling the driver, a rising edge has to occur on INA, INB for OUTA and OUTB to go high, respectively. The same conditions apply if the output signals are disabled through the DIS pin. Therefore, after DIS signal goes low, a rising edge has to occur on INA, INB for OUTA and OUTB to go high, respectively.

Under Voltage Lockout UVLOI, UVLOA, UVLOB

NCx575y0 UVLOA and UVLOB ensures reliable switching of the IGBT connected to the driver output. Driving the IGBT with low gate voltage causes it to switch outside the saturation region (in the linear region) which significantly increases the power losses and there is a danger of damage.

UVLOI ensures correct transmission of the signals from the primary side to the secondary side of the driver.

NCx575y0 is equipped by edge triggered inputs in order to prevent output pulse trimming. Therefore, after returning from safe state to active state, a rising edge has to occur on

INA, INB in order to set OUTA and OUTB high, respectively (see Figures 7, 8 and Figures 9, 10).

As a side effect of this feature is that the t_{UVR} time is always prolonged by a $t_{UVR-spread}$. The $t_{UVR-spread}$ is the delay caused by the time before next rising edge of PWM signal comes.

Another note for the t_{UVR} is that it is valid if the V_{DD2} rises from just below $V_{UVLO-OUT-OFF}$ to $V_{UVLO-OUT-ON}$. The cold−start time from $V_{DDA(B)}$ = 0 V to PWM at the output is t_{UVR} + startup time of the internal bias circuits. The whole time is about 20 μs and the internal bias circuit startup time is about 10 μs.

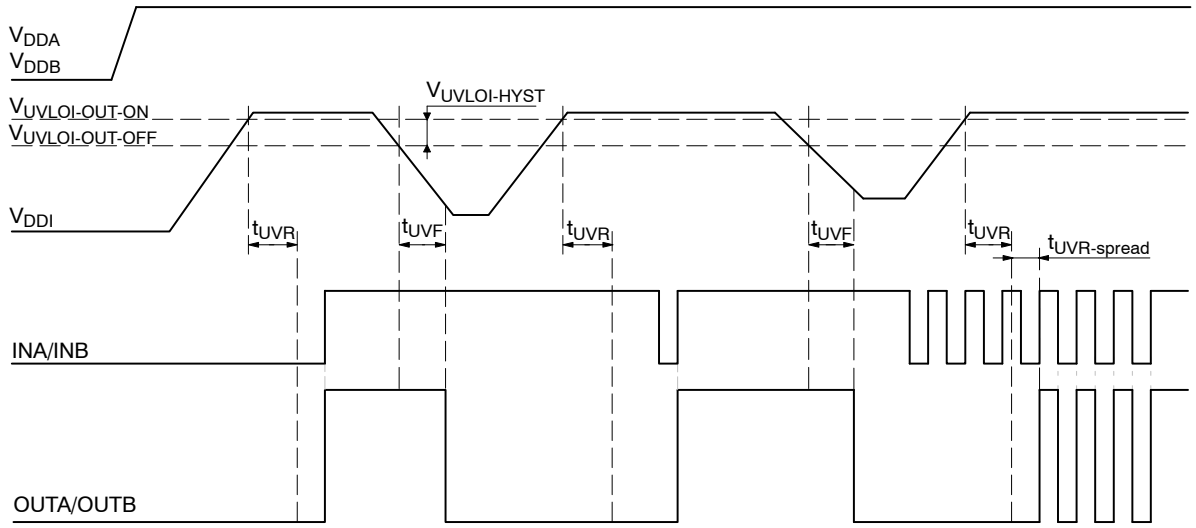


Figure 7. Output Ramp−up and Ramp−down Times during UVLOI

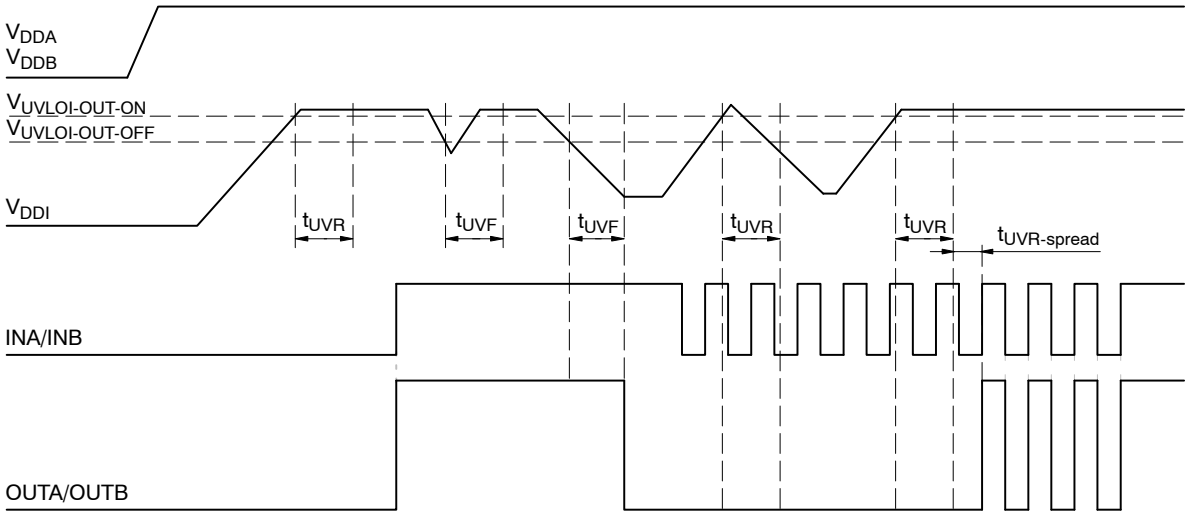


Figure 8. V_{DDI} Glitch Filtering

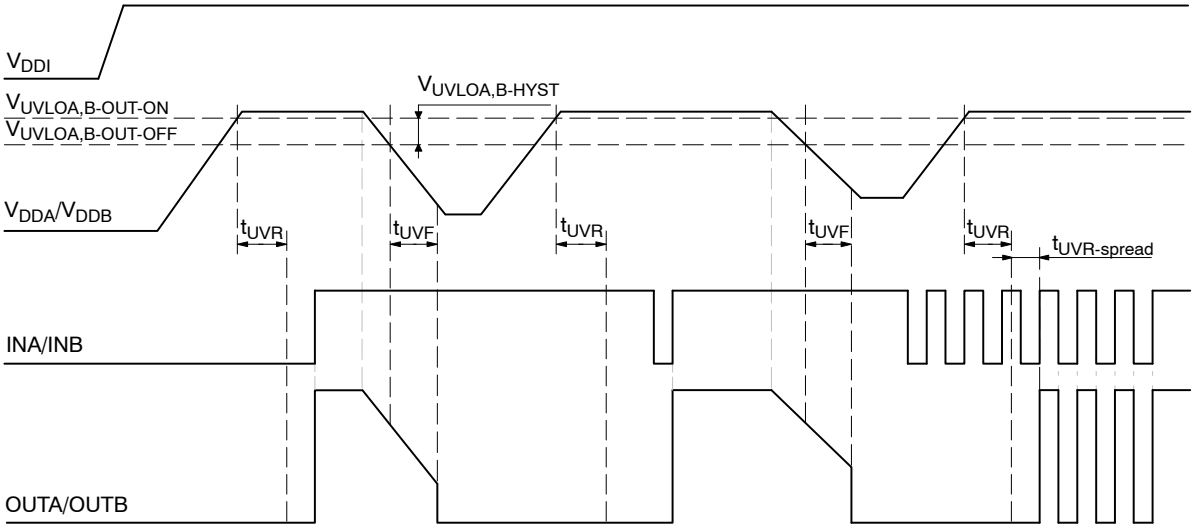


Figure 9. Output Ramp−up and Ramp−down Times during UVLOA, UVLOB

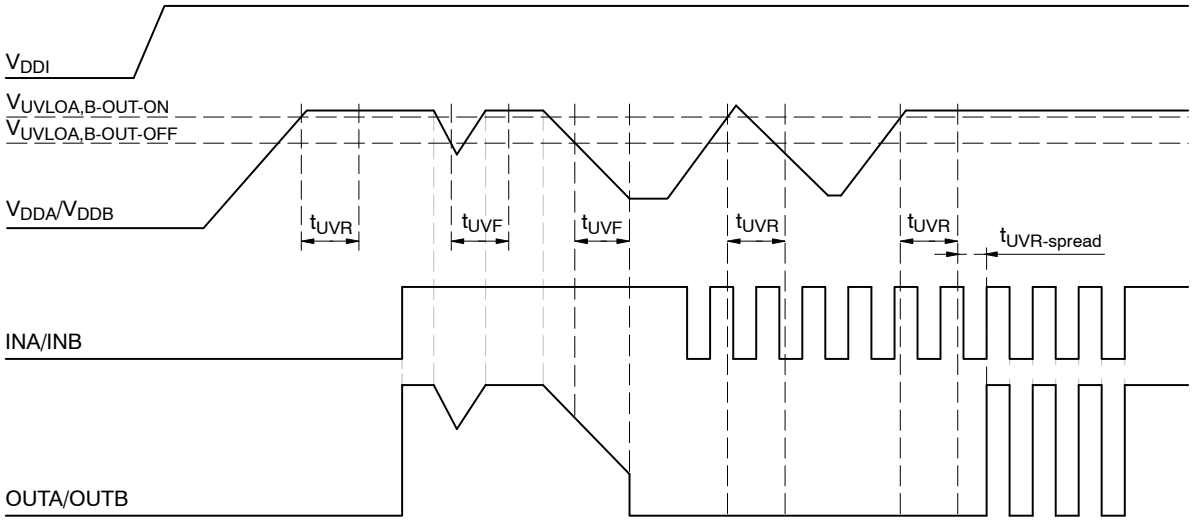


Figure 10. V_{DDA}/V_{DDB} Glitch Filtering

Power Supply

Decoupling (VDDI, VDDA, VDDB)

Suitable external power capacitors are required for reliable driving of IGBT gate with high current. Parallel combination of 100 nF + 4,7 μF low ESR ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving of IGBT modules (containing several parallel IGBT's) with a gate capacitance over 10 nF a higher decoupling capacity is required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver's power pins. The recommended layout is provided in the Figure 12.

Cooling Polygons on GNDA/GNDB

It is important to provide cooling polygons if driving IGBTs with higher gate capacitance values and using higher switching frequencies. They have to be connected to GNDA and GNDB (See Figure 12).

Output Current on GNDA/GNDB

The NCx575y0 has a high current, low−drop MOSFET output stage. It is capable of driving IGBTs with gate capacitance C_G of up to 100 nF. For optimal IGBT driving a few conditions have to be met:

- Low inductance (wide and short) traces from OUTA (OUTB) to R_G and to IGBT gate and from emitter (source) to GNDA (GNDB).
- Sufficient power rating of gate resistors R_G.
- Reasonable combination of switching frequency f and gate capacitance C_G of the IGBT.
- Good V_{DDA} and V_{DDB} decoupling (discussed above).
- Sufficient cooling pads (discussed above).

Low Inductance Traces

All the traces have to be as low inductance as possible due to the high current path from the driver output to IGBT gate. In practice that means wide tracks which are as short as possible. Tracks also have to be routed in order to not create big loops. The driving path (driver output, RG, IGBT gate) and return path (IGBT emitter, GNDA or GNDB pin) have to be routed as a pair and not enclosing other components.

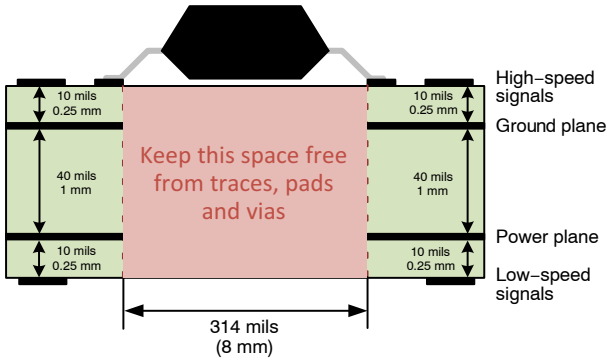


Figure 11. SOIC−16WB Recommended Layer Stack

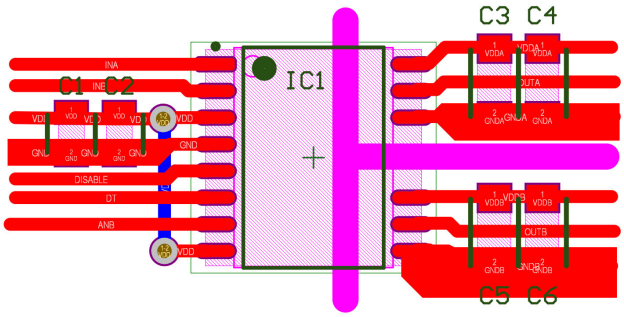
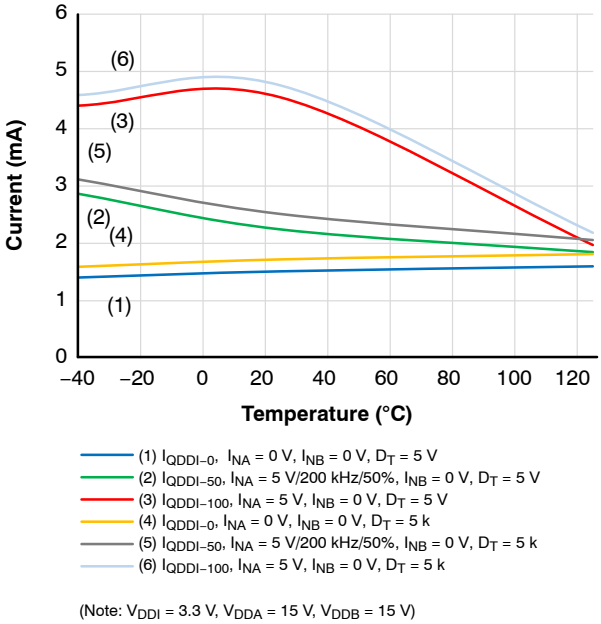


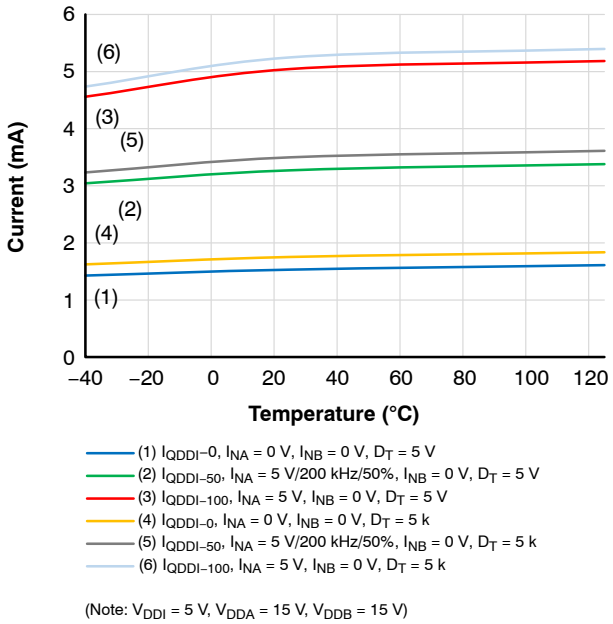
Figure 12. SOIC−16 Recommended Layer Stack (CASE 752AJ)

TYPICAL CHARACTERISTICS



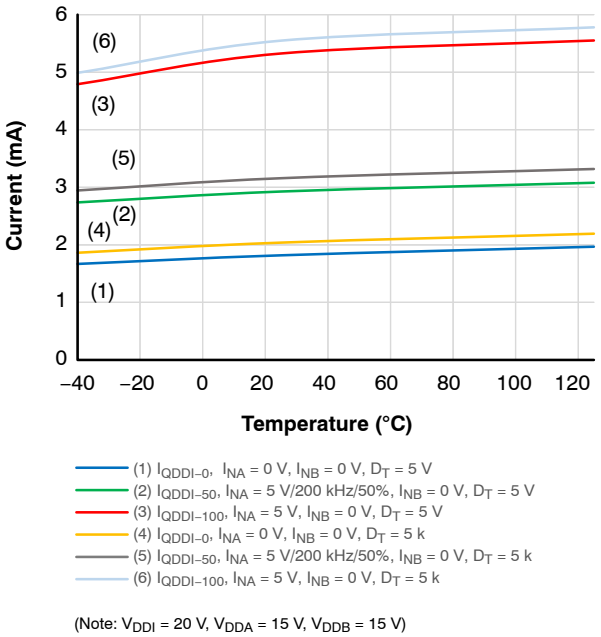
(Note: V_{DDI} = 3.3 V, V_{DDA} = 15 V, V_{DDB} = 15 V)

Figure 13. I_{QDDI} Supply Current, V_{DDI} = 3.3 V



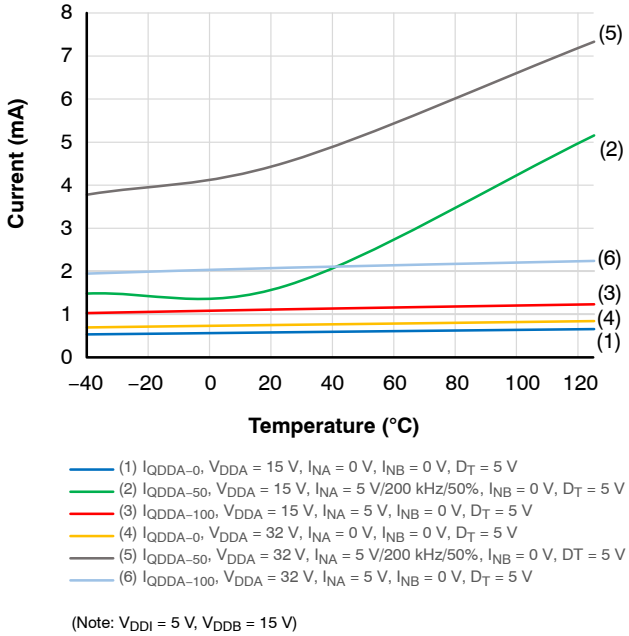
(Note: V_{DDI} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V)

Figure 14. I_{QDDI} Supply Current, V_{DDI} = 5 V



(Note: V_{DDI} = 20 V, V_{DDA} = 15 V, V_{DDB} = 15 V)

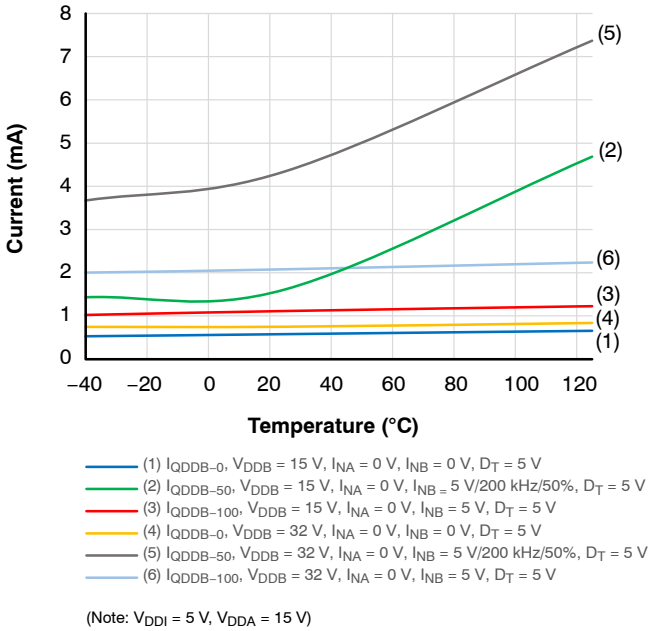
Figure 15. I_{QDDI} Supply Current, V_{DDI} = 20 V



(Note: V_{DDI} = 5 V, V_{DDB} = 15 V)

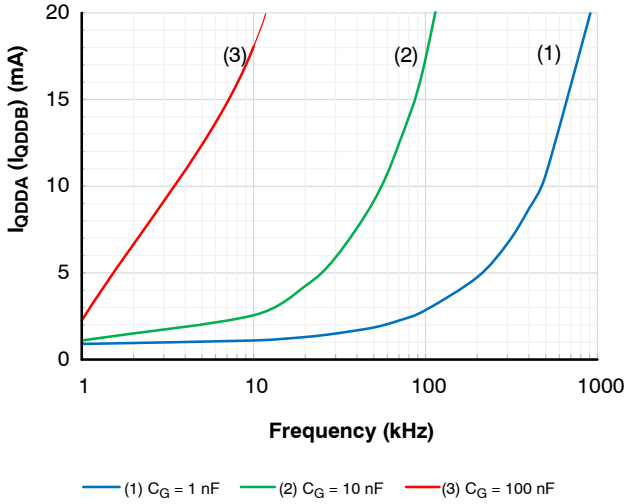
Figure 16. I_{QDDA} Supply Current

TYPICAL CHARACTERISTICS



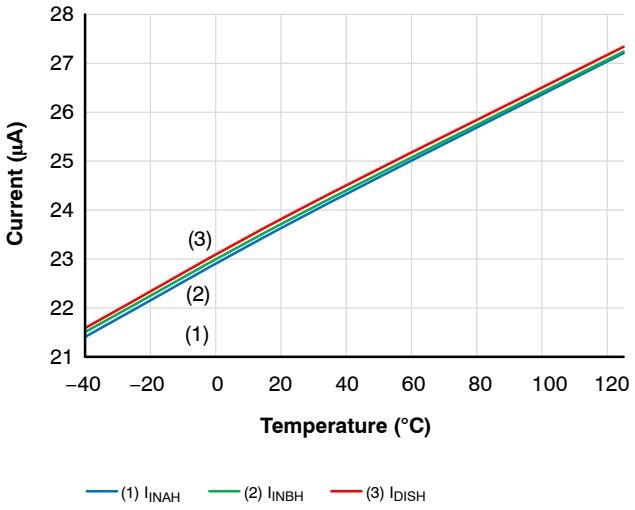
(Note: V_{DDI} = 5 V, V_{DDA} = 15 V)

Figure 17. I_{QDDB} Supply Current



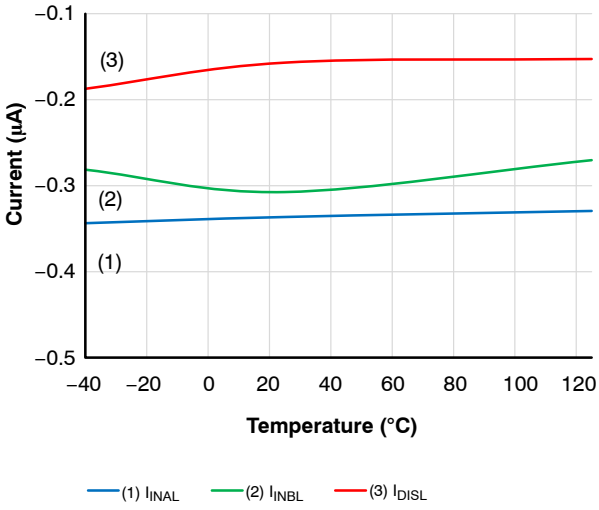
(Note: V_{DDI} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V, I_{NA} = 5 V/50%, I_{NB} = 0 V, D_T = V_{DDI}, DIS = GNDI, R_G = 0 Ω)

Figure 18. I_{QDDA} (I_{QDDB}) Supply Current vs. Switching Frequency



(Note: V_{DDI} = V_{INA} = V_{INB} = V_{DIS} = 3.3 V, V_{DDA} = V_{DDB} = 15 V)

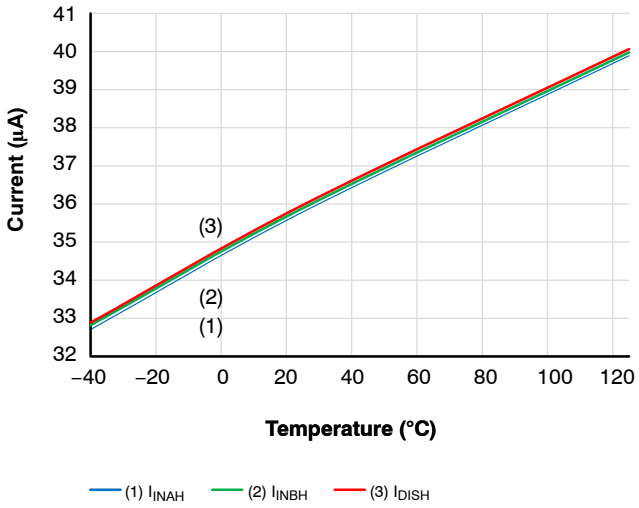
Figure 19. Input Bias Current – Logic “1”



(Note: V_{DDI} = 3.3 V, V_{INA} = V_{INB} = V_{DIS} = GNDI, V_{DDA} = V_{DDB} = 15 V)

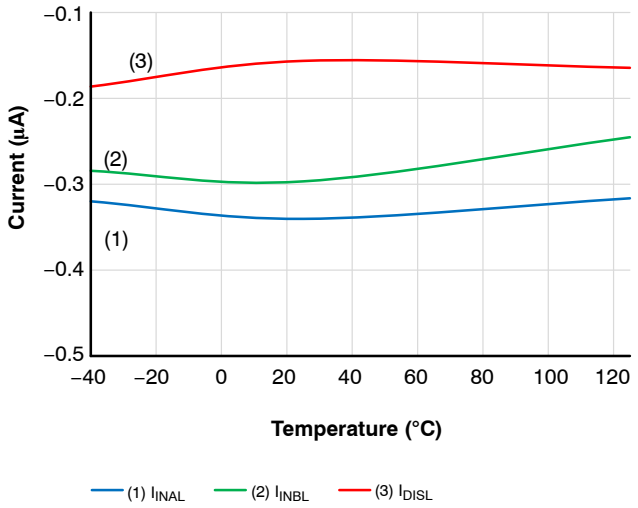
Figure 20. Input Bias Current – Logic “0”

TYPICAL CHARACTERISTICS



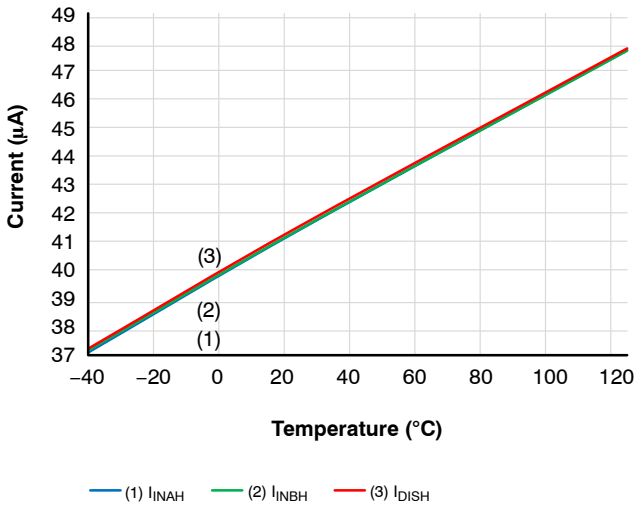
(Note: V_{DDI} = V_{INA} = V_{INB} = V_{DIS} = 5 V, V_{DDA} = V_{DDB} = 15 V)

Figure 21. Input Bias Current – Logic “1”



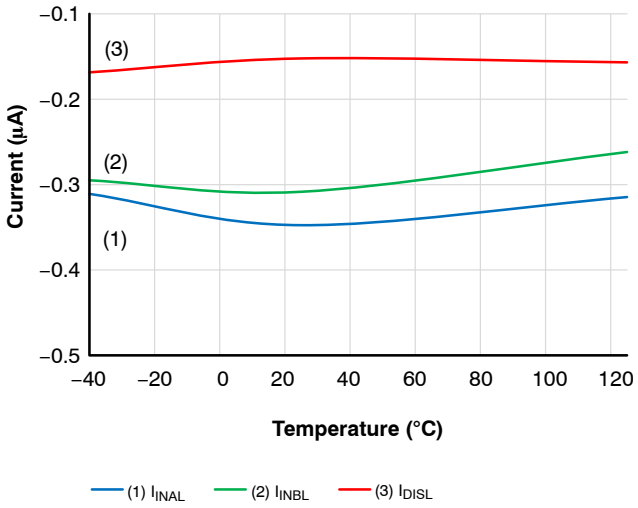
(Note: V_{DDI} = 5 V, V_{INA} = V_{INB} = V_{DIS} = GNDI, V_{DDA} = V_{DDB} = 15 V)

Figure 22. Input Bias Current – Logic “0”



(Note: V_{DDI} = V_{INA} = V_{INB} = V_{DIS} = 20 V, V_{DDA} = V_{DDB} = 15 V)

Figure 23. Input Bias Current – Logic “1”



(Note: V_{DDI} = 20 V, V_{INA} = V_{INB} = V_{DIS} = GNDI, V_{DDA} = V_{DDB} = 15 V)

Figure 24. Input Bias Current – Logic “0”

TYPICAL CHARACTERISTICS

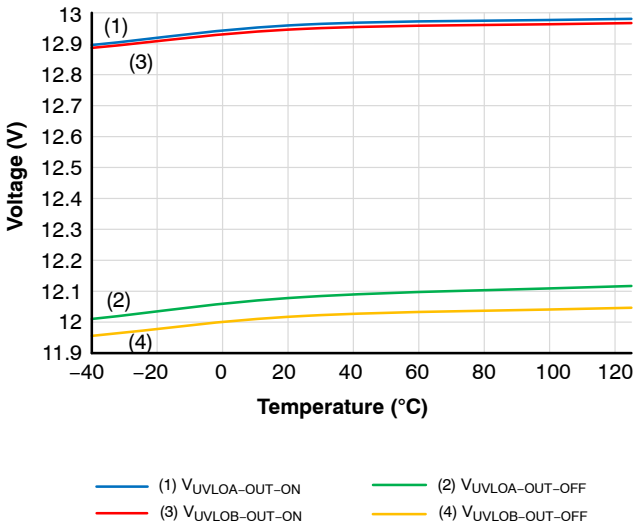


Figure 25. NCx57540 UVLOA and UVLOB Threshold Voltage

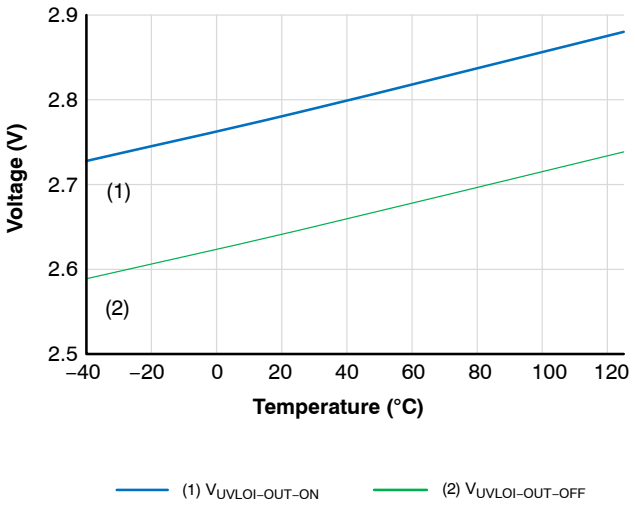


Figure 26. UVLOI Threshold Voltage

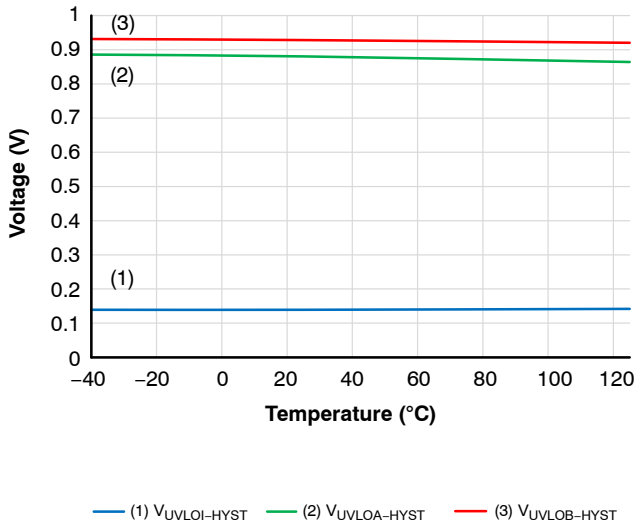


Figure 27. UVLOx Enable/Disable Voltage Hysteresis

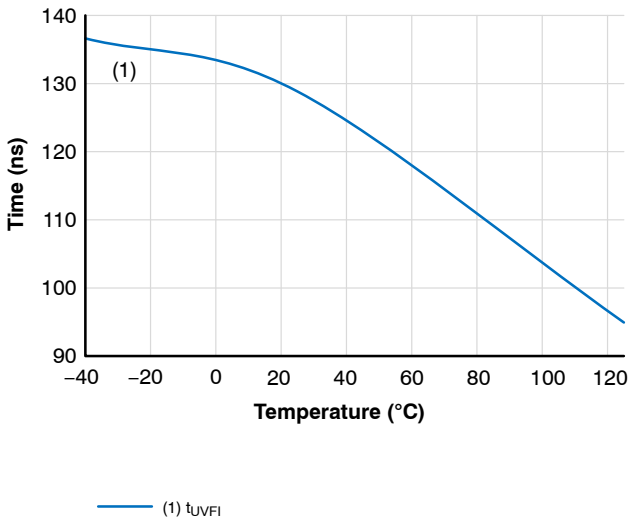


Figure 28. UVLOI Fall Delay

TYPICAL CHARACTERISTICS

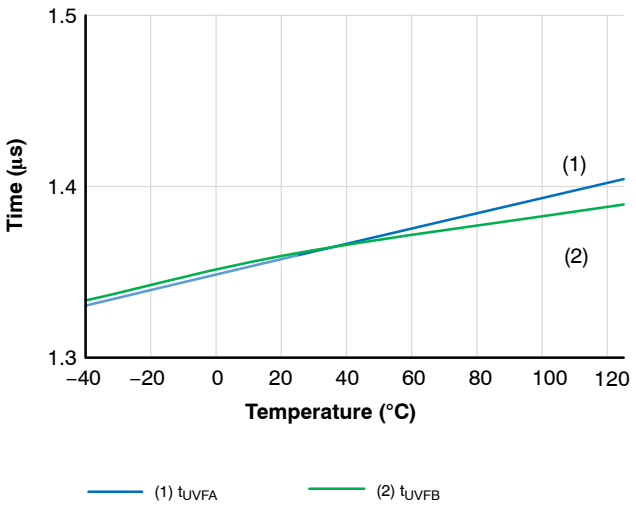


Figure 29. UVLOA and UVLOB Fall Delay

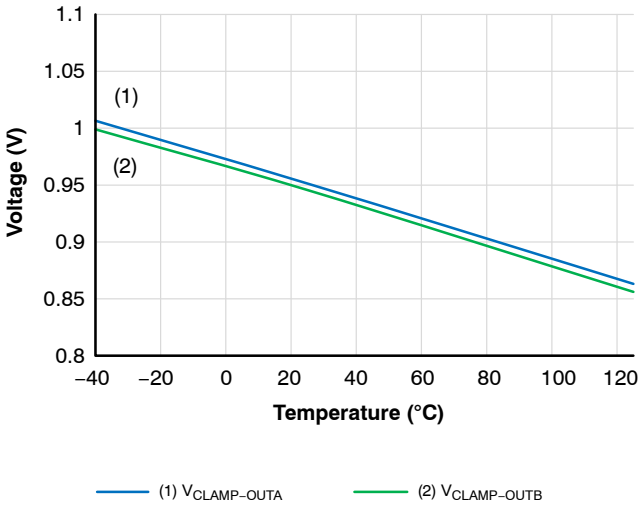


Figure 30. IGBT Short Circuit Clamping Voltage

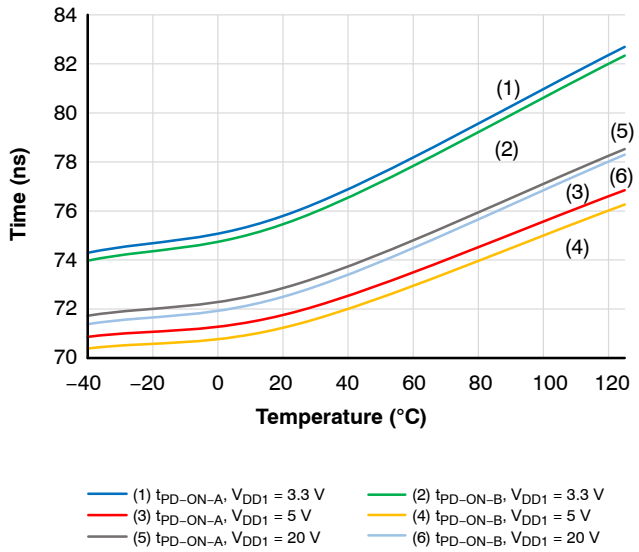


Figure 31. Propagation Delay Turn−on

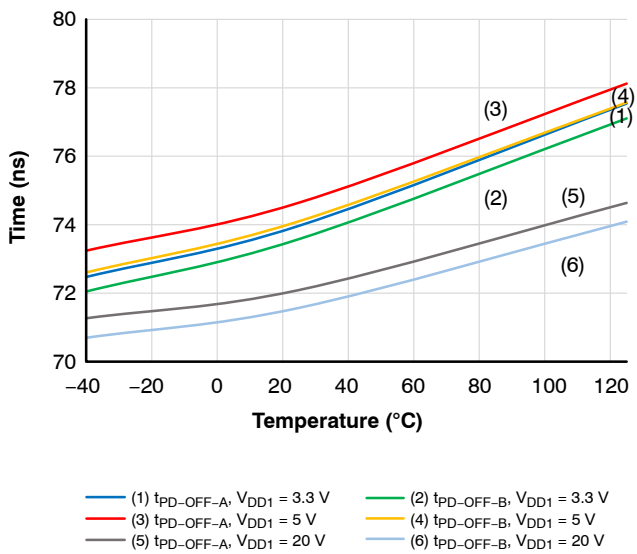


Figure 32. Propagation Delay Turn−off

TYPICAL CHARACTERISTICS

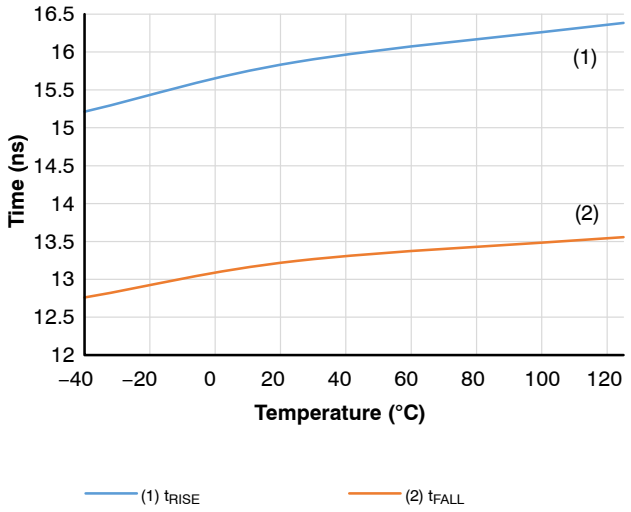


Figure 33. Rise Time / Fall Time

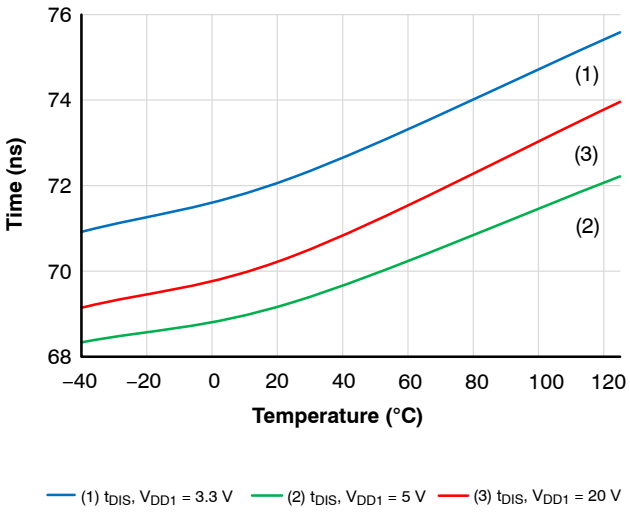
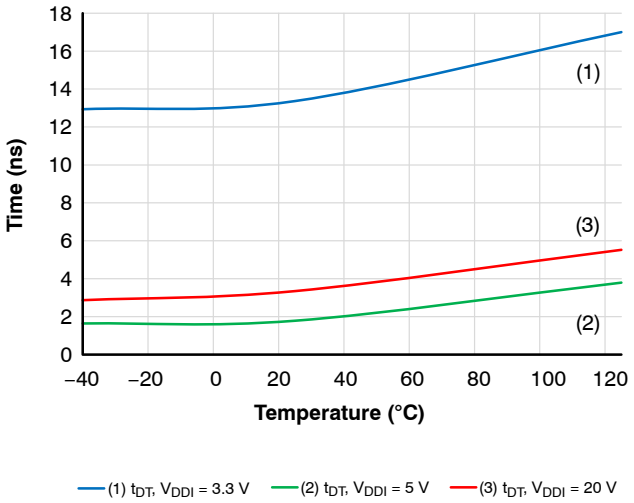
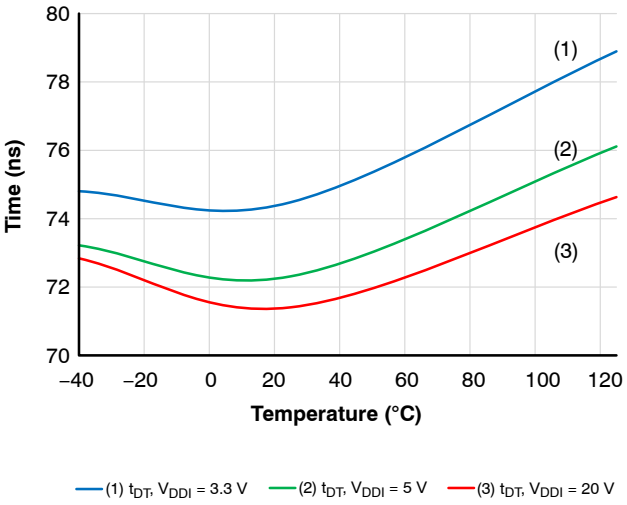


Figure 34. Disable Delay Time



(Note: V_{INA} is inverted from V_{INB}, V_{DDA} = V_{DDB} = 15 V)

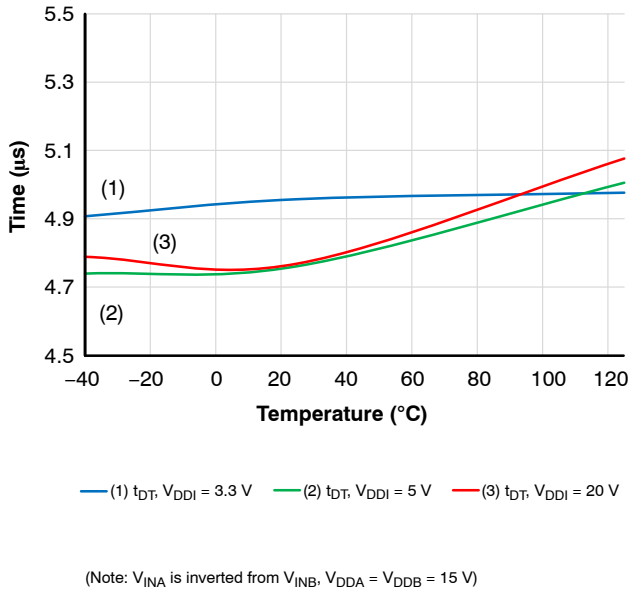
Figure 35. Deadtime, DT pin FLOAT



(Note: V_{INA} is inverted from V_{INB}, V_{DDA} = V_{DDB} = 15 V)

Figure 36. Deadtime, DT pin 5 kΩ to GNDI

TYPICAL CHARACTERISTICS



(Note: V_{INA} is inverted from V_{INB}, V_{DDA} = V_{DDB} = 15 V)

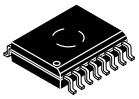
Figure 37. Deadtime, DT pin 500 kΩ to GNDI

ORDERING INFORMATION

Device	Qualification	Package	Case	Shipping†
NCD57530DWKR2G	Industrial	SOIC−16 Wide Body (less pin 12 & 13) (Pb−Free)	752AJ	1,000 / Tape & Reel
NCD57540DWKR2G				
NCV57530DWKR2G*	Automotive (AEC−Q100 Qualified and PPAP Capable)			
NCV57540DWKR2G*				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



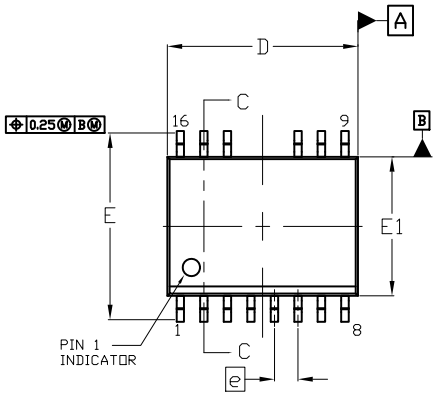
1

SCALE 1:1

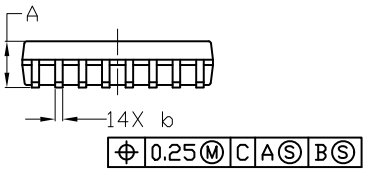
SOIC−16 WB LESS PINS 12 & 13

CASE 752AJ
ISSUE O

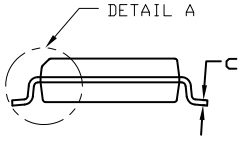
DATE 17 FEB 2021



TOP VIEW



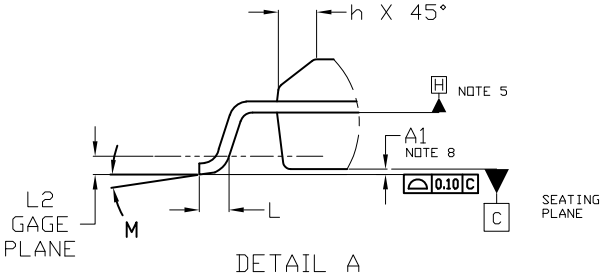
SIDE VIEW



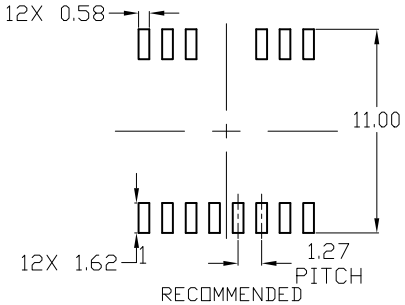
SECTION C−C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	2.35	2.50	2.65
A1	0.10	0.18	0.25
b	0.35	0.42	0.49
c		0.25 REF	
D	10.15	10.30	10.45
E	10.05	10.30	10.55
E1	7.40	7.50	7.60
e		1.27 BSC	
h	0.25	---	0.75
L	0.50	---	0.90
L2		0.25 REF	
M	0°	---	7°



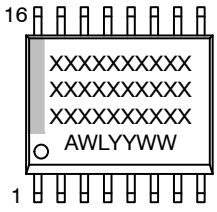
DETAIL A



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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