Dual Smart Card Interface IC with SPI Programming Interface

NCN6804

The NCN6804 is a dual interface IC with serial control. It is dedicated for Smart Card/Secure Access Module (SAM) reader/writer applications. It allows the management of two external ISO/EMV cards (Class A, B or C). An SPI bus is used to control and configure the dual interface. The cards are controlled in a multiplexed mode. Two NCN6804 devices (4 smart card interfaces) can share one single control bus thanks to a dedicated hardware address pin (S1).

An accurate protection system guarantees timely and controlled shutdown in the case of external error conditions.

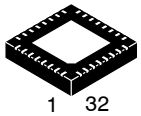
This device is an enhanced version of the NCN6004A, more compact, more flexible and fully compatible with the NCN6001, its single interface counterpart version. It is fully compatible with ISO 7816−3, EMV and GIE−CB standards.

Features

- Dual Smart Card / SAM Interface with SPI Programming Bus
- Fully Compatible with ISO 7816−3, EMV and GIE−CB Standards
- One Protected Bidirectional Buffered I/O Line per Card Port
- Wide Power Supply Voltage Range: 2.7V < $V_{DDPA/B}$ & V_{DD} < 5.5 V
- Programmable/Independent CRD_VCC Supply for Each Smart Card
- Multiplexed Mode of Operating
- Handles 1.8 V, 3.0 V and 5.0 V Smart Cards
- Programmable Rise & Fall Card Clock Slopes (Slow & Fast Modes)
- Support up to 40 MHz Clock with Internal Programmable Clock (division ratio 1/1, 1/2, 1/4) Managed Independently for Each Card
- Built−in Programmable CRD_CLK Stop Function handles Low State
- ESD Protection on Card pins (8 kV, Human Body Model)
- Activation / Deactivation built−in Sequencer
- Internal I/O Pull−up Resistor with Resistor Disconnection Option (EN_RPU)
- 4−Wire Series Bus Interface – SPI
- QFN32 (5x5 mm^2) Package
- This is a Pb−Free Device

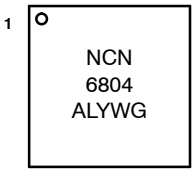
Typical Application

- Point Of Sales (POS) and Transaction Terminals
- ATM (Automatic Teller Machine) / Banking Terminal Interfaces
- Set Top Box Decoder and Pay TV



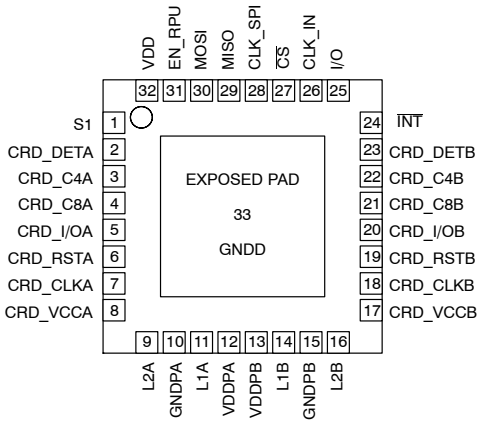
QFN32
CASE 488AM

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCN6804MNR2G	QFN32 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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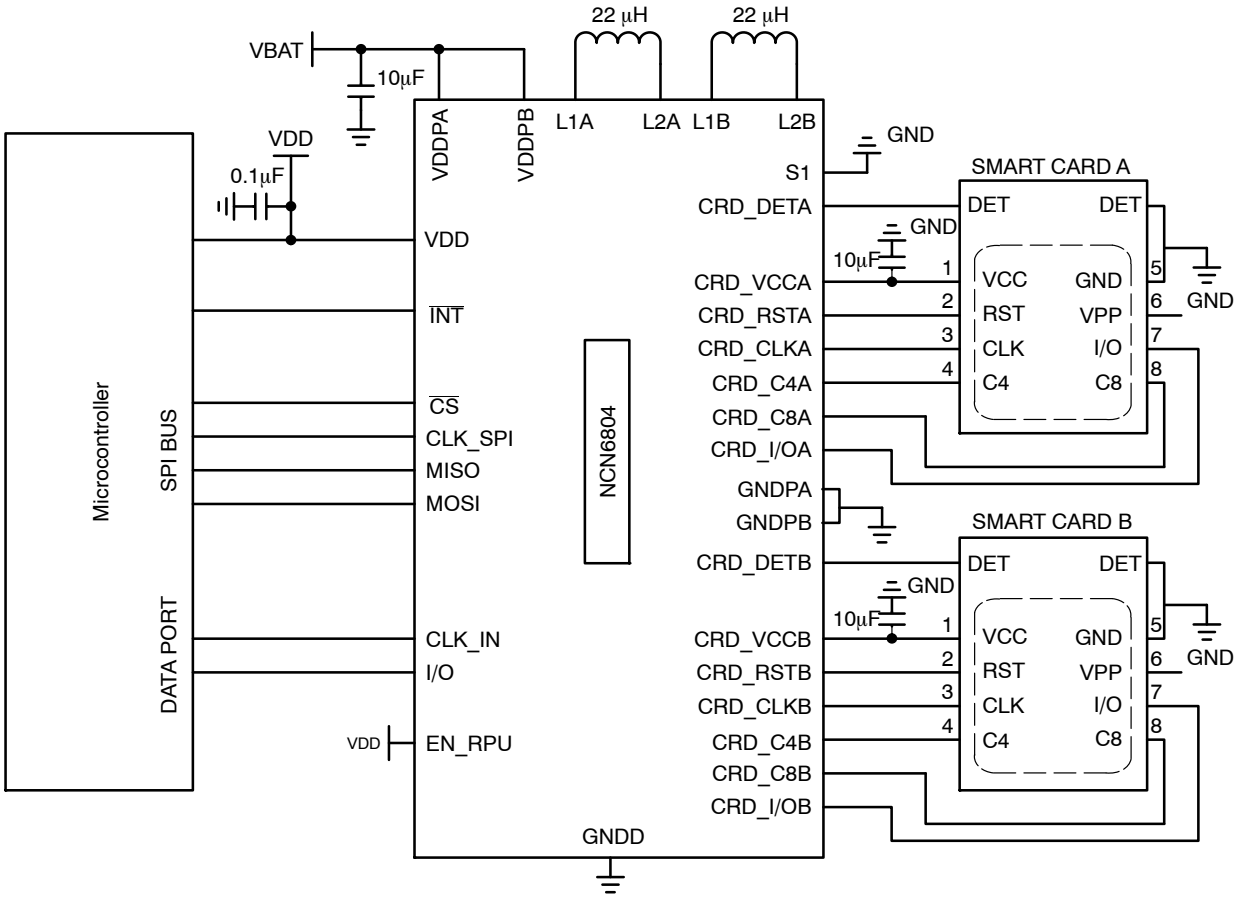


Figure 1. Typical Interface Application

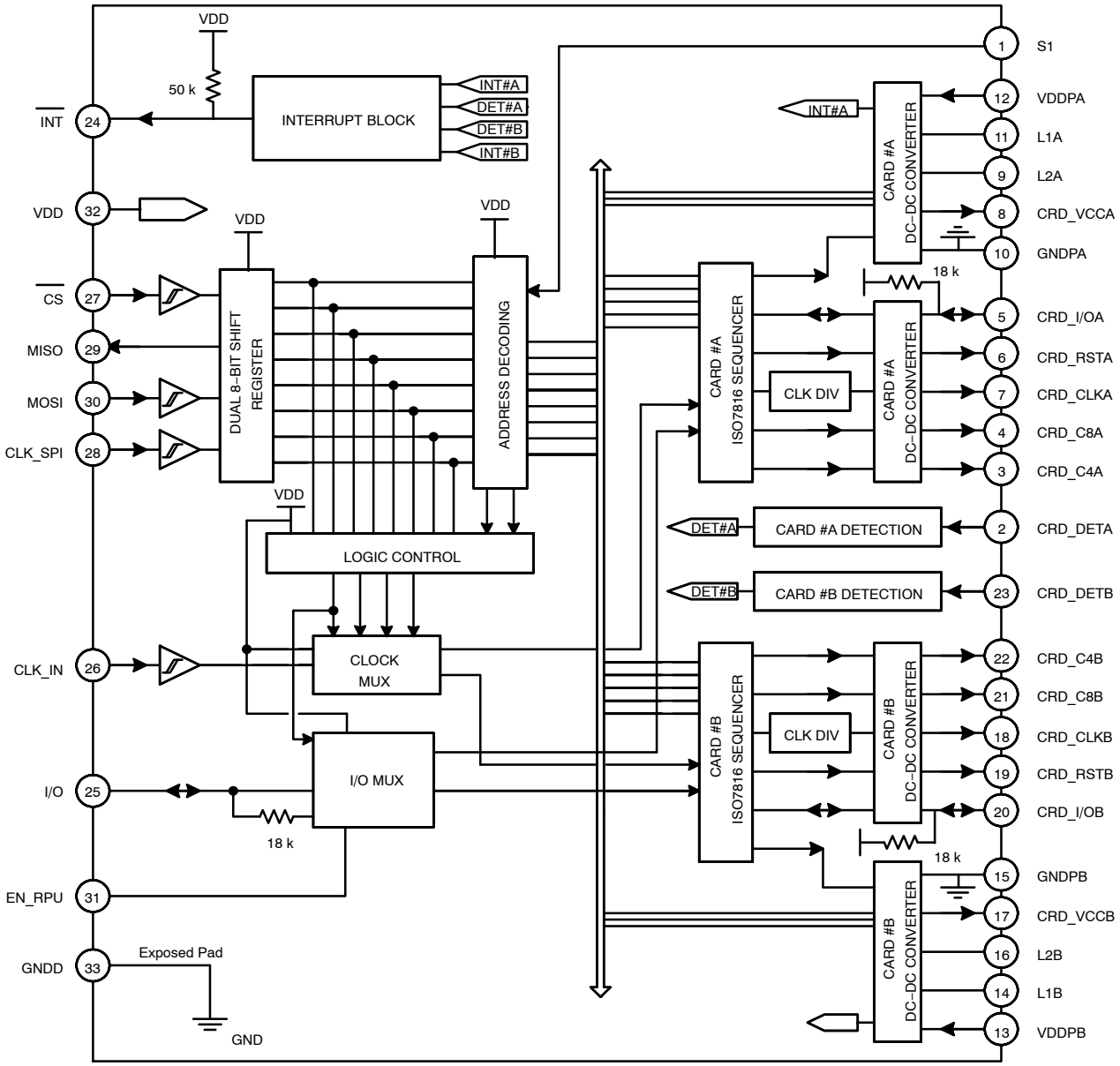


Figure 2. NCN6804 Block Diagram

PIN FUNCTION AND DESCRIPTION

PIN	Name	Type	Description
1	S1	I	Address pin (Chip Identification pin) − allows having in parallel up to 2 NCN6804 devices (4 interfaces) managed by 1 Chip Select pin only ($\overline{CS}$) − multiple interface application case. When one dual interface only is used this pin can be connected to GROUND.
2, 23	CRD_DETA, CRD_DETB	I	The signal coming from the external card connector is used to detect the presence of the card. A built−in pull−up low current source biases this pin HIGH, making it active LOW, assuming one side of the external switch is connected to ground. A built−in digital filter protects the system against voltage spikes present on this pin. The polarity of the signal is programmable by the MOSI message; refer to Table 2. On the other hand, the meaning of the feedback message contained in the MISO register bit b4, depends upon the SPI mode of operation as defined here below: SPI Normal Mode: The MISO bit b4 is HIGH when a card is inserted, whatever be the polarity of the card detect switch. SPI Special Mode: The MISO bit b4 copies the logic state of the card detect switch as depicted here below, whatever be the polarity of the switch used to handle the detection: CRD_DET = LOW => MISO/b4 = LOW CRD_DET = HIGH => MISO/b4 = HIGH In both cases, the chip must be programmed to control the right logic state (Table 2). Since the bias current supplied by the chip is very low, typically 5.0 μA, care must be observed to avoid low impedance or cross coupling when this pin is in the Open state.
3, 22	CRD_C4A, CRD_C4B	O	Auxiliary mixed analog/digital line to handle synchronous card connected when used to the card pin C4. An accelerator circuit makes sure the output positive going rise time is fully within the ISO/EMV specifications.
4, 21	CRD_C8A, CRD_C8B	O	Auxiliary mixed analog/digital line to handle synchronous card connected when used to the card pin C8. An accelerator circuit makes sure the output positive going rise time is fully within the ISO/EMV specifications.
5, 20	CRD_IOA, CRD_IOB	I/O	This pin handles the connection to the serial I/O pin of the card connector. A bi−directional level translator adapts the serial I/O signal between the card and the μC. An internal active pull down device forces this pin to GROUND during either the CRD_VCC start up sequence, or when CRD_VCC = 0V. The output current is internally limited to 15mA. When operating in a synchronous mode I/O is transmitted through the SPI bus (MOSI bit b2) to CRD_I/O. In that case I/O is disconnected and no longer used.
6, 19	CRD_RSTA, CRD_RSTB	O	This pin is connected to the RESET pin of the card connector. A level translator adapts the RESET signal from the μC (through the SPI bus) to the external card. The output current is internally limited to 15mA. The CRD_RST is validated when $\overline{CS}$ = LOW, and is hard wired to GROUND by and internal active pull down circuit when the card is deactivated.
7, 18	CRD_CLKA, CRD_CLKB	O	Clock pin connected to the card pin C3. An internal active pull down device forces this pin to GROUND during the CRD_VCC start up sequence, or when CRD_VCC = 0V. The rise and fall slopes, either FAST or SLOW, of this signal can be programmed by the SPI bus. Refer to Table 2.
8, 17	CRD_VCCA, CRD_VCCB	Power	Power supply to the external card (card pin C1). An external capacitor C_{out} = 10 μF minimum is required. In the event of a CRD_VCC under−voltage issue, the NCN6804 detects the situation and feedback the information in the STATUS bit (MISO bit b0). The device does not take any further action; particularly the DC/DC converter is neither stopped nor re−programmed by the NCN6804. It is up to the external μC to handle the situation. However, when CRD_VCC is overloaded, the NCN6804 shuts off the DC/DC converter, runs a Power Down ISO7816 sequence and reports the fault in the STATUS register (MISO register bit b0).
9	L2A	Power	The high side of the external inductor A.
10	GNDPA	Power	DC/DC converter A power ground pin.
11	L1A	Power	The low side of the external inductor A.
12	VDDPA	Power	DC/DC converter A power supply input (C_{bypass_min} = 4.7 μF).
13	VDDPB	Power	DC/DC converter B power supply input (C_{bypass_min} = 4.7 μF).
14	L1B	Power	The low side of the external inductor B.
15	GNDPB	Power	DC/DC converter B power ground pin.
16	L2B	Power	The high side of the external inductor B.
24	$\overline{INT}$	O	This pin is activated LOW when a card has been inserted and detected by the CRD_DETA or CRD_DETB pins in either of the external ports. Similarly an interrupt is generated when the CRD_VCCA or B output is overloaded, or when the card has been extracted whatever be the transaction status (running or stand by). The $\overline{INT}$ signal is reset to HIGH according to Table 7. On the other hand, the pin is forced to logic HIGH when the power supply voltage VDDPA or B drops below 2 V.

PIN FUNCTION AND DESCRIPTION

PIN	Name	Type	Description
25	I/O	I/O	This pin is connected to an external micro−controller (μC) interface. A bi−directional level translator adapts the serial I/O signal between the smart card and the μC. The level translator is enabled when $\overline{CS}$ = LOW, the sub address has been selected and the system operates in the Asynchronous mode. When a Synchronous card is in use this pin is disconnected and the data and transaction take place through the MOSI and the MISO registers. The internal pull up resistor connected on the μC side is activated and visible by the selected chip only.
26	CLK_IN	I	This pin (high impedance) can be connected to either the μC master clock or to a crystal oscillator clock to drive the external smart cards. The signal is fed to the internal clock selector circuit and translated to the CRD_CLKA or CRD_CLKB pins at either the same frequency, or divided by 2, 4 or 8, depending upon the programming mode. Refer to table 2. Synchronous case: clock managed through the SPI bus − CLK_IN is disconnected. Note: The chip guarantees the EMV 50% Duty Cycle when the clock divider ratio is 1/2, 1/4, or 1/8, even when the CLK_IN signal is out of the 45% to 55% range specified by ISO and EMV specifications.
27	$\overline{CS}$	I	This pin synchronizes and enables the SPI communication. All the NCN6804 functions, both programming and card transaction, are disabled when $\overline{CS}$ = HIGH.
28	CLK_SPI		Clock Signal to synchronize the SPI data transfer. This clock is fully independent from the CLK_IN signal and does not play any role with the data transaction (I/O − CRD_I/O).
29	MISO	O	Master In Slave Out: SPI Data Output from the NCN6804. This STATUS byte carries the state of the interface, the serial transfer being achieved according to the programmed mode (Table 2), using the same CLK_SPI signal and during the same MOSI time frame. An external 4.7 kΩ pull down resistor might be necessary to avoid misunderstanding of the pin 29 voltage during the High Z state.
30	MOSI	I	Master Out Slave In: SPI Data Input from the μC. This byte contains the address of the selected chip among the two possible (bit b6), together with the programming code for a given interface. See Table 2.
31	EN_RPU	I	This pin is used to activate the I/O internal pull−up resistor such as: EN_RPU = Low => I/O Pull−up resistor disconnected EN_RPU = High => I/O Pull−up resistor connected When two or more NCN6804 chips share the same I/O bus, one chip only shall have the internal pull−up resistor enabled to avoid any overload of the I/O line. Moreover, when Asynchronous and Synchronous cards are handled by the interfaces, the activated I/O pull−up resistor must preferably be the one associated with the asynchronous circuit. On the other hand, since no internal pull−up bias resistor is built in the chip, pin 31 must be connected to the right voltage level to make sure the logic function is satisfied.
32	VDD	Power	This pin is connected to the system controller power supply (C_{bypass_min} = 100 nF). When V_{DD} is below 2.5 V the CRD_VCCA or B is disabled. The NCN6804 goes into a shutdown mode.
33	GNDD	Power	Digital/analog Ground. This pin is the Exposed Pad and is the Ground for the digital/analog circuit section. It needs to be connected to the PCB Ground.

ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model, Smart Card Pins (Card Interface Pins (Card A and B)) (Note 1) Human Body Model, CRD_DETA/B Pins (2, 23) (Note 1) Human Body Model, All Other Pins (Note 1)	 8 kV 4 kV 2 kV
Moisture sensitivity (Note 2) QFN−32	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
DC/DC Converter Power Supply Voltage ($V_{DDPA/B}$)	V_{sup} (Note 4)	$-0.5 \le V_{sup} \le 6$	V
Power Supply from Microcontroller Side (V_{DD})	V_{DD}	$-0.5 \le V_{DD} \le 6$	V
External Card Power Supply (Card A and B)	CRD_VCC	$-0.5 \le$ CRD_VCC ≤ 6	V
Digital Input Pins	V_{in} I_{in}	$-0.5 \le V_{in} \le (V_{DD} + 0.5)$ but $< 6.0 \pm 5$	V mA
Digital Output Pins (I/O, MISO, $\overline{INT}$)	V_{out} I_{out}	$-0.5 \le Vo_{ut} \le (V_{DD} + 0.5)$ but $< 6.0 \pm 10$	V mA
Smart Card Output Pins	V_{out}	-0.5 $V_{out} \le$ (CRD_VCC + 0.5) but< 6.0	V
Smart Card Output Pins Excepted CRD_CLK	I_{out}	15 (Internally Limited)	mA
CRD_CLK Pin	I_{out}	70 (Internally Limited)	mA
Inductor Current	I_{Lmax}	500 (Internally Limited)	mA
QFN−32 5x5 mm^2 package Power Dissipation @ T_A = +85°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta jA}$	 1650 40	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+125	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
4. $V_{sup} = V_{DDPA/B} = V_{DDPA}$ and V_{DDPB}

POWER SUPPLY SECTION (−40°C to +85°C, unless otherwise noted)

Pin	Symbol	Rating	Min	Typ	Max	Unit
12, 13	V_{sup}	Power Supply ($V_{DDPA/B}$) (Note 5)	2.7		5.5	V
12, 13	I_{sup}	DC Operating current – All Card Pins Unloaded, CLK_IN=Low V_{sup} = 2.7 V, CRD_VCCA or B = 5 V V_{sup} = 5.5 V, CRD_VCCA or B = 5 V			 0.5 0.5	mA
12, 13	$\overline{I_{supst}}$	Standby Supply Current, no card inserted $\overline{INT}$=CLK_IN=CLK_SPI=$\overline{CS}$= I/O = MOSI = EN_RPU = H V_{sup} = 5.5 V			 50	μA
32	V_{DD}	Operating Voltage (Note 5)	2.7		5.5	V
32	I_{VDD}	Operating Current – CLK_IN = CLK_SPI = MOSI = High, $\overline{CS}$ = I/O =Low			150	μA
32	I_{VDD_SD}	Shutdown Current – $\overline{CS}$ = High			60	μA
32	$UVLOV_{DD}$	Under voltage lockout	1.8		2.5	V
8, 17	CRD_VCC	Output Card Supply Voltage @ 2.7 V< VCC < 5.5 V CRD_VCCA/B = 1.8 V @ I_{load} = 35 mA CRD_VCCA/B = 3.0 V @ I_{load} = 60 mA CRD_VCCA/B = 5.0 V @ I_{load} = 65 mA	 1.66 2.76 4.65	 1.80 3.00 5.00	 1.94 3.24 5.35	V
8, 17	I_{CRD_VCC}	Maximum Continuous Output Current @ CRD_VCC = 1.8 V @ CRD_VCC = 3.0 V @ CRD_VCC = 5.0 V	 35 60 65			mA
8, 17	$I_{CRD_VCC_OV}$	Output Over−Current Limit : V_{sup} = 2.7 V, CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V V_{sup}= 5.5 V, CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V			 200 260	mA
8, 17	DV_{CRD_VCC}	Output Card Supply Voltage Ripple @ V_{sup} = 3.6V, L = 22 μH, C_{out} = 10 μF (Ceramic X7R), I_{CRD_VCC}= ISO Maximum Current (Note 6) CRD_VCCA/B = 5.0 V CRD_VCCA/B = 3.0 V CRD_VCCA/B = 1.8 V		 60 45 40		mV
8, 17	CRD_VCC_{TON}	Output Card Turn On Time V_{sup} = 2.7 V, CRD_VCCA/B = 5.0 V L_{out} = 22 μH, C_{out} = 10 μF Ceramic			 500	μs
8, 17	CRD_VCC_{TOFF}	Output Card Turn Off Time VCCA/P = 2.7 V, CRD_VCCA/B = 5.0 V L_{out} = 22 μH, C_{out} = 10 μF Ceramic, CRD_VCC_{OFF} < 0.4 V		 100	 250	μs

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. V_{DD} and V_{sup} have separated pads for noise and EMI immunity improvement – by similarity with the NCN6001 V_{DD} and V_{sup} have to be equal and connected to the same power supply (V_{DD} = V_{sup} = $V_{DDPA/B}$)
6. Ceramic X7R, SMD type capacitors are mandatory to achieve the CRD_VCC ripple specifications. The ceramic capacitor has to be chosen according to its ESR (very low ESR) and DC bias features. The capacitance value can strongly vary with the DC voltage applied (see Figure 22).

DIGITAL INPUT/OUTPUT SECTION CLK_IN, I/O, CLK_SPI, MOSI, MISO, $\overline{CS}$, $\overline{INT}$, EN_RPU (−40°C to +85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
26	F_{CLK_IN}	Input Asynchronous Clock Duty Cycle = 50% @ V_{DD} = 3.0 V @ V_{DD} = 5.0 V			 30 40	MHz
26	F_{tr} F_{tf}	Input Clock Rise time Input Clock Fall time	2 2			ns
28	F_{CLK_SPI}	Input SPI clock			15	MHz
28	tr_{spi}, tf_{spi}	Input CLK_SPI Rise/Falltime			12	ns
30	tr_{mosi}, tf_{mosi}	Input MOSI Rise/Falltime			12	ns
29	tr_{miso}, tf_{miso}	Output MISO Rise/Falltime @ C_S = 30 pF			12	ns
27	tr_{str}, tf_{str}	Input $\overline{CS}$ Rise/Falltime			12	ns
25	t_{RIO} t_{FIO}	I/O Data Transfer Switching Time, both directions (I/O & CRD_IOA/B) @ Cs = 30 pF I/O Rise time (see Note 7) I/O Fall time			 0.8 0.8	μs
24	R_{INT}	$\overline{INT}$ Pull Up Resistor	20	45	80	kΩ
25,26,27,28,30	V_{IH}	Positive going Input High Level Voltage Threshold (CLK_IN, MOSI, CLK_SPI, $\overline{CS}$, EN_RPU)	0.70 * V_{DD}		V_{DD}	V
25,26,27,28,30	V_{IL}	Negative going Input Low Level Voltage (CLK_IN, MOSI, CLK_SPI, $\overline{CS}$, EN RPU)	0		0.3 *V_{DD}	V
24, 29	V_{OH}	Output High Voltage $\overline{INT}$, MISO @ I_{OH} = −10 μA (source)	 V_{DD}– 1.0			V
24, 29	V_{OL}	Output Low Voltage $\overline{INT}$, MISO @ I_{OL} = 200 μA (sink)			 0.40	V
28	td_{clk_spi}	Delay Between 2 Consecutive CLK_SPI Burst Sequence	33			ns
25	$R_{pu_I/O}$	I/0 Pullup Resistor	12	18	24	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions are not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Since a 18 kΩ (Typical) pullup resistor is provided by the NCN6804, the external MPU can use an Open Drain connection. On the other hand NMOS smart cards can be used straightforward.

SMART CARD INTERFACE SECTION (−40°C to +85°C temperature range unless otherwise noted)
Note: Digital inputs undershoot ≤ 0.30V to ground, digital inputs overshoot < V_{DD} + 0.30V

Pin	Symbol	Rating	Min	Typ	Max	Unit
6,19		CRD_RSTA/B @ CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V				
	V_{OH}	Output RESET V_{OH} @ I_{rst} = −200 μA	CRD_VCC − 0.5		CRD_VCC	V
	V_{OL}	Output RESET V_{OL} @ I_{rst} = 200 μA			0.40	V
		CRD_RSTA/B @ CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V				
	t_R	Output RESET Risetime @ C_{out} = 30 pF			100	ns
	t_F	Output RESET Falltime @C_{out} = 30 pF			100	ns
3, 4 21, 22		CRD_C4A/B, CRD_C8A/B @ CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V				
	V_{OH}	Output V_{OH} @ I_{rst} = −200 μA	CRD_VCC −0.5		CRD_VCC	V
	V_{OL}	Output V_{OL} @ I_{rst} = 200 μA			0.4	V
	t_R	Output Rise time @ C_{out} = 30 pF			100	ns
	t_F	Output Fall time @C_{out} = 30 pF			100	ns
7, 18		CRD_CLKA/B as a function of CRD_VCCA/B				
		CRD_VCCA/B = 1.8 V, 3.0 V or 5.0V				
	F_{CRDCLK}	Output Frequency			20	MHz
	V_{OH}	Output V_{OH} @ Icrd_clk = −200μA	CRD_VCC−0.5		CRD_VCC	V
	V_{OL}	Output V_{OL} @ Icrd_clk = 200μA			0.4	V
		CRD_CLKA/B Output Duty Cycle				
	F_{CRDDC}	CRD_VCCA/B = 1.8 V, 3.0 V or 5.0 V	45		55	%
		Rise & Fall time @ CRD_VCCA/B = 1.8 V, 3.0 V or 5.0 V Clock programmed as FST_SLP				
	t_{ress}	Output CRD_CLKA/B Risetime @ C_{out} = 30 pF			4	ns
	t_{fcs}	Output CRD_CLKA/B Falltime @ C_{out} = 30 pF			4	ns
	t_{rills}	Rise & Fall time @ CRD_VCCA/B = 1.80V to 5.0V			16	ns
	t_{ulsa}	Clock programmed as SLO_SLP			16	ns
		Output CRD_CLKA/B Risetime @ C_{out} = 30 pF				
		Output CRD_CLKA/B Falltime @ C_{out} = 30 pF				
5,20	V_{IH}	CRD_IOA/B Input Voltage High Level @ CRD_VCCA/B = 1.8 V, 3 V and 5 V	CRD_VCC*0.6		CRD_VCC+0.3	V
	V_{IL}	CRD_IOA/B Input Voltage Low Level @ CRD_VCCA/B = 1.8 V, 3 V and 5 V	−0.30		0.80	V
	V_{OH}	Output V_{OH} @ Icrd_I/O = −20μA, V_{IH} = VDD @ CRD_VCCA/B = 1.8 V, 3 V and 5 V	CRD_VCC − 0.5		CRD_VCC	V
	V_{OL}	Output V_{OL} @ Icrd_I/O = 500 μA, V_{IL} = 0 V @ CRD_VCCA/B = 1.8 V, 3 V and 5 V	0		0.40	V
	t_R	CRD_IOA/B Rise Time, @ C_{out} = 30 pF			0.8	μs
	t_F	CRD_IOA/B Fall Time, @ C_{out} = 30 pF			0.8	μs
5, 20	R_{CRDPU}	CRD_IOA/B Pull Up Resistor	12	18	24	kΩ
2, 23		Card Detection digital filter delay:				
	T_{CRDIN}	Card Insertion	25	50	150	μs
	T_{CRDOFF}	Card Extraction	25	50	150	μs
2, 23	V_{IHDET}	Card Insertion or Extraction Positive going Input High Voltage	0.70 * VCC		VCC	V
2, 23	V_{ILDET}	Card Insertion or Extraction Negative going Input Low Voltage	0		0.30 * VCC	V

SMART CARD INTERFACE SECTION (−40°C to +85°C temperature range unless otherwise noted)
Note: Digital inputs undershoot ≤ 0.30V to ground, digital inputs overshoot < V_{DD} + 0.30V

Pin	Symbol	Rating	Min	Typ	Max	Unit
3, 4, 5, 6, 19, 20, 21, 22	Icrd	Output peak Max Current under Card Static Operation Mode @ CRD_VCC = 1.8V, 3.0V, 5.0V CRD_I/OA/B, CRD_RSTA/B, CRD_C4A/B, CRD_C8A/B			15	mA
7, 18	Icrd_clk	Output peak Max Current under Card Static Operation Mode @ CRD_VCC = 1.8 V, 3.0 V, 5.0 V CRD_CLKA/B			70	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

PROGRAMMING

Write Register → WRT_REG (Is Low Only)

Similar to the NCN6001, the NCN6804's WRT_REG register handles 3 command bits [b5:b7] and 5 data bits [b0:b4] as depicted in Tables 1 and 2. These bits are concatenated into 1 byte [MSB0,LSB0] in order to accelerate the programming sequence. The register can be updated when $\overline{CS}$ is low only.

The WRT_RGT has been defined to be compatible with the NCN6001 write register.

Table 1. WRT_REG BIT DEFINITIONS

b0
b1
	If (b7 + b6 + b5) = 000 or (b7 + b6 + b5) = 010 then
	Case 00
	CRD_VCCA = 0 V
	Case 01
	CRD_VCCA = 1.8 V
	Case 10
	CRD_VCCA = 3.0 V
	Case 11
	CRD_VCCA = 5.0 V
	Else if (b7 + b6 + b5) = 001 or (b7 + b6 + b5) = 011 then
	Case 00
	CRD_VCCB = 0 V
	Case 01
	CRD_VCCB = 1.8 V
	Case 10
	CRD_VCCB = 3.0 V
	Case 11
	CRD_VCCB = 5.0 V
	Else if (b7 + b6 + b5) =110 or (b7 + b6 + b5) = 111 then
	b1 drives CRD_C4A or B (respectively)
	b0 drives CRD_C8A or B (respectively)
	Else if (b7 + b6 + b5) =101 then
	Case 00
	CRD_DET = NO
	Case 01
	CRD_DET = NC
	Case 10
	SPI_MODE = Special
	Case 11
	SPI_MODE = Normal
	Else if (b7 + b6 + b5) =100 then
	NA (Not Applicable)
	End if

8. When operating in Asynchronous mode, b6 is compared with the external voltage level present pin S1 (Pin 1).
9. The CRD_RST pin reflects the content of the MOSI WRT_REG [b4] during the chip programming sequence. Since the bit shall be Low to address the chip's internal register, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

Table 1. WRT_REG BIT DEFINITIONS

b2
b3
	If (b7 + b6 + b5) = 000 or (b7 + b6 + b5) = 010 then
	Case 00
	CRD_CLKA = Low
	Case 01
	CRD_CLKA = CLK_IN
	Case 10
	CRD_CLKA = CLK_IN / 2
	Case 11
	CRD_CLKA = CLK_IN / 4
	
	Else if (b7 + b6 + b5) = 001 or (b7 + b6 + b5) = 011 then
	Case 00
	CRD_CLKB = Low
	Case 01
	CRD_CLKB = CLK_IN
	Case 10
	CRD_CLKB = CLK_IN / 2
	Case 11
	CRD_CLKB = CLK_IN / 4
	
	Else if (b7 + b6 + b5) =110 or (b7 + b6 + b5) = 111 then
	b3 drives CRD_CLKA or B (respectively)
	b2 drives CRD_IOA or B (respectively)
	Else if (b7 + b6 + b5) =101 then
	Case 00
	CRD_CLKA & B = SLO_SLP
	Case 01
	CRD_CLKA & B = FST_SLP
	Case 10
	NA
	Case 11
	NA
	Else if (b7 + b6 + b5) =100 then
	NA (Not Applicable)
	End if

b4	If (b7 + b6 + b5) <> 101 and (b7 + b6 + b5) <> 100 then b4 Drives CRD_RSTA or B Pin
b5 b6 b7	000 Select NCN6804 device # 1 Asynchronous Card A (Note 8) 001 Select NCN6804 device # 1 Asynchronous Card B (Note 8) 010 Select NCN6804 device # 2 Asynchronous Card A (Note 8) 011 Select NCN6804 device # 2 Asynchronous Card B (Note 8) 100 NA 101 Set Card Detection Switch polarity, Set SPI_MODE normal or special , Set CRD_CLKA & B slopes Fast or Slow 110 Select External Synchronous Card A 111 Select External Synchronous Card B

8. When operating in Asynchronous mode, b6 is compared with the external voltage level present pin S1 (Pin 1).
9. The CRD_RST pin reflects the content of the MOSI WRT_REG [b4] during the chip programming sequence. Since the bit shall be Low to address the chip's internal register, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

Table 2. WRT_REG BIT DEFINITIONS AND FUNCTIONS

ADRESS			PARAMETERS							
MSB0				LSB0				MOSI bits[b3 : b2]	MOSI bits [b1 : b0]	MOSI bits [b3 : b0]
b7	b6	b5	b4	b3	b2	b1	b0	CRD_CLK	CRD_VCC	
0	S1	A/B	CRD_RST	0	0	0	0	Low	0	
0	S1	A/B	CRD_RST	0	1	0	1	1/1	1.8V	
0	S1	A/B	CRD_RST	1	0	1	0	1/2	3.0V	
0	S1	A/B	CRD_RST	1	1	1	1	1/4	5.0V	
1	1	A/B	CRD_RST	CRD_CLK	CRD_I/O	CRD_C4	CRD_C8			Synchronous
1	0	1	X	X	0	0	0			NO
1	0	1	X	X	0	0	1			NC
1	0	1	X	X	0	1	0			Special
1	0	1	X	X	0	1	1			Normal
1	0	1	X	X	1	0	0			SLO_SLP
1	0	1	X	X	1	0	1			FST_SLP

10. Card A: b5 = 0, Card B: b5 = 1, Device # 1: b6 = 0 ⇔ pin S1 connected to GND, Device # 2: b6 = 1 ⇔ pin S1 connected to V_{DD}
11. Address 101 and bits [b0:b4] not documented in the table are not applicable with no effect on the device programming and configuration. The sign X in the table means that either 1 or 0 can be used.

Read Register → READ_REG

The READ_REG register (1 byte) contains the data read from the card interface. The selected chip register is transferred to the MISO Pin during the MOSI sequence ($\overline{CS}$ = Low).

Table 3 gives a definition of the bits.

Depending upon the programmed SPI_MODE, the content of READ_REG is transferred on the MISO line either on the Positive going (SPI_MODE = Special) or upon the Negative going slope (SPI_MODE = Normal) of the CLK_SPI signal.

The external microcontroller shall discard the three high bits since they carry no valid data.

Table 3. MOSI AND MISO BITS IDENTIFICATIONS AND FUNCTIONS

MOSI	b7	b6	b5	b4	b3	b2	b1	b0	Operating Mode
	0	0	0	CRD_RST	CRD_CLK	CRD_CLK	CRD_VCC	CRD_VCC	Async. Card A, Program Chip
	0	0	1	CRD_RST	CRD_CLK	CRD_CLK	CRD_VCC	CRD_VCC	Async. Card B, Program Chip
	0	1	0	CRD_RST	CRD_CLK	CRD_CLK	CRD_VCC	CRD_VCC	Async. Card A, Program Chip
	0	1	1	CRD_RST	CRD_CLK	CRD_CLK	CRD_VCC	CRD_VCC	Async. Card B, Program Chip
	1	1	0	CRD_RST	CRD_CLK	CRD_I/O	CRD_C4	CRD_C8	Sync. Card A, Sets Card Bits
	1	1	1	CRD_RST	CRD_CLK	CRD_I/O	CRD_C4	CRD_C8	Sync. Card B, Sets Card Bits
MISO	z	z	z	Card Detect	CRD_I/O	CRD_C4	CRD_C8	PWR Monitor	Read Back Data

When a command is sent to A for example by selecting the address %000 the corresponding MISO byte has the state of the interface A (Card detectA, b4; I/OA, b3; C4A, b2; C8A, b1; CRD_VCCA ok, b0) – that is the state loaded while sending the previous MOSI command A or B.

When a command is sent to B for example by selecting the address %001 the corresponding MISO byte has the state of the interface B (Card detectB, b4; I/OB, b3; C4B, b2; C8B, b1; CRD_VCCB ok, b0) – that is the state loaded while sending the previous MOSI command A or B.

Card A or Card B Selection – Multiplexed Mode

The bit b5 in the MOSI sequence enables the selection of the NCN6804's interface A or B (see Table 2) to the exception of the addresses {100} decoded with no effect on the device and {101} used to program device general configuration. Then:

When b5 = LOW the interface A is selected and the transaction or communication takes place through this interface according to Table 2. The programming applies to Card A only.

When b5 = HIGH the interface B is selected and the transaction or communication takes place through this interface according to Table 1. The programming applies to Card B only.

CRD_VCCA and CRD_CLKA can be maintained applied to card A when the device is switched from A to B. This mode of operating is of course the same when the device is switched from B to A: CRD_VCCB and CRD_CLKB can be maintained applied to card B.

The device configuration is programmed using the address {101} similarly to the NCN6001. In that case, the programming is applied simultaneously to Card A and Card B.

Asynchronous Mode

In this mode, the S1 pin is used to define the physical address (by comparison with the bit b6 (MOSI)) of the interfaces when a bank of up to 2 NCN6804 (total of 4 interfaces) shares the same digital bus.

Synchronous Mode

In this mode, the CLK_IN clock input and the I/O input/output are not used. The clock and the data are provided and transferred through the SPI bus using MOSI and MISO as shown Table 2.

When this operating mode is used and if two NCN6804 devices want to be implemented, it is no longer possible to share the same $\overline{CS}$ signal. Consequently in this particular case and when the devices operate in a multiple interface mode a dedicated $\overline{CS}$ signal must be provided to each NCN6804 device.

Since bits [b4 – b0] of the MOSI register contain the smart card data, programming the CRD_VCC output voltage shall be done by sending a previous MOSI message according to Table 2 using the address [b7, b6, b5] = [0, S1, A/B]. For example if a synchronous card is used, prior to make a transaction with it, it will be powered−up for example at 5 V by sending the command %00000011 (address S1 = 0 and card A selected).

The CRD_RSTA/B pin reflects the content of the MOSI WRT_REG [b4] during the chip programming sequence. Since this bit shall be LOW to address the internal register of the chip, care must be observed as this signal will be immediately transferred tot he CRD_RSTA/B pin.

Startup Default Conditions

At startup, when power supply is turned on, the internal POR (Power On Reset) circuit sets the chip in the default conditions as defined below (Table 4).

Table 4. STARTUP DEFAULT CONDITIONS

CRD_DETA/B	Normally Open
CRD_VCCA/B	OFF
CRD_CLKA/B	tr & tf = SLOW
CRD_CLKA/B	LOW
Protocol	Special Mode
I/O Pull−up resistor	Connected
$\overline{INT}$	High

Card Detection

The card is detected by the external switch connected to pin 23 for Card B and pin 2 for Card A. The internal circuit provides a positive bias of this pin and the polarity of the insertion/extraction is programmable by the MOSI protocol as depicted Table 2.

The bias current is 1μA typical and cares must be observed to avoid leakage to ground from this pin to maintain the logic function. In particular, using a low impedance probe (< 1 MΩ) might lead to uncontrolled operation during the debug.

Depending upon the programmed condition, the card can be detected either by a Normally Open (default condition) or a Normally Close switch (see Table 2). On the other hand, the meaning of the feedback message contained in the MISO register bit b4 depends upon the SPI mode of operation as defined here below:

SPI Normal Mode: the MISO bit b4 is High when a card is inserted, whatever be the polarity of the card detect switch.

SPI Special Mode: the MISO bit b4 copies the logic state of the Card detect switch as depicted here below, whatever be the polarity of the switch used to handle the detection:

CRD_DETA/B = Low ⇒ MISO / b4 = LOW

CRD_DETA/B = High ⇒ MISO / b4 = HIGH

CRD_VCC Operation

The dual NCN6804 interface has 2 built−in DC/DC converters. Each of them can be programmed to provide one of the three possible values, 1.8 V, 3.0 V or 5.0 V, assuming the input voltage VDDPA or B is within the 2.7 V to 5.5 V range. Card A and Card B can be independently powered−up or down. Consequently if necessary for example the device can be switched from card A to card B while the card A power voltage is maintained (this is of course true from A to B or from B to A). CRD_VCCA & B are voltage regulated and protected against overload by a current overload detection system. The DC/DC converter operates as a buck/boost converter. The power conversion mode is automatically switched to handle one of these two modes of operation depending upon the voltage difference between the CRD_VCCA or B and VDDPA or B respectively.

The CRD_VCCA or B output current range is given Table 5; these values comply with the smart card ISO7816 standard and related.

Table 5. CRD_VCCA OR B OUTPUT VOLTAGE DEFINITION

CRD_VCCA or B	Current range per Card	Cumulated Current Range (Card A and Card B)
1.8 V	0 to 35+ mA	0 to 70 + mA
3.0 V	0 to 60+ mA	0 to 120 + mA
5.0 V	0 to 65+ mA	0 to 130 + mA

Whatever is the CRD_VCCA or B output voltage, a built−in comparator makes sure the voltage is within the ISO7816−3/EMV specifications. If the voltage is no longer within the minimum/maximum values, the DC/DC is switched off, the powerdown sequence takes place and an interrupt is presented at the $\overline{INT}$ Pin 24.

Powerup Sequence

The Powerup Sequence makes sure all the card related signals are Low during the CRD_VCCA/B positive going slope. These lines are validated when CRD_VCCA/B is above the minimum voltage specified by the EMV standard depending upon the programmed CRD_VCC A or B value (see CRD_VCC Power Supply).

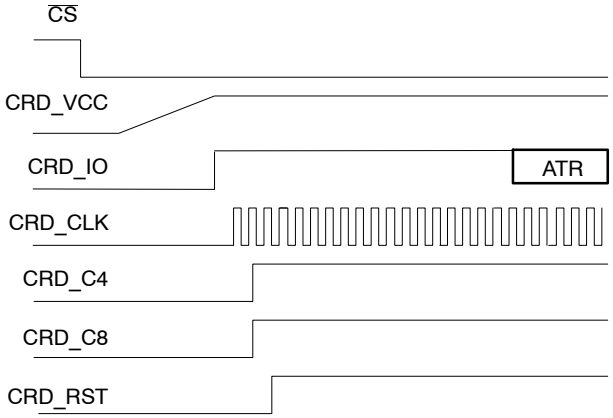


Figure 3. Startup CRD_VCC Sequence

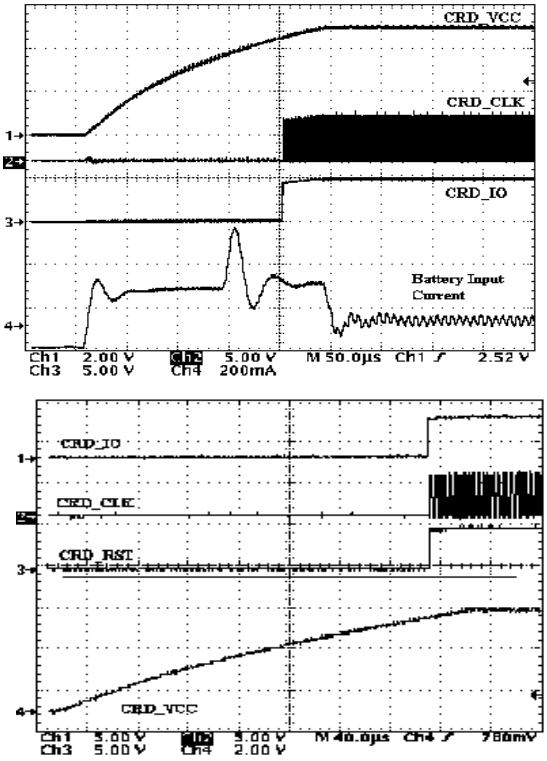


Figure 4. Measured Typical Startup CRD_VCC Sequence

At powerup, the CRD_VCCA/B turn−on time depends upon the current capability of the DC/DC converter associated with the external inductor L and the reservoir capacitor connected across CRD_VCCA or B and GROUND. During this sequence, the average input current is 300 mA typical (see Figure 4), assuming the system is fully loaded during the start up.

Even if enabled by the built−in sequencer the activation sequence is under the control and responsibility of the application software.

On the other hand, at turn off, the CRD_VCCA/B fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal NMOS transistor built across CRD_VCCA/B and Ground. These behaviors are depicted Figure 5.

Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the t_{ON} or t_{OFF} provided by the datasheet does not meet his requirements.

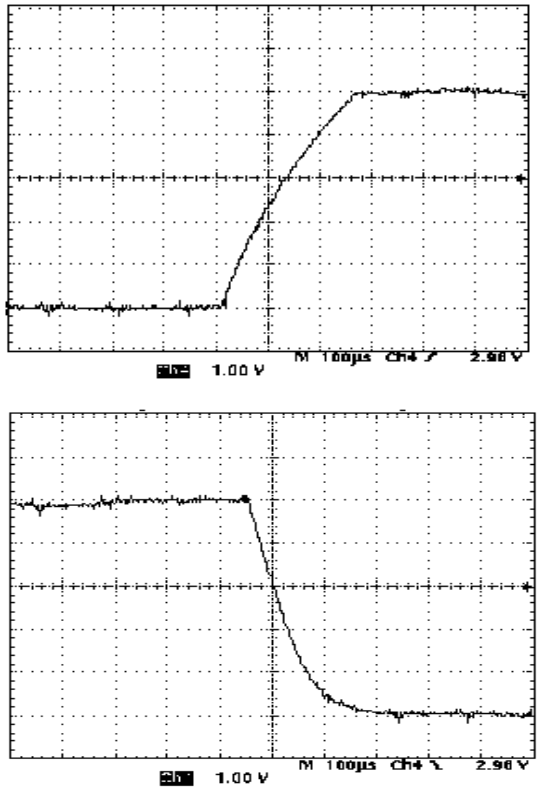


Figure 5. CRD_VCC Typical Turn−on and Turn−off Times

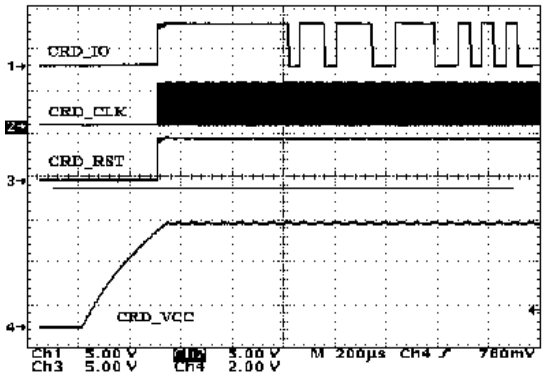


Figure 6. Figure 7: Start Up Sequence with ATR.

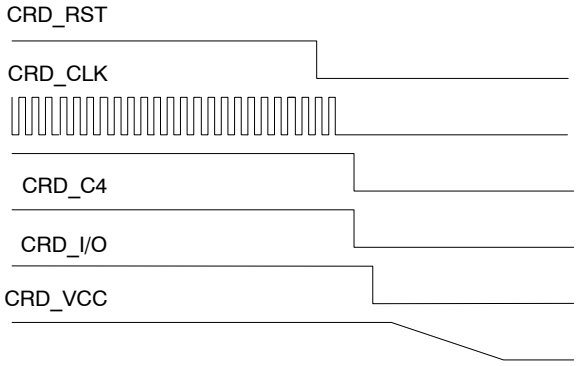


Figure 7. Typical Power Down Sequence
(Typical Delay Between Each Signal is 500 ns)

Powerdown Sequence

The NCN6804 provides an automatic Power Down sequence, according to the ISO7816−3 specifications. When a power down sequence is enabled the communication session terminates immediately. The sequence is launched under a micro−controller decision, when the card is extracted, or when the CRD_VCCA/B voltage is overloaded as described by the ISO/CEI 7816−3 sequence depicted here after (see Figure 8):

→ CRD_ RST is forced to Low
→ CRD_CLK is forced to Low, unless it is already in this state
→ CRD_C4 & CRD_C8 are forced to Low
→ Then CRD_IO is forced to Low
→ Finally the CRD_VCC supply is powered down

Since the internal digital filter is activated for any card insertion or extraction, the physical power−down sequence will be activated 50 µs (typical) after the card has been extracted. Of course, such a delay does not exist when the micro−controller intentionally launches the power down.

Data I/O Level Shifter

The level shifter accommodates the voltage difference that might exist between the micro−controller and the smart card. A pulsed accelerator circuit provides the fast positive going transient according to the ISO7816−3 specifications. The basic I/O level shifter is depicted Figure 8.

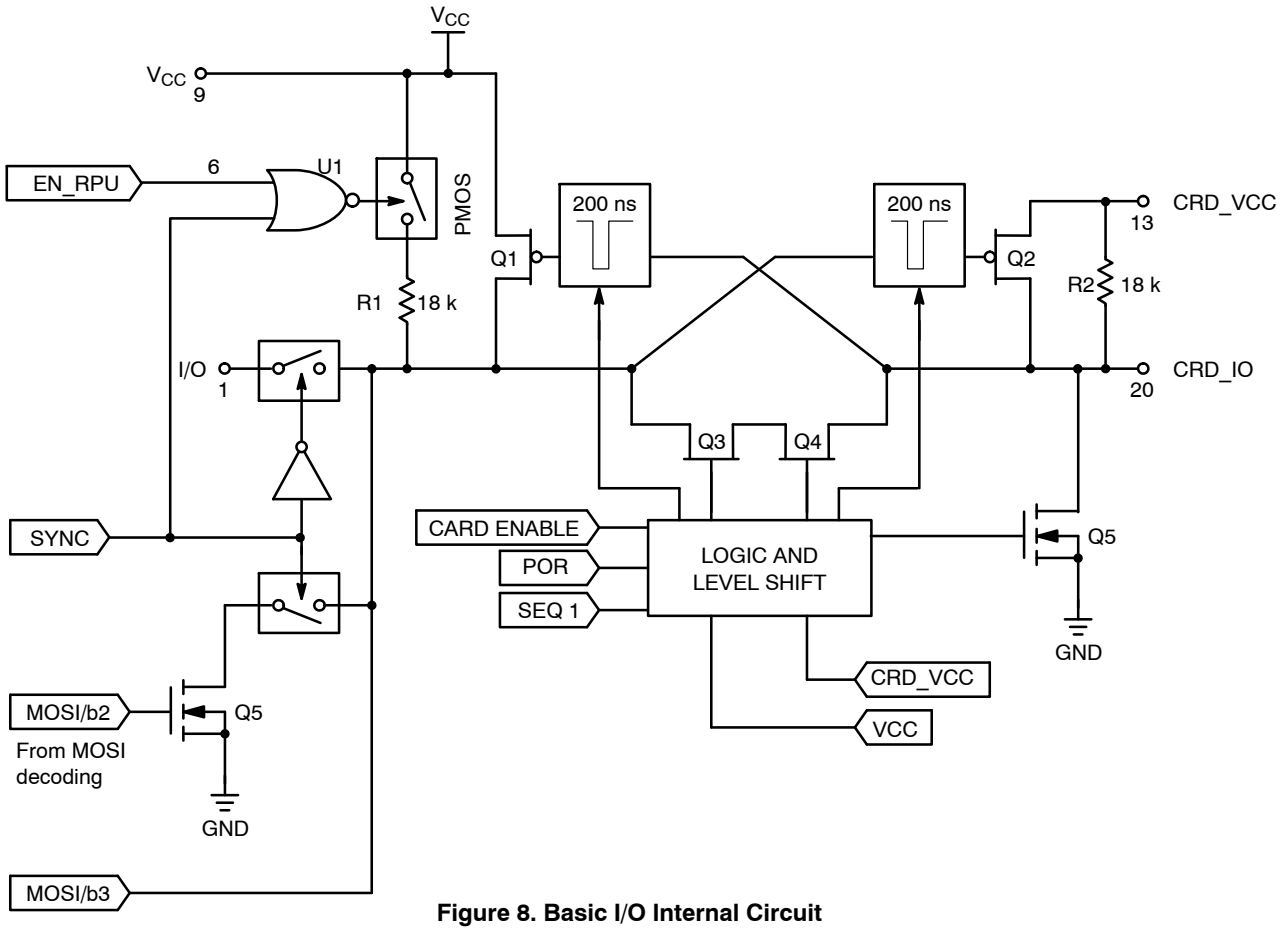


Figure 8. Basic I/O Internal Circuit

The transaction is valid when the Chip Select pin is Low, the I/O signal being Open Drain or Totem Pole on either sides.

Since the device can operate either in a single or a multiple card system provisions have been made to avoid CRD_IOA or B current overload. Depending upon the selected mode of operation (Async. or Sync), the card I/O line is respectively connected to either I/O Pin 25, or to the MOSI register byte bit 2. On the other hand, the logic level present at the card I/O is feedback to the micro−controller via the MISO register bit 3. The logic levels present at Pin 31 (EN_RPU) controls the connection of the internal pullup as depicted Table 6.

Table 6. I/O PULLUP RESISTOR TABLE

EN_RPU	I/O Pullup Resistor	Device Operation
Low	Open, 18 kΩ Disconnected	Applicable in the Multidevice Mode Case
High	Internal 18 kΩ Pullup Active	Single Device Mode

NOTE: 18 kΩ typical value

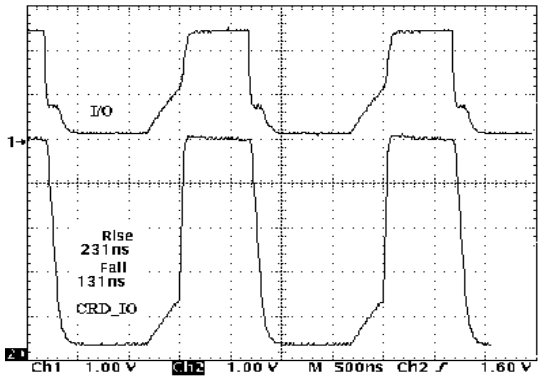


Figure 9. Typical I/O rise & fall time (CRD_IOA or B/ C_{out} > 30 pF and open−drain)

Interrupt

When the system is powered up, the $\overline{INT}$ Pin is set to HIGH upon Power On Reset (POR) signal. The interrupt Pin 24 is forced LOW when a card is inserted or extracted in either of the external ports, or when a fault is developed across the CRD_VCC output voltage A or B. This signal is neither combined with $\overline{CS}$ signal, nor with the chip address. The $\overline{INT}$ signal is clear to HIGH upon one of the conditions Table 7.

Table 7. INTERRUPT RESET LOGIC TABLE

Interrupt Source ($\overline{INT}$ set to LOW)	$\overline{CS}$	Interrupt Clearance ($\overline{INT}$ reset to HIGH) CRD_VCCA/B / {b1, b0} Programming	Chip Address
Card Insertion	L	{0,1}, {1,0} or {11}	{b7:b5} = 0XX
Card Extraction	L	{0,0}	{b7:b5} = 0XX
Over Load	L	{0,0}	{b7:b5} = 0XX

In order to know the source of the interrupt (card A or card B), the software has to poll the MISO register by sending a MOSI A command (address {b7, b6, b5} = {0, X, 0}) followed by a MOSI B command (address {b7, b6, b5} = {0, X, 1}) (or conversely). The corresponding MISO content provides the previous state of the interface A or B that is the information related to the cause of the interrupt. For each case the MISO status obtained will be compared with the MISO state prior to the interrupt. When 2 NCN6804 devices share the same digital SPI bus, it is up to the software to poll the devices using again the MISO register to identify the reason of the interrupt.

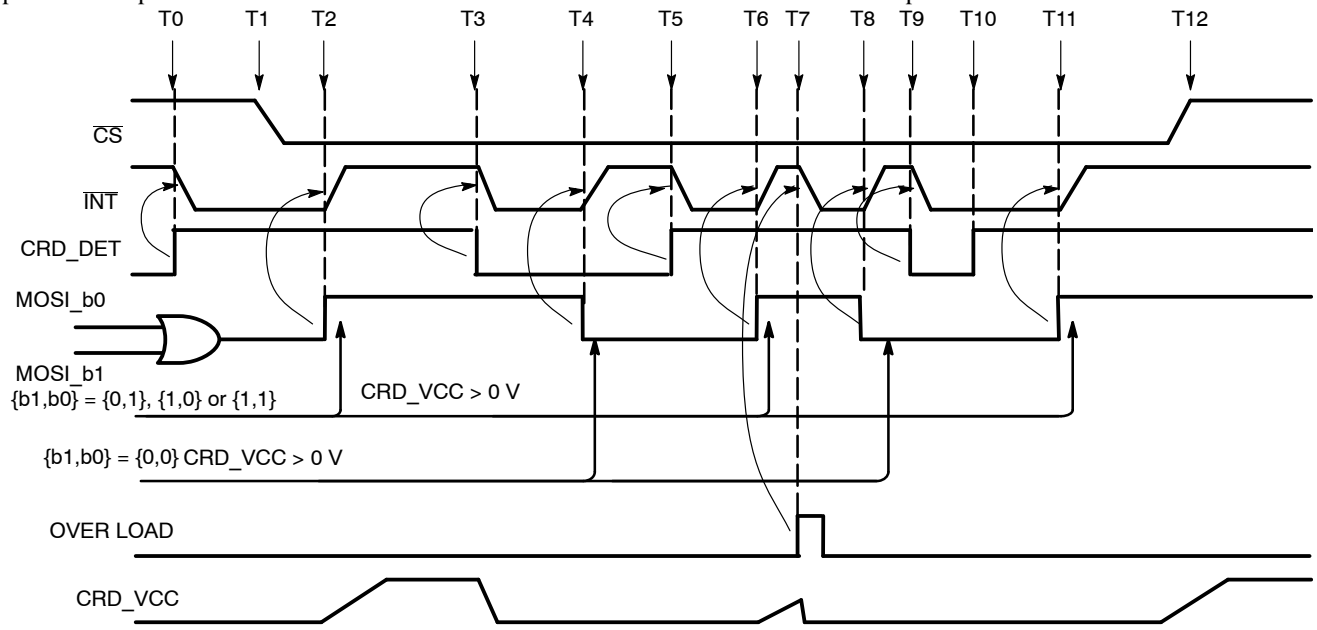


Figure 10. Basic Interrupt Function

Table 8. INTERRUPT FUNCTION OPERATION

T0	A card has been inserted into the reader and detected by the CRD_DET signal. The NCN6001 pulls down the interrupt line.
T1	The μC sets the $\overline{CS}$ signal to Low, the chip is now active, assuming the right address has been placed by the MOSI register.
T2	The μC acknowledges the interrupt and resets the $\overline{INT}$ to High by the MOSI [B1 : B0] logic state: CRD_VCC is programmed higher than zero volt.
T3	The card has been extracted from the reader, CRD_DET goes Low and an interrupt is set ($\overline{INT}$ = L). On the other hand, the PWR_DOWN sequence is activated by the NCN6001.
T4	The interrupt pin is clear by the zero volt programmed to the interface.
T5	Same as T0
T6	The μC start the DC/DC converter, the interrupt is cleared (same as T2)
T7	An overload has been detected by the chip : the CRD_VCC voltage is zero, the $\overline{INT}$ goes Low.
T8	The card is extracted from the reader, CRD_DET goes Low and an interrupt is set ($\overline{INT}$ = L).
T9	The card is re−inserted before the interrupt is acknowledged by the μC: the $\overline{INT}$ pin stays Low.
T10	The μC acknowledges the interrupt and reset the $\overline{INT}$ to High by the MOSI [B1 : B0] logic state: CRD_VCC is programmed higher than zero volt.
T11	The Chip Select signal goes High, all the related NCN6001 interface(s) are deactivated and no further programming or transaction can take place.

SPI Port

The product communicates to the external micro controller by means of a serial link using a Synchronous Port Interface protocol, the CLK_SPI being Low or High during the idle state. The NCN6804 is not intended to operate as a Master controller, but executes commands coming from the MPU.

The CLK_SPI, $\overline{CS}$ and MOSI signals are under the microcontroller's responsibility. The MISO signal is generated by the NCN6804, using the CLK_SPI and CS lines to synchronize the bits carried out by the data byte. The basic timings are given in Figure 11 and 12. The system runs with two internal registers associated with MOSI and MISO data:

WRT_REG is a write only register dedicated to the MOSI data.

READ_REG is a read only register dedicated to the MISO data.

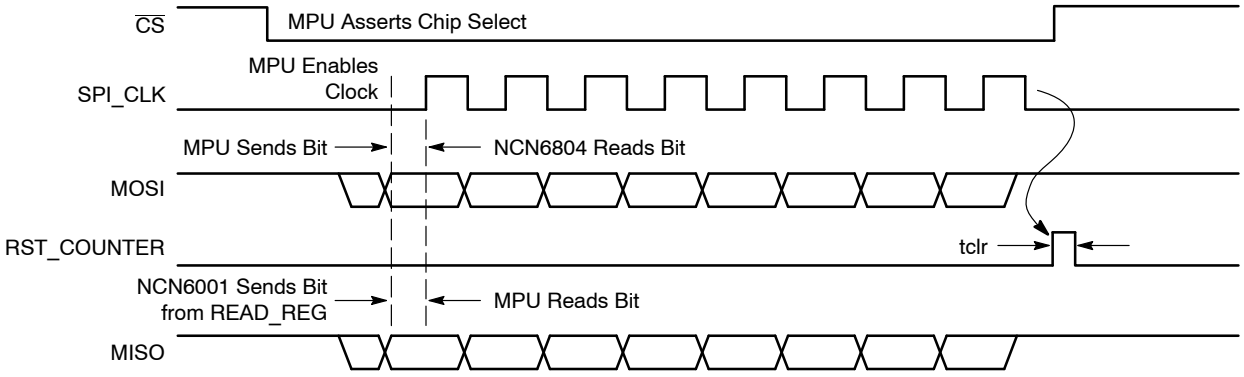


Figure 11. Basic SPI Timings and Protocol

When the $\overline{CS}$ line is High, no data can be written or read on the SPI port. The two data lines become active when $\overline{CS}$ = Low, the internal shift register is cleared and the communication is synchronized by the negative going edge of the $\overline{CS}$ signal. THe data presents on the MOSI line are considered valid on the negative going edge of the CLK_SPI clock and is transferred to the shift register on the next positive edge of the same CLK_SPI clock.

To accommodate the simultaneous MISO transmit, an internal logic identifies the chip address on the fly (reading and decoding the three first bits) and validate the right data present on the line. Consequently, the data format is MSB first to read the first three signal as bits b5, b6 and b7. The chip address is decoded from this logic value and validates the chip according to the S1 pin conditions: see Figure 12.

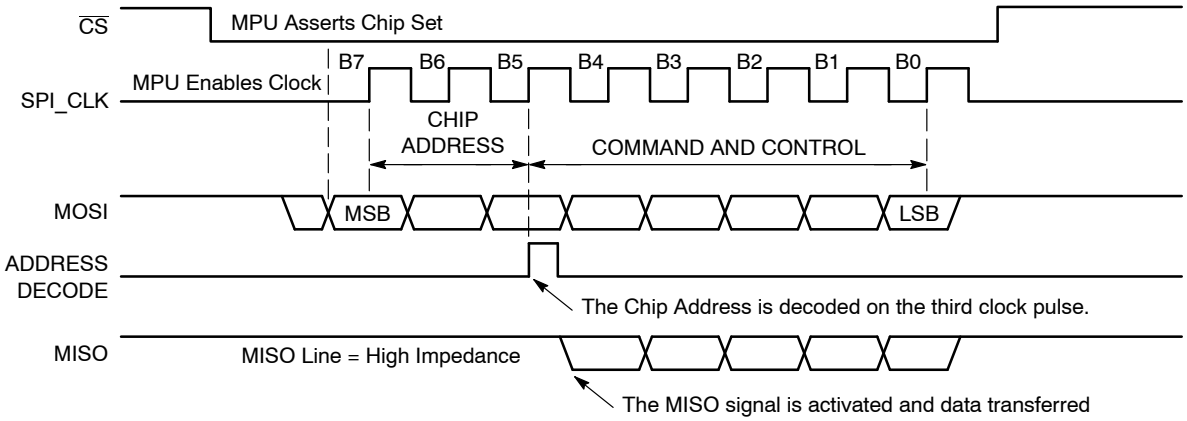


Figure 12. Chip Address Decoding Protocol and MISO Sequence

When the bit transfer is completed, the content of the internal shift register is latched on the positive going edge of the $\overline{CS}$ signal and the NCN6804 related functions are updated accordingly.

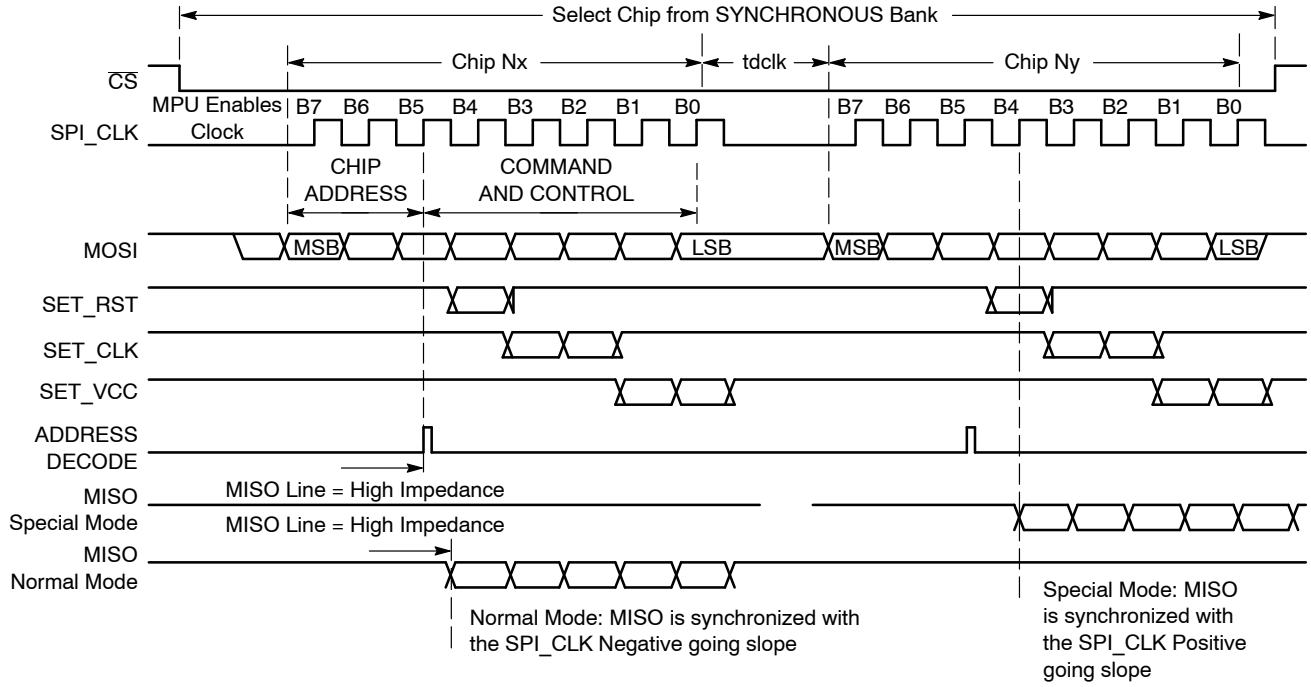


Figure 13. Basic Multi Command SPI Bytes

Since the 2 dual circuits present in the Asynchronous Bank have an individual physical address, the system can control 2 of these chips by sending the data content within the same $\overline{CS}$ frame as depicted in Figure 13. The bits are decoded on the fly and the related sub blocks are updated accordingly. According to the SPI general specification, no code or activity will be transferred to any chip when the $\overline{CS}$ is High.

When 2 SPI dual bytes are sequentially transferred on the MOSI line, the CLK_SPI sequence must be separated by at least one half positive period of this clock (see td_{clk} parameter).

The oscillograms given Figures 14 and 15 illustrate the SPI communication protocol.

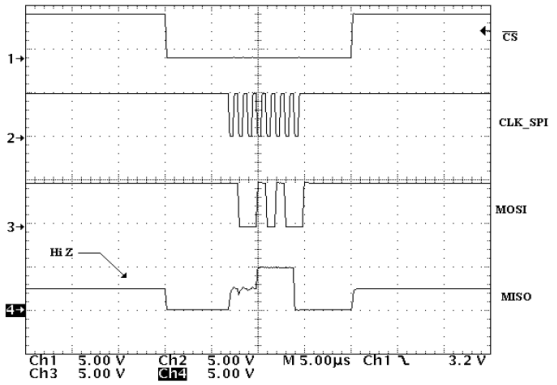
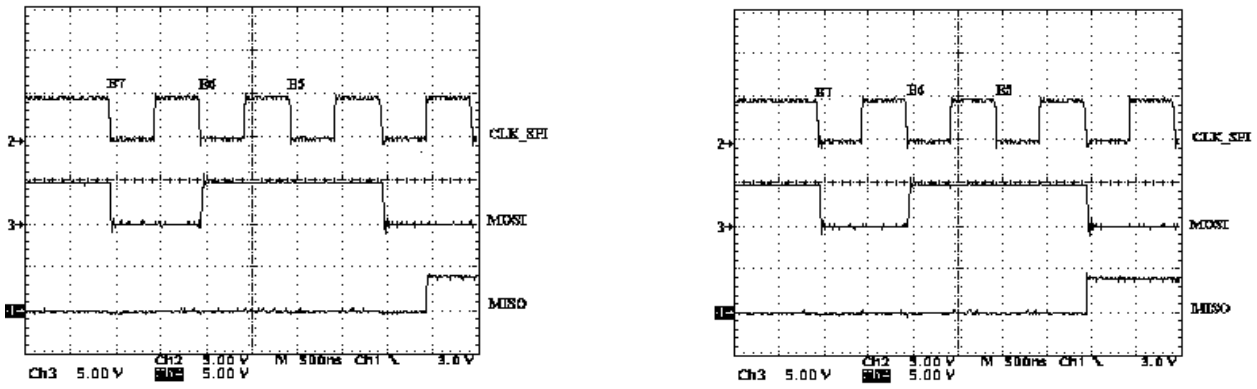


Figure 14. Programming Sequence



Special mode

Standard mode

Figure 15. MISO Read Out Sequences

DC/DC Operation

The power conversion is based on a full bridge structure able to handle either step up or step down power supply (see Figure 16). The operation is fully automatic and, beside the output voltage programming, does not need any further adjustment.

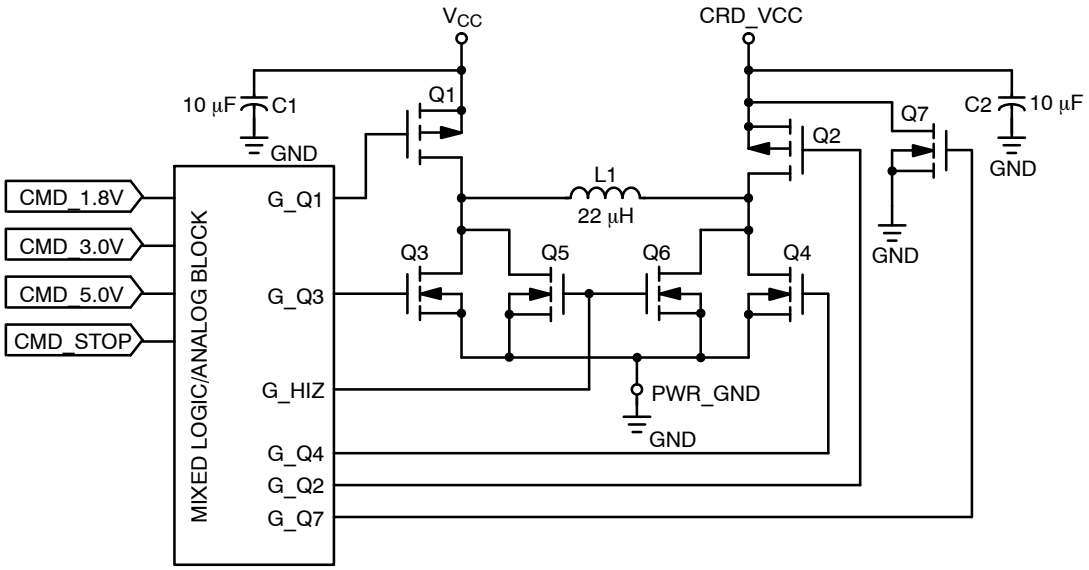


Figure 16. Basic DC/DC Converter

In order to achieve the 250 µs maximum time to discharge CRD_VCCA or B to 400 mV called by the EMV specifications, an active pull down NMOS is provided to discharge the external CRD_VCCA/B reservoir capacitor. This timing is guaranteed for a 10 µF maximum load reservoir capacitor value (see Figure 4).

The system operates with a two cycle concept (all comments are referenced to Figures 16 and 17):

1. Cycle 1 Q1 and Q4 are switched ON and the inductor L1 is charged by the energy supplied by the external battery. During this phase, the pair Q2/Q3 and the pair Q5/Q6 are switched OFF. The current flowing the two MOSFET Q1 and Q4 is internally monitored and will be switched OFF when the I_{peak} value (depending upon the programmed output voltage value) is reached. At this point, Cycle 1 is completed and Cycle 2 takes place. The ON time is a function of the battery voltage and the value of the inductor network (L and Zr) connected across pins 10/11. A 4 _s timeout structure ensures the system does run in a continuous Cycle 1 loop.
2. Cycle 2 Q2 and Q3 are switched ON and the energy stored into the inductor L1 is dumped into the external load through Q2. During this phase, the pair Q1/Q4 and the pair Q5/Q6 are switched OFF. The current flow period is constant (900 ns typical) and Cycle 1 repeats after this time if the CRD_VCC voltage is below the specified value.

When the output voltage reaches the specified value (1.8 V, 3.0 V or 5.0 V), Q2 and Q3 are switched OFF immediately to avoid over voltage on the output load. In the meantime, the two extra NMOS Q5 and Q6 are switched ON to fully discharge any current stored into the inductor, avoiding ringing and voltage spikes over the system. Figure 17 illustrates the theoretical waveforms present in the DC/DC converter.

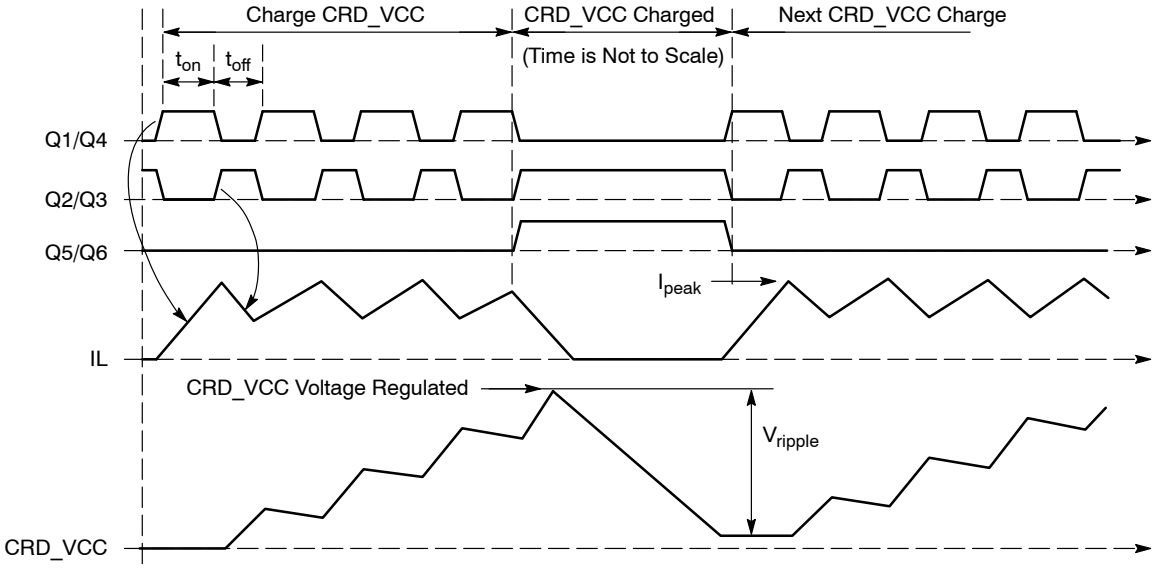


Figure 17. Theoretical DC/DC Operating Waveforms

When the CRD_VCC is programmed to zero volt, or when the card is extracted from the socket, the active pull down Q7 rapidly discharges the output reservoir capacitor, making sure the output voltage is below 0.4 V when the card slides across the ISO contacts.

Based on the experiments carried out during the NCN6804 characterization, the best comprise, at time of printing this document, is to use two 4.7 µF/10 V/ ceramic/X7R capacitors in parallel to achieve the CRD_VCC filtering. The ESR will not extend 50 mΩ over the temperature range and the combination of standard parts provides an acceptable –20% to +20% tolerance, together with a low cost. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application. Figure 18 illustrates the CRD_VCC ripple observed in the NCN6804 demoboard depending upon the type of capacitor used to filter the output voltage.

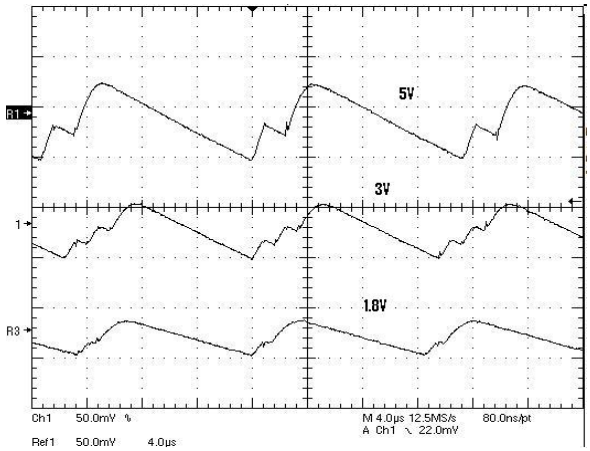


Figure 18. Typical CRD_VCC Ripple Voltage (5 V, 3 V and 1.8 V) – cms Capacitor C_{OUT} = 10 µF, 1210, X7R, 16 V

During the operation, the inductor is subject to high peak current as depicted Figure 19 and the magnetic core must sustain this level of current without damage. In particular, the ferrite material shall not be saturated to avoid uncontrolled current spike during the charge up cycle. Moreover, since the DC/DC efficiency depends upon the losses developed into the active and passive components, selecting a low ESR inductor is preferred to reduce these losses to a minimum.

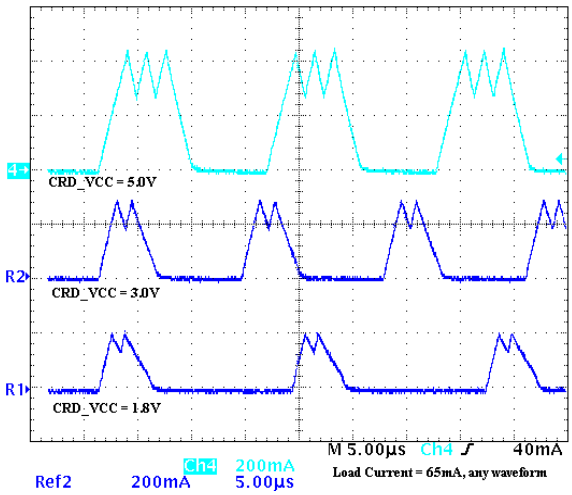


Figure 19. Typical Inductor Current

According to the ISO7816−3 and EMV specifications, it is recommended the interface limits the CRD_VCC output current to 200 mA maximum, under short circuit conditions. The NCN6804 supports such a parameter, the limit being depending upon the input and output voltages as depicted Figure 20.

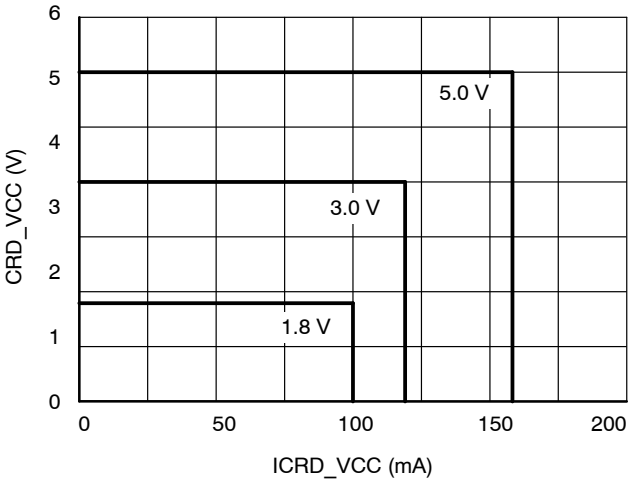


Figure 20. Output Current Limit: Output voltage CRD_VCC (1.8 V, 3.0 V, 5.0 V)

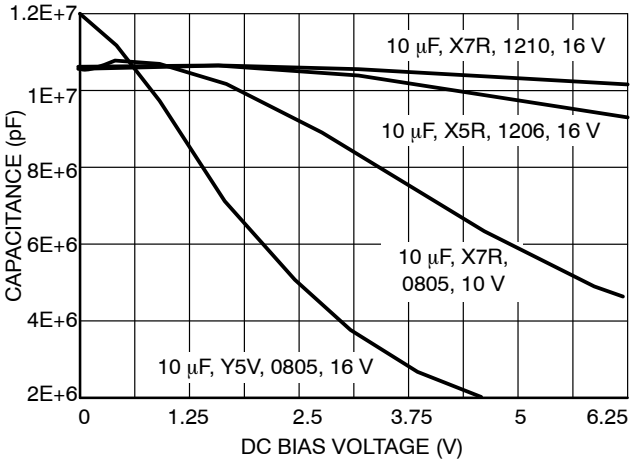


Figure 21. Variation of the Capacitance Value of Different CMS Capacitors with the DC Voltage Applied Across its Terminals

On the other hand, the circuit is designed to make sure no over current exist over the full temperature range. As a matter of fact, the output current limit is reduced when the temperature increases.

DC−TO−DC Converter External PASSIF Component Selection

To be functional the NCN6804's DC−to−DC converters need external passive components carefully selected. The performance and specification compliance of the NCN6804 are guaranteed by the DC/DC converter input capacitor, by the inductor and the reservoir capacitor characteristics. The input capacitor enables the decoupling and filtering of the input power supply voltage (V_{BAT}) and its value has to be high enough to guarantee a good operating stability of the converter. A CMS very low ESR capacitor shall be preferably used with a minimum value of 4.7 μF recommended, 10 μF will be preferred − this will strongly depend on how the capacitance value varies with the DC voltage applied across the capacitor terminals (see Figure 21). The inductor shall be sized to handle the 500 mA peak current (Min. I_{sat}) flowing during the DC/DC operation and will have to offer a low parasitic series resistor in order to maintain a good efficiency (Ex: Coilcraft, 1008PS−223KLC). The reservoir output capacitor shall be also ceramic surface mount capacitor with very low ESR (lower than 50 mΩ) and good temperature characteristics (X7R type). 10 μF is the recommended capacitance value under 5 V, 3 V and 1.8 V to get the better operating performance with a low CRD_VCC ripple level. The CMS capacitor shall be selected accordingly that is with a capacitance value of 10 μF covering the range 1.8 V – 5 V (see Figure 21). This value constitutes a good compromise for a good CRD_VCC ripple and CRD_VCC turn−on and turn−off times.

Smart Card Clock Divider

The main purpose of the built in clock generator is three folds:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Controls the clock state according to the smart card specification.

In addition, the NCN6804 adjusts the signal coming from the μC to get the Duty Cycle window as defined by the ISO7816−3 specification.

The byte content of the SPI port b2 and b3 fulfills the programming functions when $\overline{CS}$ is Low as depicted Figures 22 and 23. The clock input stage (CLOCK_IN) can handle a 40 MHz frequency maximum signal, the divider being capable to provide a 1:4 ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a given application and, in any case, the output clock [CRD_CLKA/B] shall be limited to 20 MHz maximum. In order to minimize the dI/dt and dV/dV developed in the CRD_CLKA/B line, the output stage includes a special function to adapt the slope of the clock signal for different applications. This function is programmed by the MOSI register (see Table 2) whatever be the clock division.

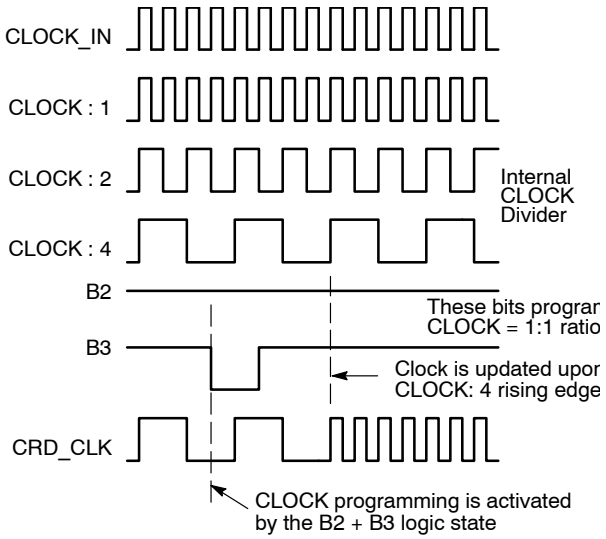


Figure 22. Typical Clock Divider Synchronization

In order to avoid any duty cycle out of the smart card ISO7816−3 specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio (see Figure 22). Consequently, the output CRD_CLKA/B frequency division can be delayed by four CLOCK_IN pulses and the micro controller software must take this delay into account prior to launch a new data transaction. On the other hand, the output signal Duty Cycle cannot be guaranteed 50% if the division ratio is 1 and if the input Duty Cycle signal is not within the 46% – 56% range.

The input signals CLK_IN and MOSI/b3 are automatically routed to the level shifter and control block according to the mode of operation.

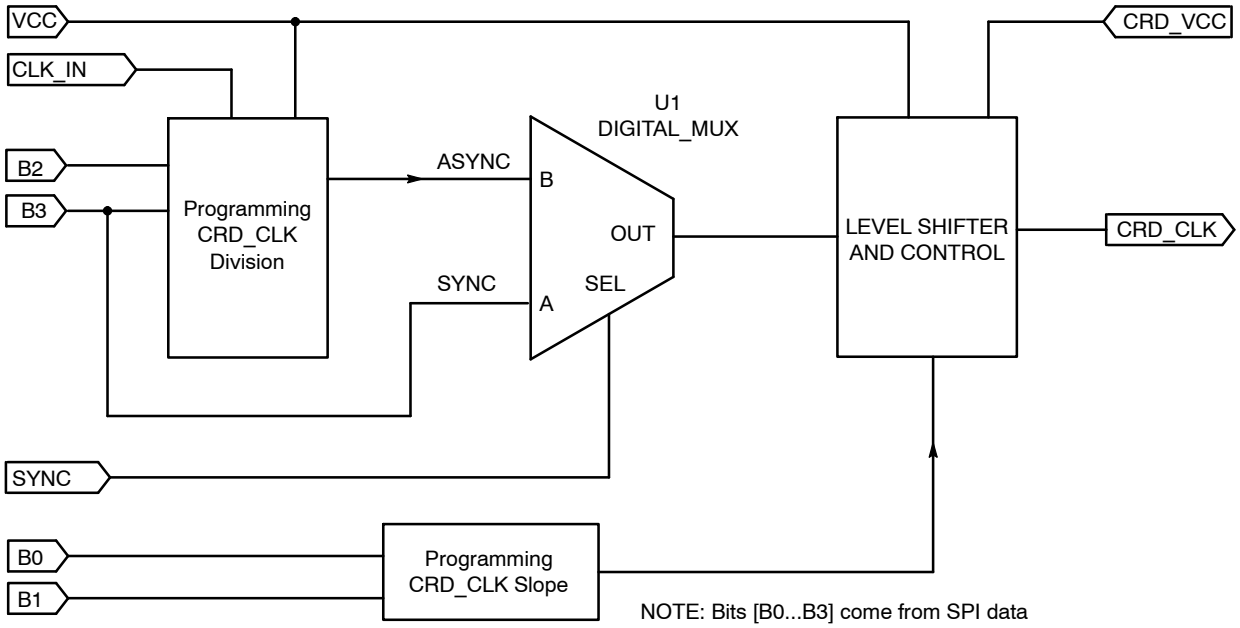


Figure 23. Basic Clock Divider and Level Shifter

The input clock can be divided by 1/1, ½, or ¼,, depending upon the specific application, prior to be applied to the smart card driver. On the other hand, the positive and negative going slopes of the output clock (CRD_CLKA/B) can be programmed to optimize the operation of the chip: see Table 2. The slope of the output clock can be programmed on the fly, independently of either the CRD_VCCA/B voltage or the operating frequency, but cares must be observed as the CRD_RSTA/B will reflect the logic state present at MOSI / b4 register.

Table 9. OUTPUT CLOCK RISE AND FALL TIME SELECTION

B0	B1	CRD_CLK Division Ratio	CRD_CLK SLO_SLP	CRD_CLK FST_SLP
0	0	–	Output Clock = Low	Output Clock = Low
0	1	1	10 ns (typ.)	2 ns (typ.)
1	0	1/2	10 ns (typ.)	2 ns (typ.)
1	1	1/4	10 ns (typ.)	2 ns (typ.)

Input Schmitt Triggers

All the Logic Input pins have built in Schmitt trigger circuits to protect the NCN6804 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted Figure 24.

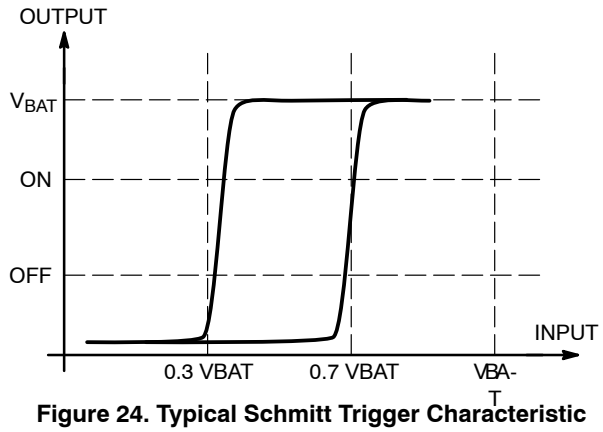


Figure 24. Typical Schmitt Trigger Characteristic

Security Features

In order to protect both the interface and the external smart card, the NCN6804 provides security features to prevent irreversible failures as described here after.

Pin Current Limitation: In the case of a short circuit to ground, the current forced by the device is limited to 15 mA for any pins, except CRD_CLK A/B pin which is limited to 70 mA. No feedback is provided to the external MPU.

DC/DC Operation: The internal circuit continuously senses the CRD_VCCA/B voltage; in the case of either over or undervoltage situation it updates the READ_REG register accordingly and forces the $\overline{\text{INT}}$ Pin to Low. This register can be readout by the MPU.

Battery Voltage: Both the Over and Undervoltage are detected by the NCN6804, the READ_REG register being updated accordingly. The external MPU can read the register through the MISO pin to take whatever is appropriate to cope with the situation.

ESD Protection

The NCN6804 dual smart card interface features an HBM ESD voltage protection (JEDEC standard) in excess of 8 kV for all the CRD pins (CRD_IOA/B, CRD_CLKA/B, CRD_RSTA/B, CRD_$V_{CCA/B}$ and GND). CRD_DETA/B have a protection of 4 kV HBM. All the other pins (microcontroller side) sustain at least 2 kV.

These values are guaranteed for the device in its full integrity without considering the external capacitors added to the circuit for a proper operating. Consequently in the operating conditions it is able to sustain much more than 8 kV on its CRD pins making it perfectly protected against electrostatic discharge well over the HBM ESD voltages required by the ISO7816 standard.

Printed Circuit Board Layout

Careful layout routing will be applied to achieve a good and efficient operating of the device in its application environment and to fully exploit its performance. The bypass capacitors have to be connected as close as possible to the device pins (CRD_VCCA/B, VDD or VDDPA/B) in order to reduce as much as possible parasitic behaviors (ripple and noise). It is recommended to use ceramic capacitors (very low ESR).

The exposed pad of the QFN−32 package will be connected to the ground. A relatively large ground plane is recommended. Figure 25 shows a example of PCB device implementation and component routing.

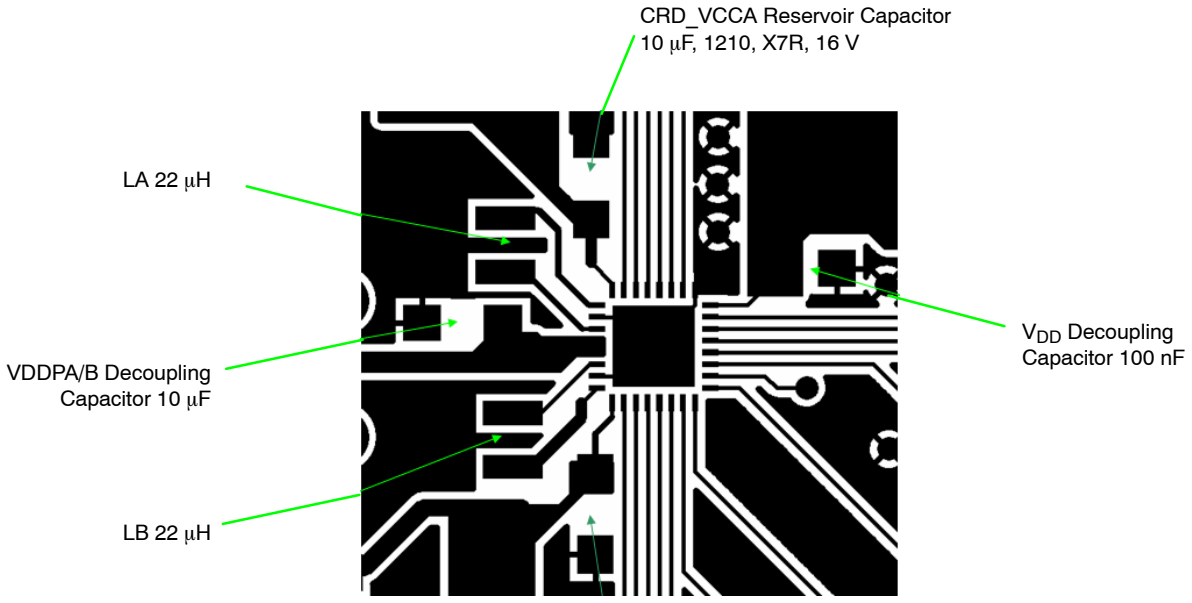
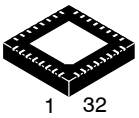


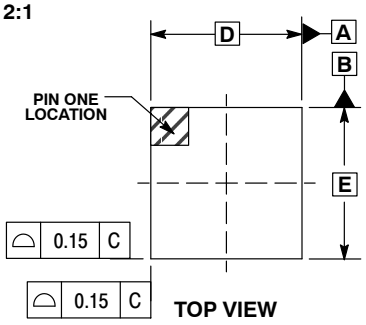
Figure 25. Example of PCB Device Implementation

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

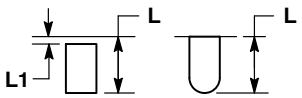
DATE 23 OCT 2013



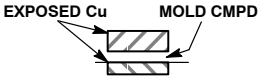
SCALE 2:1



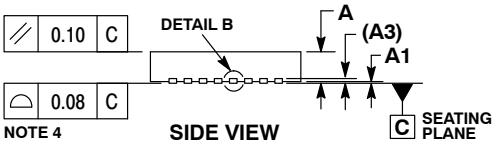
TOP VIEW



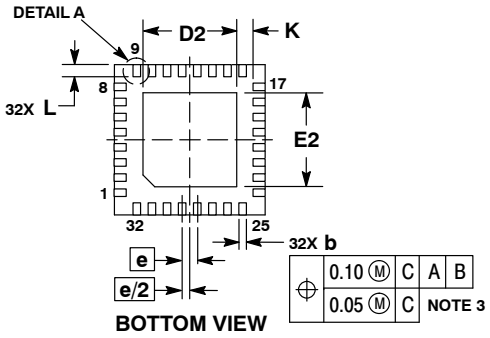
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

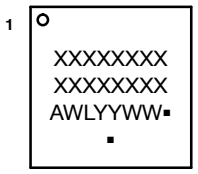


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

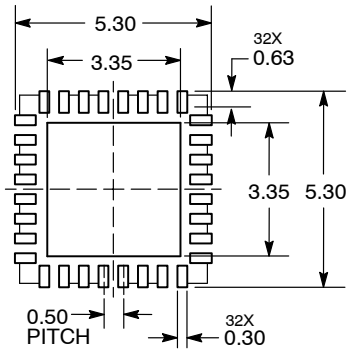


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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