# NCP1379

# Quasi-Resonant Current-Mode Controller for High-Power Universal Off-line Supplies

The NCP1379 hosts a high−performance circuitry aimed to powering quasi−resonant converters. Capitalizing on a proprietary valley−lockout system, the controller shifts gears and reduces the switching frequency as the power loading becomes lighter. This results in a stable operation despite switching events always occurring in the drain−source valley. This system works down to the 4th valley and toggles to a variable frequency mode beyond, ensuring an excellent standby power performance.

The controller includes an Over Power Protection circuit which clamps the delivered power at high−line. Safety−wise, a fixed internal timer relies on the feedback voltage to detect a fault. Once the timer elapses, the controller stops and enters auto−recovery mode, ensuring a low duty−cycle burst operation. To further improve the safety of the power supply, the NCP1379 features a pin to implement a combined brown−out/overvoltage protection.

Particularly well suited for TVs power supply applications, the controller features a low startup voltage allowing the use of an auxiliary power supply to power the device.

### Features

- Quasi−Resonant Peak Current−Mode Control Operation
- Valley Switching Operation with Valley−Lockout for Noise−Immune Operation
- Frequency Foldback at Light Load to Improve the Light Load Efficiency
- Adjustable Over Power Protection
- Auto−Recovery Output Short−Circuit Protection
- Fixed Internal 80 ms Timer for Short−Circuit Protection
- Combined Overvoltage Protection and Brown−out
- +500 mA / −800 mA Peak Current Source/Sink Capability
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- Low $V_{CC(on)}$ Allowing to Use a Standby Power Supply to Power the Device
- Extremely Low No−Load Standby Power
- SO8 Package
- These Devices are Pb−Free and are RoHS Compliant

### Typical Applications

- High Power ac−dc Converters for TVs, Set−Top Boxes etc.
- Offline Adapters for Notebooks

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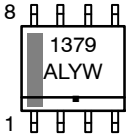
**QUASI−RESONANT PWM CONTROLLER FOR HIGH POWER AC−DC WALL ADAPTERS**

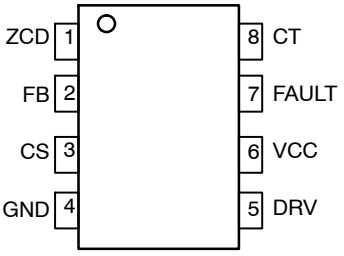
**MARKING DIAGRAMS**

**SOIC−8**
**D SUFFIX**
**CASE 751**




| | |
|---|---|
| 1379 | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

**PIN CONNECTIONS**




**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

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## TYPICAL APPLICATION EXAMPLE

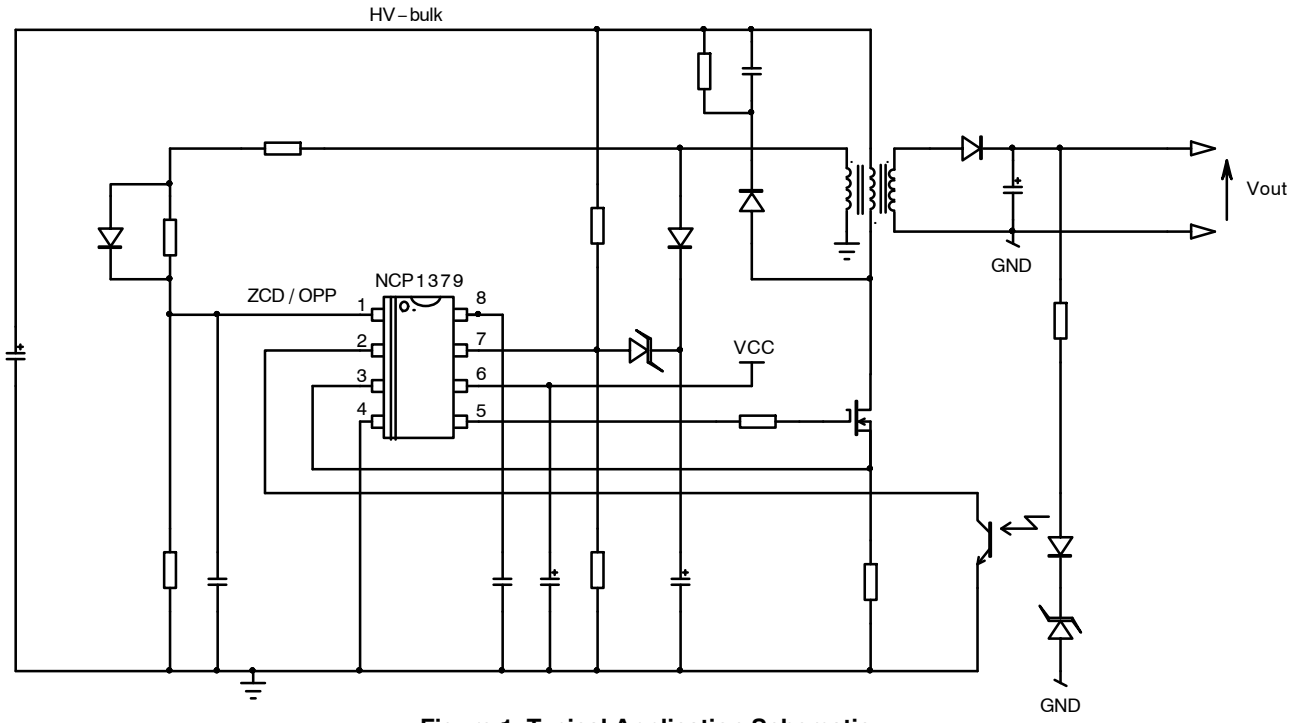



**Figure 1. Typical Application Schematic**

### PIN FUNCTION DESCRIPTION

| Pin N° | Pin Name | Function | Pin Description |
|---|---|---|---|
| 1 | ZCD | Zero Crossing Detection<br>Adjust the over power protection | Connected to the auxiliary winding, this pin detects the core reset event.<br>Also, injecting a negative voltage smaller than 0.3 V on this pin will perform over power protection. |
| 2 | FB | Feedback pin | Hooking an optocoupler collector to this pin will allow regulation. |
| 3 | CS | Current sense | This pin monitors the primary peak. |
| 4 | GND | − | The controller ground |
| 5 | DRV | Driver output | The driver's output to an external MOSFET |
| 6 | $V_{CC}$ | Supplies the controller | This pin is connected to an external auxiliary voltage. |
| 7 | Fault | Overvoltage protection<br>Brown−out | This pin observes the HV rail and protects the circuit in case of low main conditions. It also offers a way to latch the circuit in case of over voltage event. |
| 8 | $C_T$ | Timing capacitor | A capacitor connected to this pin acts as the timing capacitor in fold-back mode. |

## INTERNAL CIRCUIT ARCHITECTURE

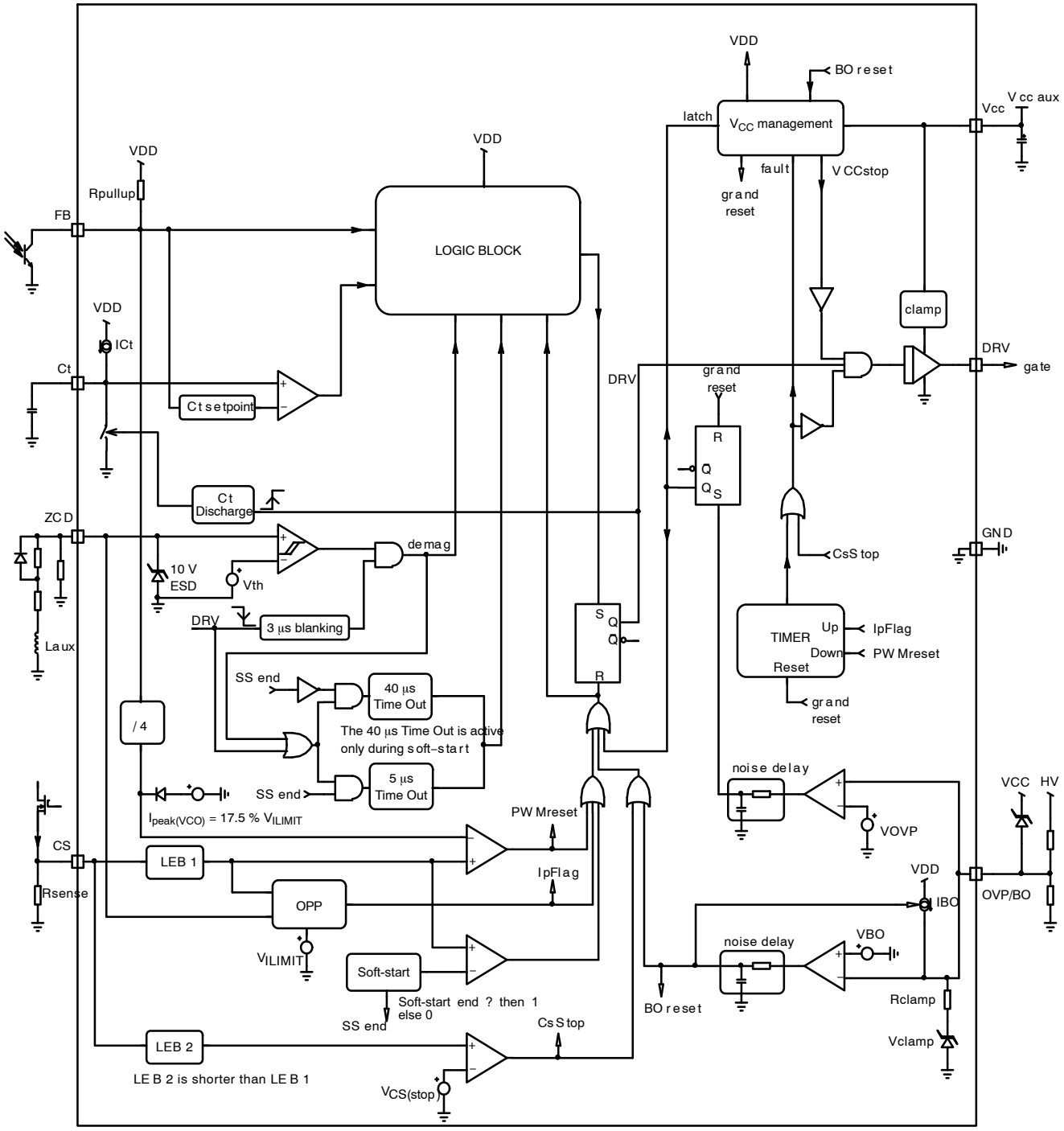



**Figure 2. Internal Circuit Architecture**

**MAXIMUM RATINGS TABLE(S)**

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CC(MAX)}$<br>$I_{CC(MAX)}$ | Maximum Power Supply voltage, VCC pin, continuous voltage<br>Maximum current for VCC pin | −0.3 to 28<br>±30 | V<br>mA |
| $V_{DRV(MAX)}$<br>$I_{DRV(MAX)}$ | Maximum driver pin voltage, DRV pin, continuous voltage<br>Maximum current for DRV pin | −0.3 to 20<br>±1000 | V<br>mA |
| $V_{MAX}$<br>$I_{MAX}$ | Maximum voltage on low power pins (except pins DRV and $V_{CC}$)<br>Current range for low power pins (except pins ZCD, DRV and $V_{CC}$) | −0.3 to 10<br>±10 | V<br>mA |
| $I_{ZCD(MAX)}$ | Maximum current for ZCD pin | +3 / −2 | mA |
| $R_{\theta JA}$ | Thermal Resistance Junction−to−Air | 120 | °C/W |
| $T_{J(MAX)}$ | Maximum Junction Temperature | 150 | °C |
| | Operating Temperature Range | −40 to +125 | °C |
| | Storage Temperature Range | −60 to +150 | °C |
| | ESD Capability, Human Body Model (HBM) model (Note 1) | 4 | kV |
| | ESD Capability, CDM model (Note 1) | 2 | kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per JEDEC Standard JESD22, Method A114E. Charged Device Model 2000 V per JEDEC Standard JESD22−C101D
2. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J$ = 25°C, $V_{CC}$ = 12 V, $V_{ZCD}$ = 0 V, $V_{FB}$ = 3 V, $V_{CS}$ = 0 V, $V_{fault}$ = 1.5 V, $C_T$ = 680 pF) For min/max values $T_J$ = −40°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 12 V)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY SECTION − STARTUP AND SUPPLY CIRCUITS** | | | | | | |
| | Supply Voltage | | | | | V |
| $V_{CC(on)}$ | Startup Threshold | $V_{CC}$ increasing | 10.5 | 11.4 | 12.3 | |
| $V_{CC(off)}$ | Minimum Operating Voltage | $V_{CC}$ decreasing | 8.3 | 9.0 | 9.4 | |
| $V_{CC(hyst)}$ | Hysteresis $V_{CC(on)}$ − $V_{CC(off)}$ | | 2.0 | 2.4 | − | |
| $V_{CC(reset)}$ | Internal logic reset | $V_{CC}$ decreasing | 6 | 7 | 8 | |
| $t_{VCC(off)}$ | $V_{CC(off)}$ noise filter | | − | 5 | − | μs |
| $t_{VCC(reset)}$ | $V_{CC(reset)}$ noise filter | | − | 20 | − | μs |
| $I_{CC(start)}$ | Startup current | FB pin open<br>$V_{CC}$ = $V_{CC(on)}$ − 0.5 V | − | 0.7 | 1.2 | mA |
| | Supply Current | | | | | mA |
| $I_{CC1}$ | Device Disabled/Fault (Note 3) | $V_{CC}$ > $V_{CC(off)}$ | − | 1.7 | 2.0 | |
| $I_{CC2}$ | Device Enabled/No output load on pin 5 | $F_{sw}$ = 10 kHz | − | 1.7 | 2.0 | |
| $I_{CC3A}$ | Device Switching ($F_{sw}$ = 65 kHz) | $C_{DRV}$ = 1 nF, $F_{sw}$ = 65 kHz | − | 2.65 | 3.00 | |
| $I_{CC3B}$ | Device Switching ($F_{sw}$ around 12 kHz) | $C_{DRV}$ = 1 nF, $V_{FB}$ = 1.25 V | − | 2.0 | − | |
| **CURRENT COMPARATOR − CURRENT SENSE** | | | | | | |
| $V_{ILIM}$ | Current Sense Voltage Threshold | $V_{FB}$ = 4 V, $V_{CS}$ increasing | 0.76 | 0.80 | 0.84 | V |
| $t_{LEB}$ | Leading Edge Blanking Duration for $V_{ILIM}$ | Minimum on time minus $t_{ILIM}$ | 210 | 275 | 330 | ns |
| $I_{bias}$ | Input Bias Current (Note 3) | DRV high | −2 | − | 2 | μA |
| $t_{ILIM}$ | Propagation Delay | $V_{CS}$ > $V_{ILIM}$ to DRV turn−off | − | 125 | 175 | ns |
| $I_{peak(VCO)}$ | Percentage of maximum peak current level at which VCO takes over (Note 4) | $V_{FB}$ = 0.4 V, $V_{CS}$ increasing | 15.4 | 17.5 | 19.6 | % |

3. Guaranteed by design
4. The peak current setpoint goes down as the load decreases. It is frozen below $I_{peak(VCO)}$ ($I_{peak}$ = cst)
5. If negative voltage in excess to −300 mV is applied to ZCD pin, the current setpoint decrease is no longer guaranteed to be linear
6. Minimum value for $T_J$ = 125°C

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J$ = 25°C, $V_{CC}$ = 12 V, $V_{ZCD}$ = 0 V, $V_{FB}$ = 3 V, $V_{CS}$ = 0 V, $V_{fault}$ = 1.5 V, $C_T$ = 680 pF) For min/max values $T_J$ = −40°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 12 V)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CURRENT COMPARATOR − CURRENT SENSE** | | | | | | |
| $V_{OPP(MAX)}$ | Setpoint decrease for $V_{ZCD}$ = −300 mV (Note 5) | $V_{ZCD}$ = −300 mV, $V_{FB}$ = 4 V, $V_{CS}$ increasing | 35.0 | 37.5 | 40.0 | % |
| $V_{CS(stop)}$ | Threshold for immediate fault protection activation | | 1.125 | 1.200 | 1.275 | V |
| $t_{BCS}$ | Leading Edge Blanking Duration for $V_{CS(stop)}$ | | − | 120 | − | ns |
| **DRIVE OUTPUT − GATE DRIVE** | | | | | | |
| $R_{SNK}$<br>$R_{SRC}$ | Drive Resistance<br>DRV Sink<br>DRV Source | <br>$V_{DRV}$ = 10 V<br>$V_{DRV}$ = 2 V | <br>−<br>− | <br>12.5<br>20 | <br>−<br>− | Ω |
| $I_{SNK}$<br>$I_{SRC}$ | Drive current capability<br>DRV Sink<br>DRV Source | <br>$V_{DRV}$ = 10 V<br>$V_{DRV}$ = 2 V | <br>−<br>− | <br>800<br>500 | <br>−<br>− | mA |
| $t_r$ | Rise Time (10 % to 90 %) | $C_{DRV}$ = 1 nF, $V_{DRV}$ from 0 to 12 V | − | 40 | 75 | ns |
| $t_f$ | Fall Time (90 % to 10 %) | $C_{DRV}$ = 1 nF, $V_{DRV}$ from 0 to 12 V | − | 25 | 60 | ns |
| $V_{DRV(low)}$ | DRV Low Voltage | $V_{CC}$ = $V_{CC(off)}$ + 0.2 V<br>$C_{DRV}$ = 1 nF, $R_{DRV}$=33 kΩ | 8.4 | 9.1 | − | V |
| $V_{DRV(high)}$ | DRV High Voltage (Note 6) | $V_{CC}$ = $V_{CC(MAX)}$<br>$C_{DRV}$ = 1 nF | 10.5 | 13.0 | 15.5 | V |
| **DEMAGNETIZATION INPUT − ZERO VOLTAGE DETECTION CIRCUIT** | | | | | | |
| $V_{ZCD(TH)}$ | ZCD threshold voltage | $V_{ZCD}$ decreasing | 35 | 55 | 90 | mV |
| $V_{ZCD(HYS)}$ | ZCD hysteresis | $V_{ZCD}$ increasing | 15 | 35 | 55 | mV |
| $V_{CH}$<br>$V_{CL}$ | Input clamp voltage<br>High state<br>Low state | <br>$I_{pin1}$ = 3.0 mA<br>$I_{pin1}$ = −2.0 mA | <br>8<br>−0.9 | <br>10<br>−0.7 | <br>12<br>−0.3 | V |
| $t_{DEM}$ | Propagation Delay | $V_{ZCD}$ decreasing from 4 V to −0.3 V | − | 150 | 250 | ns |
| $C_{PAR}$ | Internal input capacitance | | − | 10 | − | pF |
| $t_{BLANK}$ | Blanking delay after on−time | | 2.30 | 3.15 | 4.00 | μs |
| $t_{outSS}$<br>$t_{out}$ | Timeout after last demag transition | During soft−start<br>After the end of soft−start | 28<br>5.0 | 41<br>5.9 | 54<br>6.7 | μs |
| $R_{ZCD(pdown)}$ | Pulldown resistor (Note 3) | | 140 | 320 | 700 | kΩ |
| **TIMING CAPACITOR − TIMING CAPACITOR** | | | | | | |
| $V_{CT(MAX)}$ | Maximum voltage on $C_T$ pin | $V_{FB}$ < $V_{FB(TH)}$ | 5.15 | 5.40 | 5.65 | V |
| $I_{CT}$ | Source current | $V_{CT}$ = 0 V | 18 | 20 | 22 | μA |
| $V_{CT(MIN)}$ | Minimum voltage on $C_T$ pin, discharge switch activated | | − | − | 90 | mV |
| $C_T$ | Recommended timing capacitor value | | | 220 | | pF |
| **FEEDBACK SECTION − FEEDBACK** | | | | | | |
| $R_{FB(pullup)}$ | Internal pullup resistor | | 15 | 18 | 22 | kΩ |
| $I_{ratio}$ | Pin FB to current setpoint division ratio | | 3.8 | 4.0 | 4.2 | |
| $V_{FB(TH)}$ | FB pin threshold under which $C_T$ is clamped to $V_{CT(MAX)}$ | | 0.26 | 0.30 | 0.34 | V |

3. Guaranteed by design
4. The peak current setpoint goes down as the load decreases. It is frozen below $I_{peak(VCO)}$ ($I_{peak}$ = cst)
5. If negative voltage in excess to −300 mV is applied to ZCD pin, the current setpoint decrease is no longer guaranteed to be linear
6. Minimum value for $T_J$ = 125°C

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J$ = 25°C, $V_{CC}$ = 12 V, $V_{ZCD}$ = 0 V, $V_{FB}$ = 3 V, $V_{CS}$ = 0 V, $V_{fault}$ = 1.5 V, $C_T$ = 680 pF) For min/max values $T_J$ = −40°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 12 V)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FEEDBACK SECTION − FEEDBACK** | | | | | | |
| | Valley threshold | | | | | V |
| $V_{H2D}$ | FB voltage where 1st valley ends and 2nd valley starts | $V_{FB}$ decreases | 1.316 | 1.4 | 1.484 | |
| $V_{H3D}$ | FB voltage where 2nd valley ends and 3rd valley starts | $V_{FB}$ decreases | 1.128 | 1.2 | 1.272 | |
| $V_{H4D}$ | FB voltage where 3rd valley ends and 4th valley starts | $V_{FB}$ decreases | 0.846 | 0.9 | 0.954 | |
| $V_{HVCOD}$ | FB voltage where 4th valley ends and VCO starts | $V_{FB}$ decreases | 0.732 | 0.8 | 0.828 | |
| $V_{HVCOI}$ | FB voltage where VCO ends and 4th valley starts | $V_{FB}$ increases | 1.316 | 1.4 | 1.484 | |
| $V_{H4I}$ | FB voltage where 4th valley ends and 3rd valley starts | $V_{FB}$ increases | 1.504 | 1.6 | 1.696 | |
| $V_{H3I}$ | FB voltage where 3rd valley ends and 2nd valley starts | $V_{FB}$ increases | 1.692 | 1.8 | 1.908 | |
| $V_{H2I}$ | FB voltage where 2nd valley ends and 1st valley starts | $V_{FB}$ increases | 1.880 | 2.0 | 2.120 | |
| **PROTECTIONS − FAULT PROTECTION** | | | | | | |
| $T_{SHDN}$ | Thermal Shutdown | Device switching ($F_{SW}$ around 65 kHz) | 140 | − | 170 | °C |
| $T_{SHDN(HYS)}$ | Thermal Shutdown Hysteresis | | − | 40 | − | °C |
| $t_{OVLD}$ | Overload Timer | $V_{FB}$ = 4 V, $V_{CS}$ > $V_{ILIM}$ | 75 | 85 | 95 | ms |
| $t_{OVLD(off)}$ | OFF phase in auto−recovery fault mode | | 1.0 | 1.2 | 1.4 | s |
| $t_{SSTART}$ | Soft−start duration | $V_{FB}$ = 4 V, $V_{CS}$ ramping up, measured from 1st DRV pulse to $V_{CS(peak)}$ = 90% of $V_{ILIM}$ | 2.8 | 3.8 | 4.8 | ms |
| $V_{BO}$ | Brown−Out level | $V_{Fault}$ decreasing | 0.744 | 0.800 | 0.856 | V |
| $I_{BO}$ | Sourced hysteresis current $V_{Fault}$ > $V_{BO}$ | $V_{Fault}$ = $V_{BO}$ + 0.2 V | 9 | 10 | 11 | μA |
| $t_{BO(delay)}$ | Delay before entering and exiting Brown−out | | 22.5 | 30.0 | 37.5 | μs |
| $V_{OVP}$ | Internal Fault detection level for OVP | $V_{Fault}$ increasing | 2.35 | 2.5 | 2.65 | V |
| $t_{latch(delay)}$ | Delay before latch confirmation (OVP) | | 22.5 | 30 | 37.5 | μs |
| $V_{Fault(clamp)}$ | Clamped voltage (Fault pin left open) | Fault pin open | 1.0 | 1.2 | 1.4 | V |
| $R_{Fault(clamp)}$ | Clamping resistor (Note 3) | | 1.30 | 1.55 | 1.80 | kΩ |

3. Guaranteed by design
4. The peak current setpoint goes down as the load decreases. It is frozen below $I_{peak(VCO)}$ ($I_{peak}$ = cst)
5. If negative voltage in excess to −300 mV is applied to ZCD pin, the current setpoint decrease is no longer guaranteed to be linear
6. Minimum value for $T_J$ = 125°C

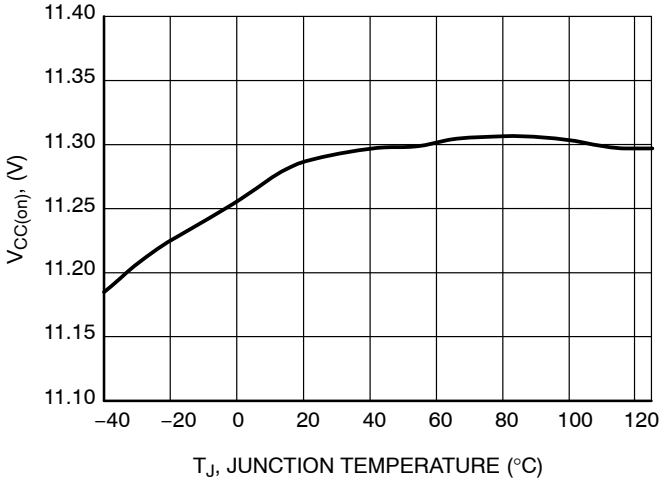



**Figure 3. $V_{CC(on)}$ vs. Junction Temperature**

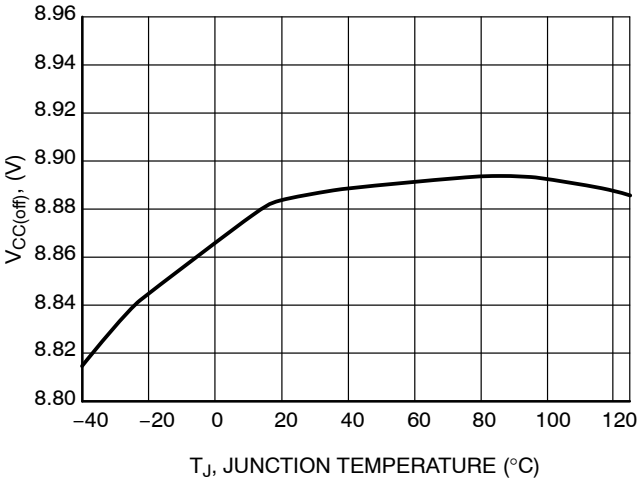



**Figure 4. $V_{CC(off)}$ vs. Junction Temperature**

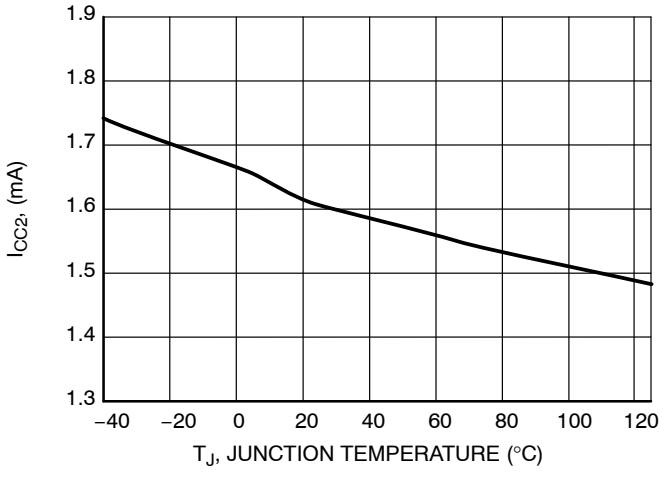



**Figure 5. $I_{CC2}$ vs. Junction Temperature**

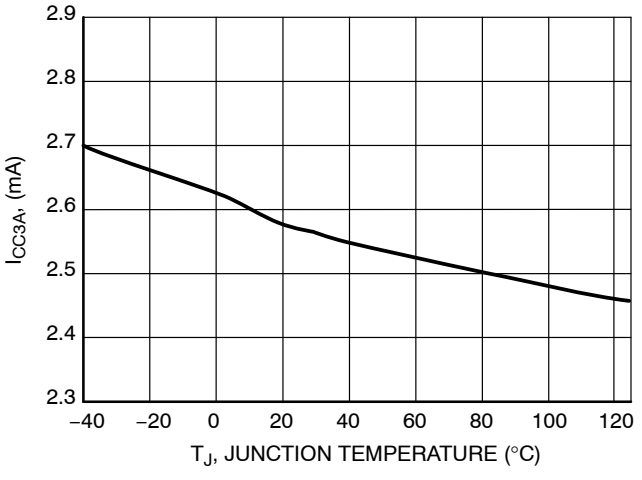



**Figure 6. $I_{CC3A}$ vs. Junction Temperature**

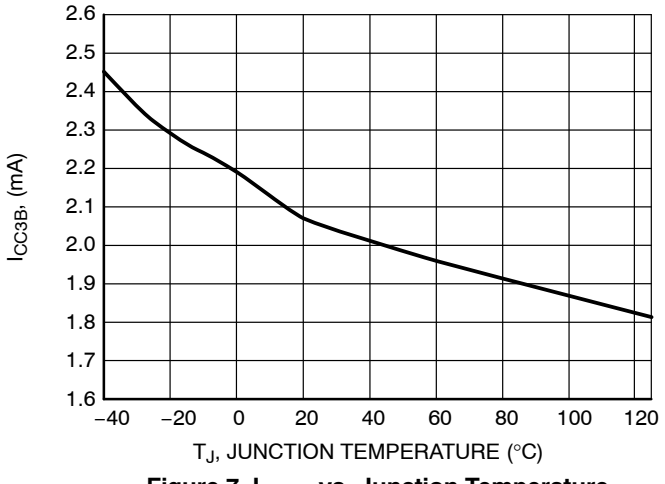



**Figure 7. $I_{CC3B}$ vs. Junction Temperature**

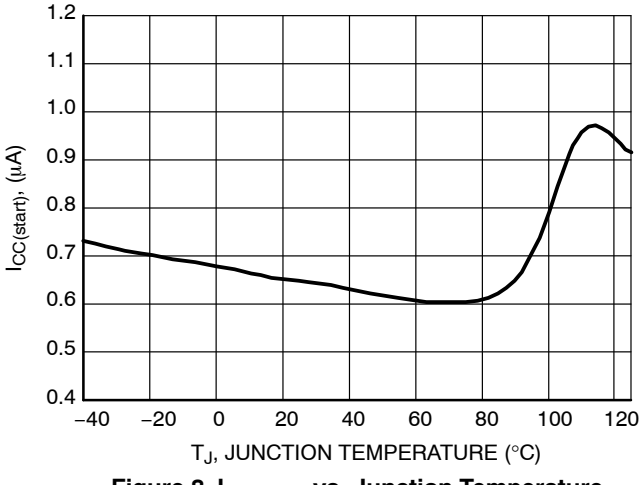



**Figure 8. $I_{CC(start)}$ vs. Junction Temperature**

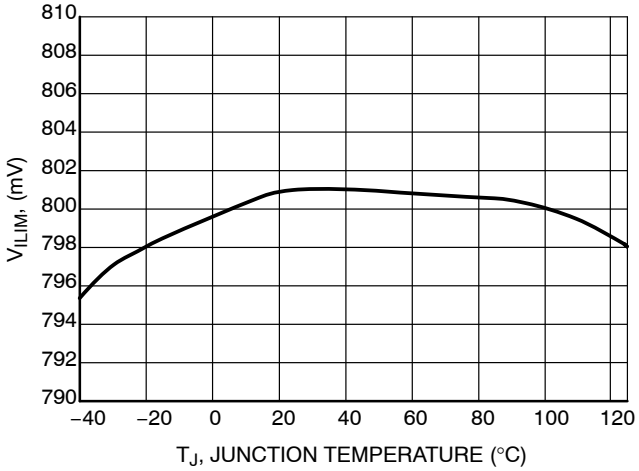



**Figure 9. $V_{ILIM}$ vs. Junction Temperature**

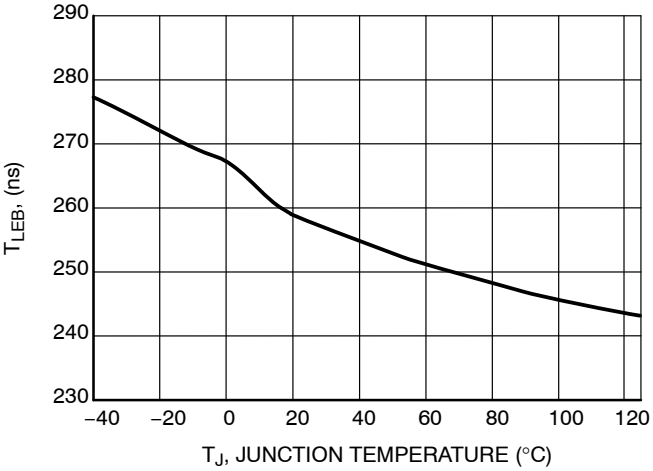



**Figure 10. $T_{LEB}$ vs. Junction Temperature**

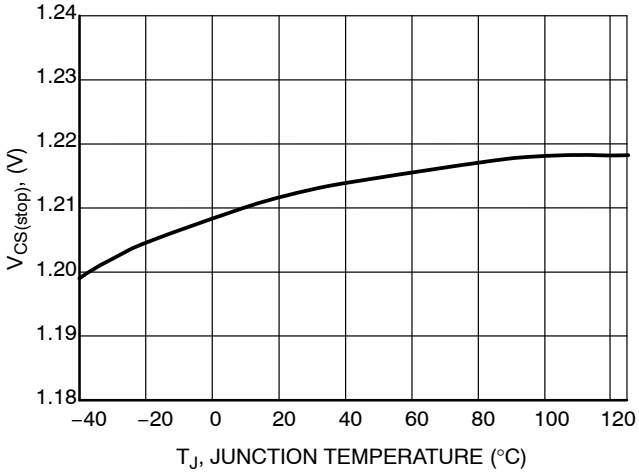



**Figure 11. $V_{CS(stop)}$ vs. Junction Temperature**

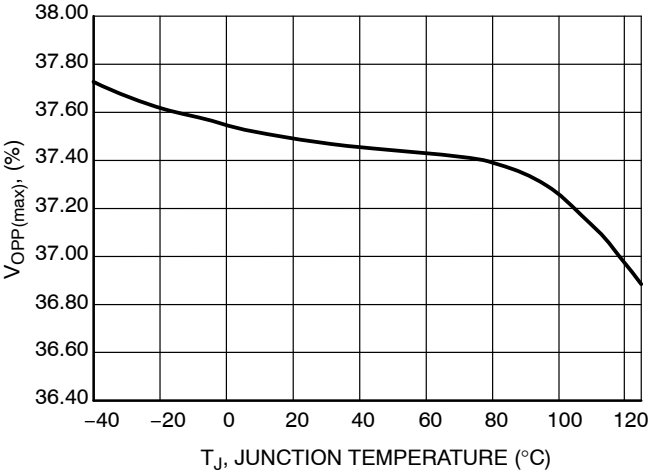



**Figure 12. $V_{OPP(MAX)}$ vs. Junction Temperature**

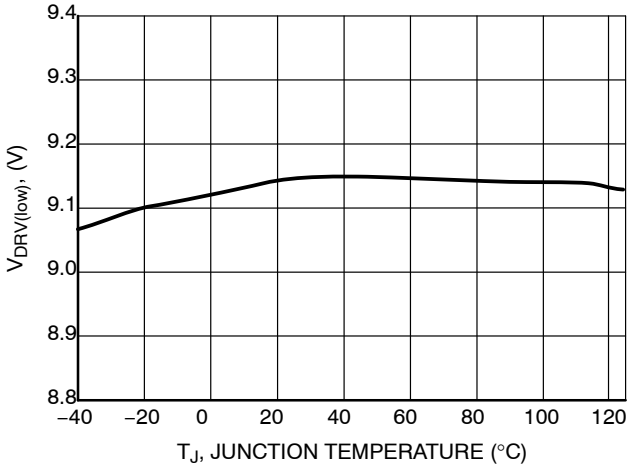



**Figure 13. $V_{DRV(low)}$ vs. Junction Temperature**

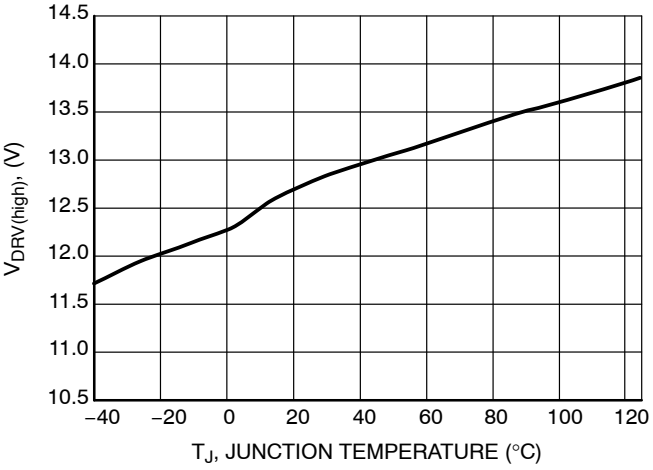



**Figure 14. $V_{DRV(high)}$ vs. Junction Temperature**

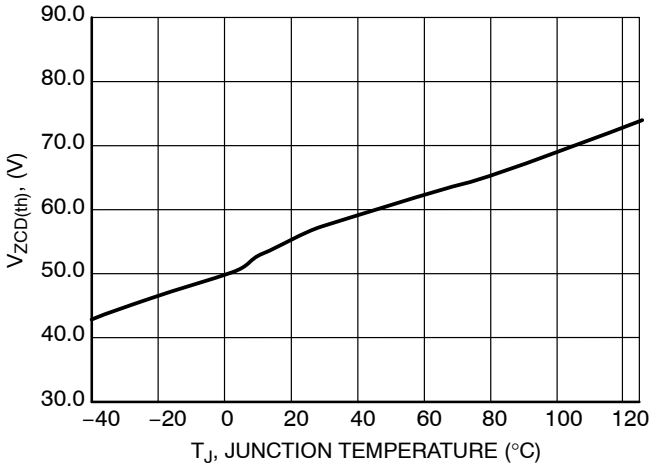



**Figure 15. $V_{ZCD(th)}$ vs. Junction Temperature**

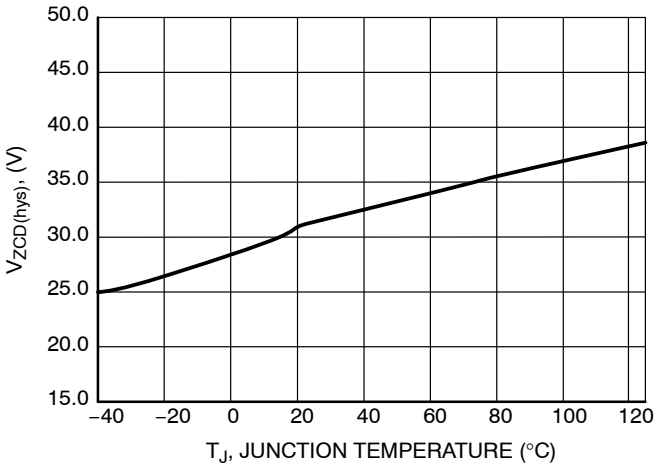



**Figure 16. $V_{ZCD(hys)}$ vs. Junction Temperature**

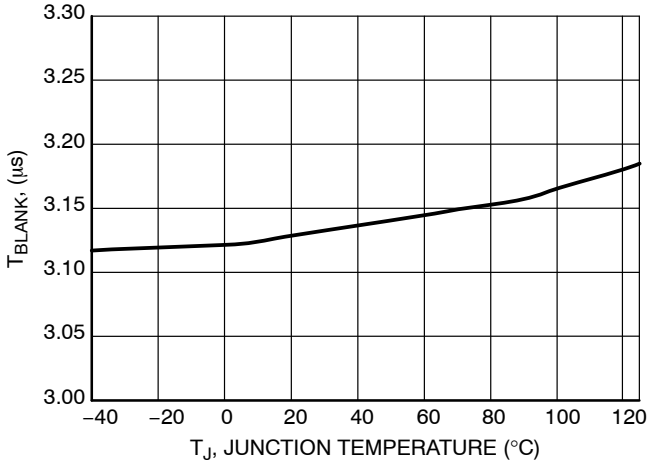



**Figure 17. $T_{BLANK}$ vs. Junction Temperature**

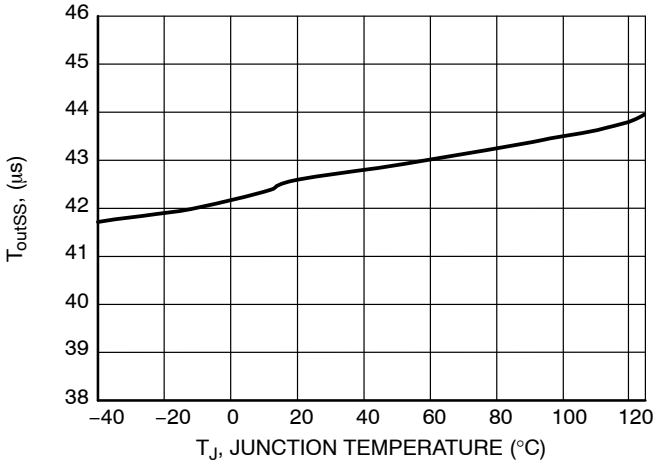



**Figure 18. $T_{outSS}$ vs. Junction Temperature**

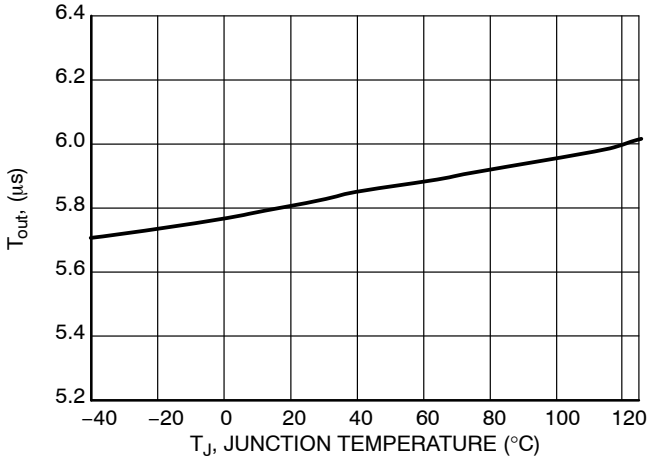



**Figure 19. $T_{out}$ vs. Junction Temperature**

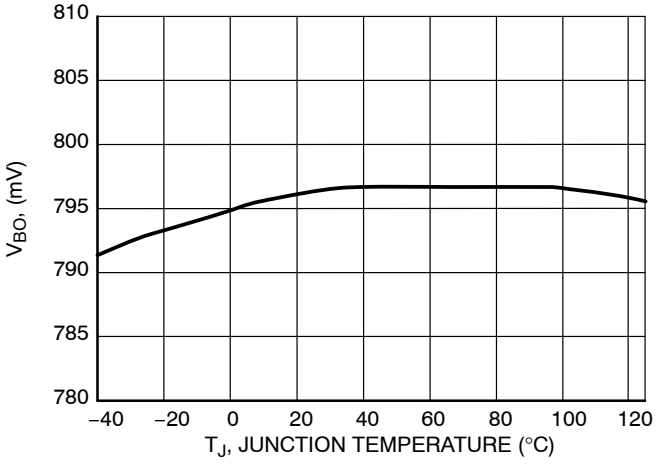



**Figure 20. $V_{BO}$ vs. Junction Temperature**

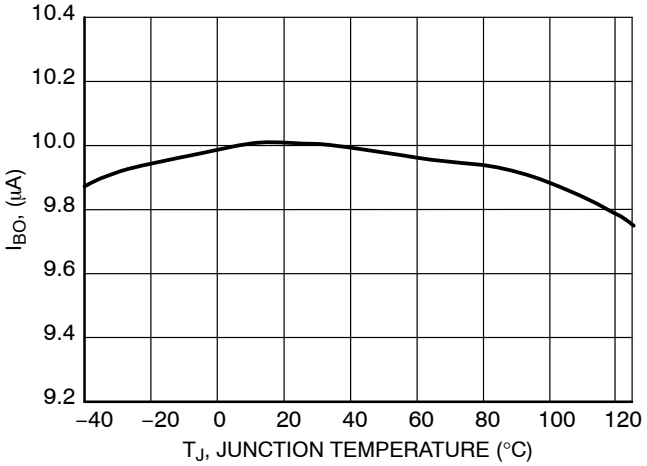



**Figure 21. $I_{BO}$ vs. Junction Temperature**

## APPLICATION INFORMATION

NCP1379 implements a standard current−mode architecture operating in quasi−resonant mode. Thanks to a proprietary circuitry, the controller prevents valley−jumping instability and steadily locks out in selected valley as the power demand goes down. Once the fourth valley is reached, the controller continues to reduce the frequency further down, offering excellent efficiency over a wide operating range. Due to a fault timer combined to an OPP circuitry, the controller is able to efficiently limit the output power at high−line.

- Quasi−Resonance Current−mode operation: implementing quasi−resonance operation in peak current−mode control, the NCP1379 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Due to a proprietary circuitry, the controller locks−out in a selected valley and remains locked until the output loading significantly changes. This behavior is obtained by monitoring the feedback voltage. When the load becomes lighter, the feedback setpoint changes and the controller jumps into the next valley. It can go down to the $4^{th}$ valley if necessary. Beyond this point, the controller reduces its switching frequency by freezing the peak current setpoint. During quasi−resonance operation, in case of very damped valleys, a 5.9 μs timer adds the missing valleys.
- Frequency reduction in light−load conditions: when the $4^{th}$ valley is left, the controller reduces the switching frequency which naturally improves the standby power by a reduction of all switching losses.
- Overpower protection (OPP): When the voltage on ZCD pin swings in flyback polarity, a direct image of the input voltage is applied on ZCD pin. We can thus reduce the peak current depending of the ZCD pin voltage level during the on−time.
- Internal soft−start: a soft−start precludes the main power switch from being stressed upon start−up. Its duration is fixed and equal to 3.8 ms.
- Fault input: the NCP1379 and D versions include a brown−out circuit which safely stops the controller in case the input voltage is too low. Restart occurs via a complete startup sequence (latch reset and soft−start). During normal operation, the voltage on this pin is clamped to 1.2 V to give enough room for OVP detection. If the voltage on this pin increases above 2.5 V, the part latches−off.
- Short−circuit protection: short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (where the auxiliary winding level does not properly collapse in presence of an output short). Here, when the internal 0.8 V maximum peak current limit is activated, the timer starts counting up. If the fault disappears, the timer counts down. If the timer reaches completion while the error flag is still present, the controller stops the pulses and goes into auto−recovery mode.

## NCP1379 OPERATING MODES

NCP1379 has two operating mode: quasi−resonant operation and VCO operation for the frequency foldback.

The operating mode is fixed by the FB voltage as portrayed by Figure 22:

- Quasi−resonant operation occurs for FB voltage higher than 0.8 V (FB decreasing) or higher than 1.4 V (FB increasing) which correspond to high output power and medium output power. The peak current is variable and is set by the FB voltage divided by 4.
- Frequency foldback or VCO mode occurs for FB voltage lower than 0.8 V (FB decreasing) or lower than 1.4 V (FB increasing). This corresponds to low output power.
- During VCO mode, the peak current decreases down to 17.5% of its maximum value and is then frozen. The switching frequency is variable and decreases as the output load decreases.
- The switching frequency is set by the end of charge of the capacitor connected to the $C_T$ pin. This capacitor is charged with a constant current source and the capacitor voltage is compared to an internal threshold fixed by FB voltage. When this capacitor voltage reaches the threshold the capacitor is rapidly discharged down to 0 V and a new period start.

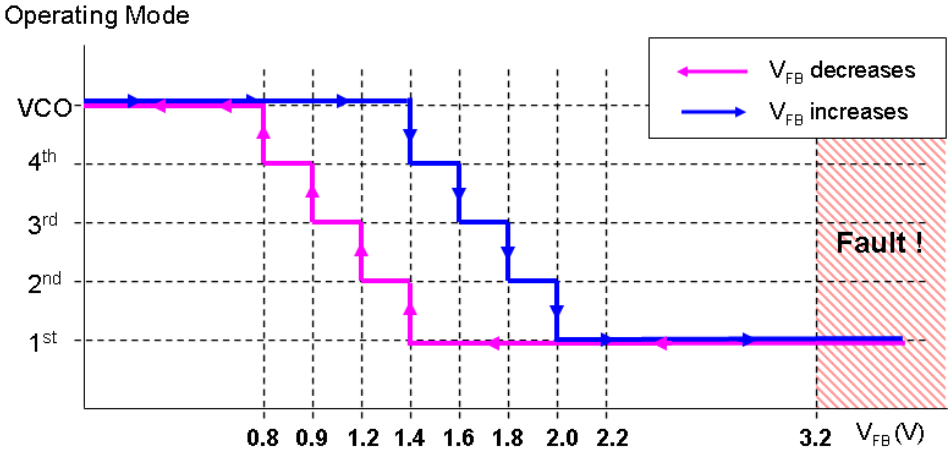



**Figure 22. Operating Valley According to FB Voltage**

## VALLEY DETECTION AND SELECTION

The valley detection is done by monitoring the voltage of the auxiliary winding of the transformer. A valley is detected when the voltage on pin 1 crosses down the 55 mV internal threshold. When a valley is detected, an internal counter is incremented. The operating valley (1st, 2nd, 3rd or 4th) is determined by the FB voltage as shown by Figure 22.

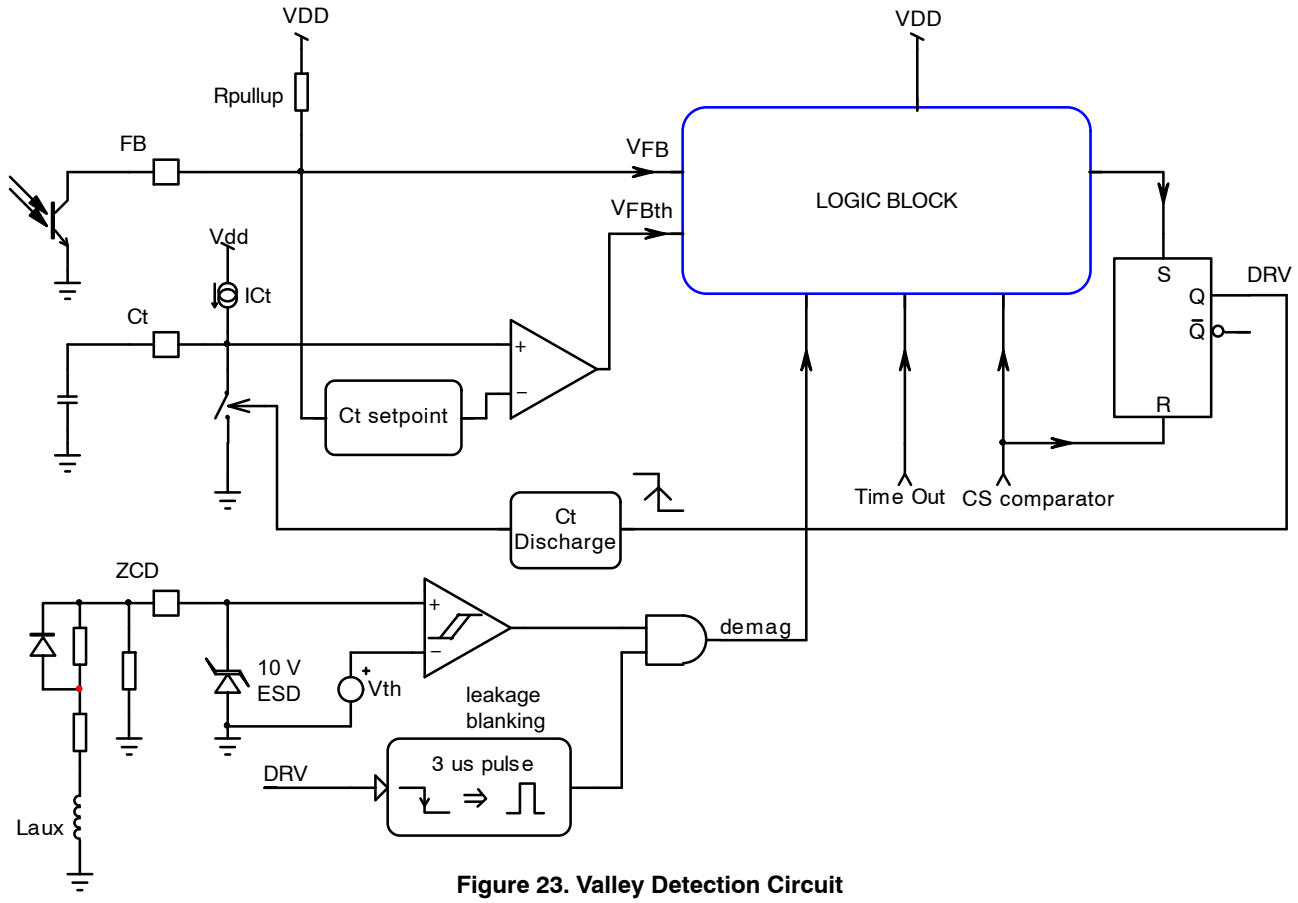



**Figure 23. Valley Detection Circuit**

As the output load decreases (FB voltage decreases the valleys are incremented from the first to the fourth. When the fourth valley is reached, if FB voltage further decreases below 0.8 V, the controller enters VCO mode.

During VCO operation, the peak current continues to decrease until it reaches 17.5% of the maximum peak current: the switching frequency expands to deliver the necessary output power. This allows achieving very low standby power consumption.

The Figure 24 shows a simulation case where the output current of a 19 V / 60 W decreases from 2.8 A to 0.1 A. No instability is seen during the valley transitions (Figures 25, 26, 27 and 28)

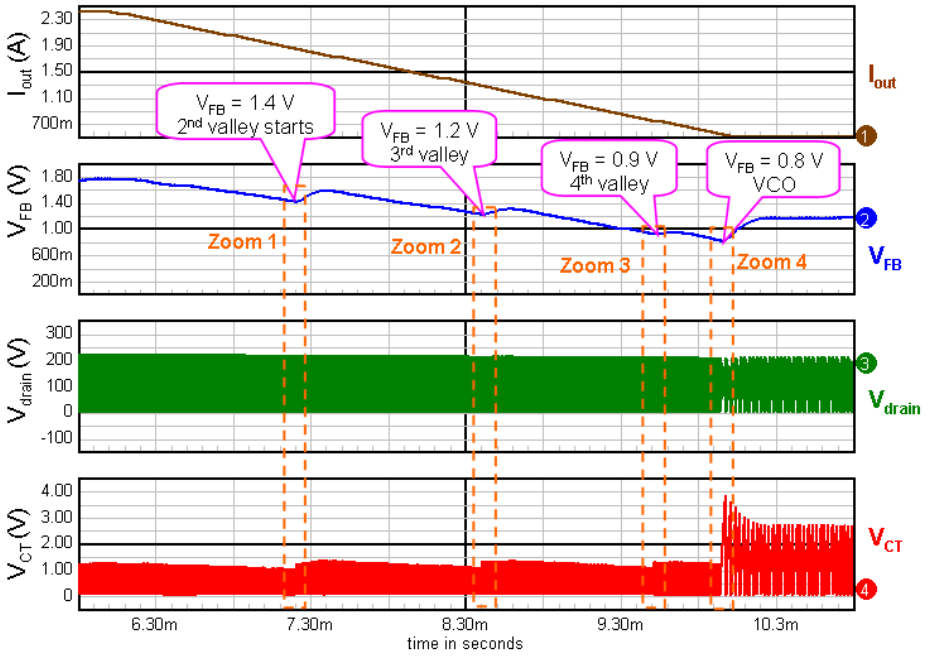



**Figure 24. Output Load is Decreased from 2.4 A to 0.5 A at 120 Vdc Input Voltage**

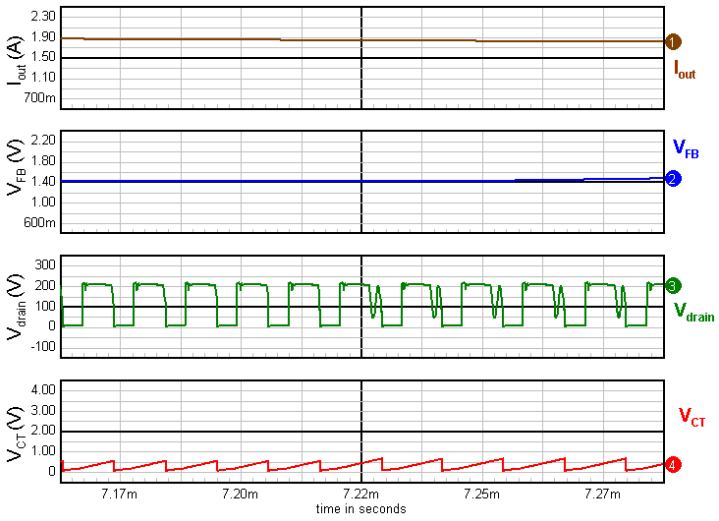



**Figure 25. Zoom 1: 1st to 2nd Valley Transition**

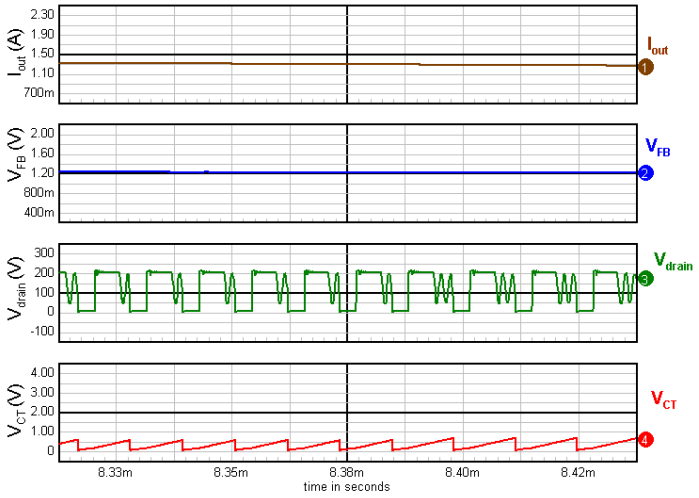



**Figure 26. Zoom 2: 2nd to 3rd Valley Transition**

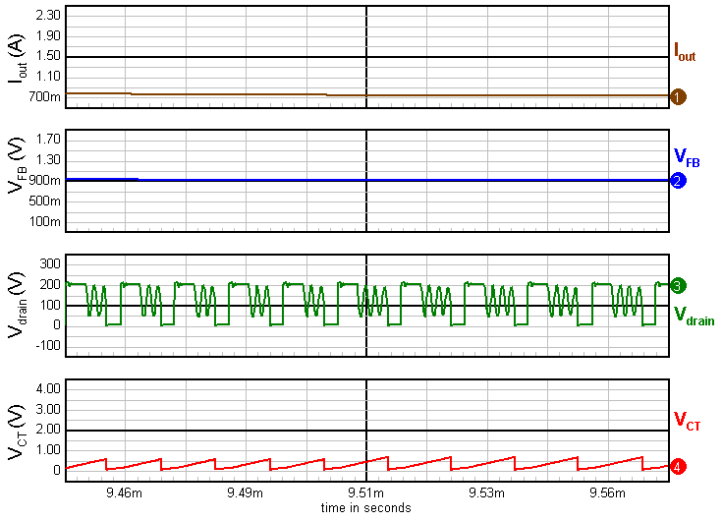



**Figure 27. Zoom 3: 3rd to 4th Valley Transition**

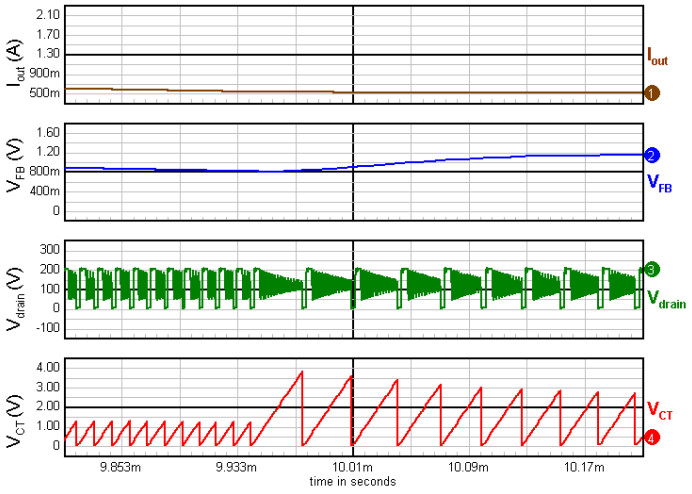



**Figure 28. Zoom 4: 4th Valley to VCO Mode Transition**

### Time Out

In case of extremely damped free oscillations, the ZCD comparator can be unable to detect the valleys. To avoid such situation, NCP1379 integrates a Time Out function that acts as a substitute clock for the decimal counter inside the logic bloc. The controller thus continues its normal operation. To avoid having a too big step in frequency, the time out duration is set to 5.9 μs. Figures 30 and 31 detail the time out operation.

The NCP1379 also features an extended time out during the soft−start.

Indeed, at startup, the output voltage reflected on the auxiliary winding is low. Because of the voltage drop introduced by the Over Power Compensation diode (Figure 35), the voltage on the ZCD pin is very low and the ZCD comparator might be unable to detect the valleys. In this condition, setting the DRV Latch with the 5.9 μs time−out leads to a continuous conduction mode operation (CCM) at the beginning of the soft−start. This CCM operation only last a few cycles until the voltage on ZCD pin becomes high enough to be detected by the ZCD comparator.

To avoid this, the time−out duration is extended to 40 μs during the soft−start in order to ensure that the transformer is fully demagnetized before the MOSFET is turned−on.

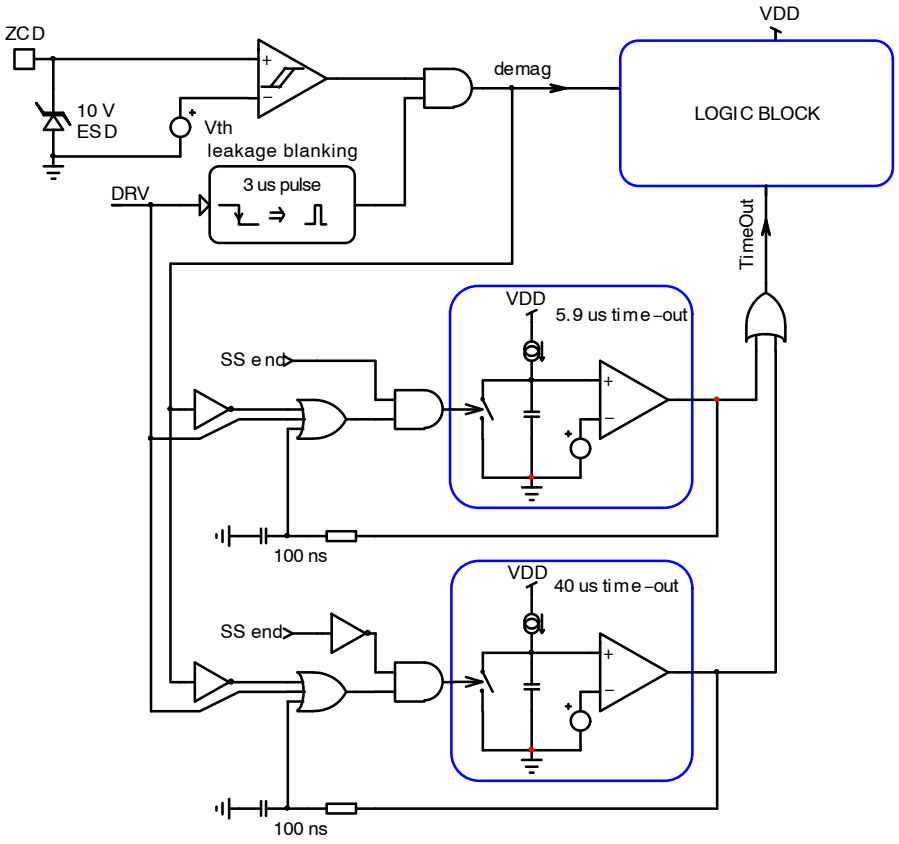



**Figure 29. Time Out Circuit**

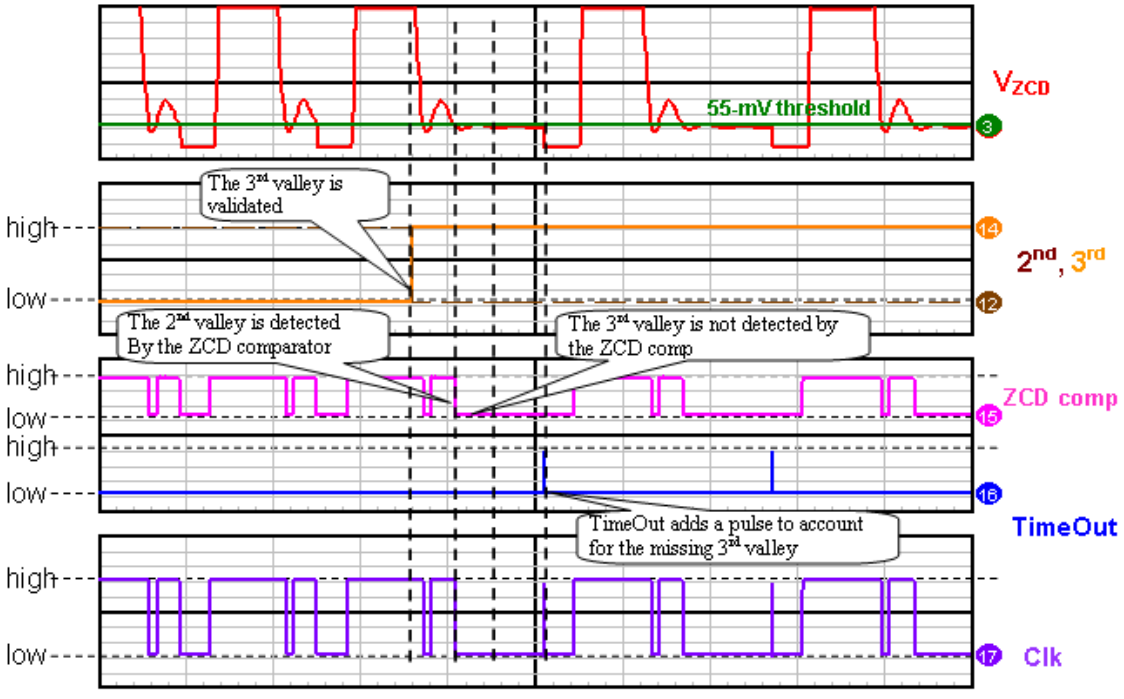



**Figure 30. Time Out Case n°1: the 3rd Valley is Missing**

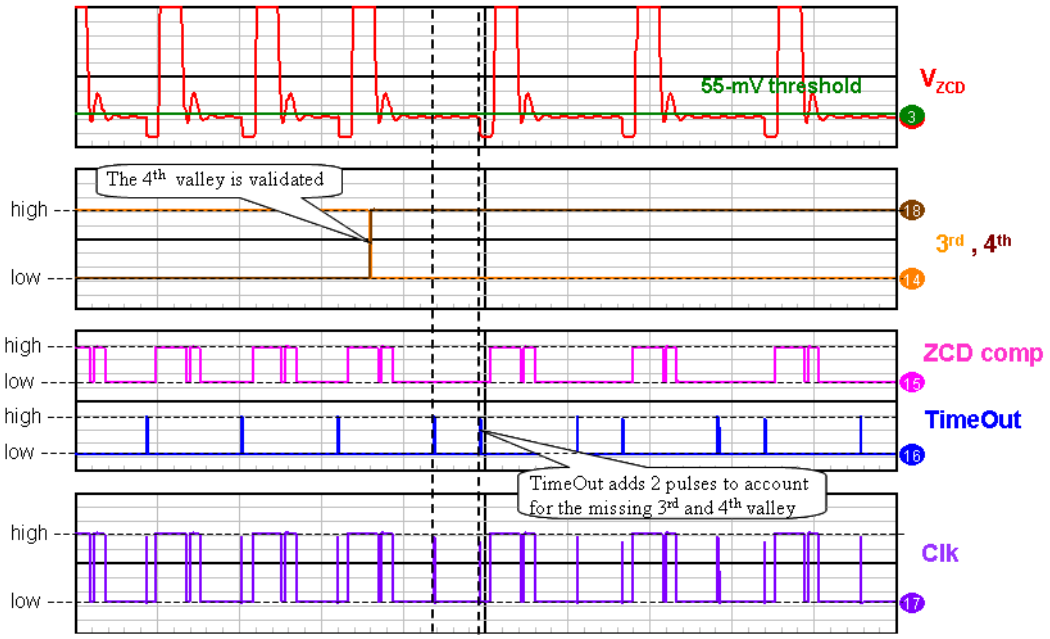



**Figure 31. Time Out Case n°2: the 3rd and 4th Valley are Missing**

## VCO MODE

VCO operation occurs for FB voltage lower than 0.8 V (FB decreasing), or lower than 1.4 V (FB increasing). This corresponds to low output power.

During VCO operation, the switching frequency is variable and expands as the output power decreases. The peak current is fixed to 17.5% of his maximum value when $V_{FB} < 0.56$ V.

The frequency is set by the end of charge of the capacitor connected to the $C_T$ pin. This capacitor is charged with a constant current source and its voltage is compared to an internal threshold ($V_{FBth}$) fixed by FB voltage (see Figure 23). When this capacitor voltage reaches the threshold, the capacitor is rapidly discharged down to 0 V and a new period start. The internal threshold is inversely proportional to FB voltage. The relationship between $V_{FB}$ and $V_{FBth}$ is given by Equation 1.

$$V_{FBth} = 6.5 - (10/3)V_{FB} \quad \text{(eq. 1)}$$

When $V_{FB}$ is lower than 0.3 V, $V_{CT}$ is clamped to $V_{CT(MAX)}$ which is typically 5.5 V. Figure 32 shows the VCO mode at works.

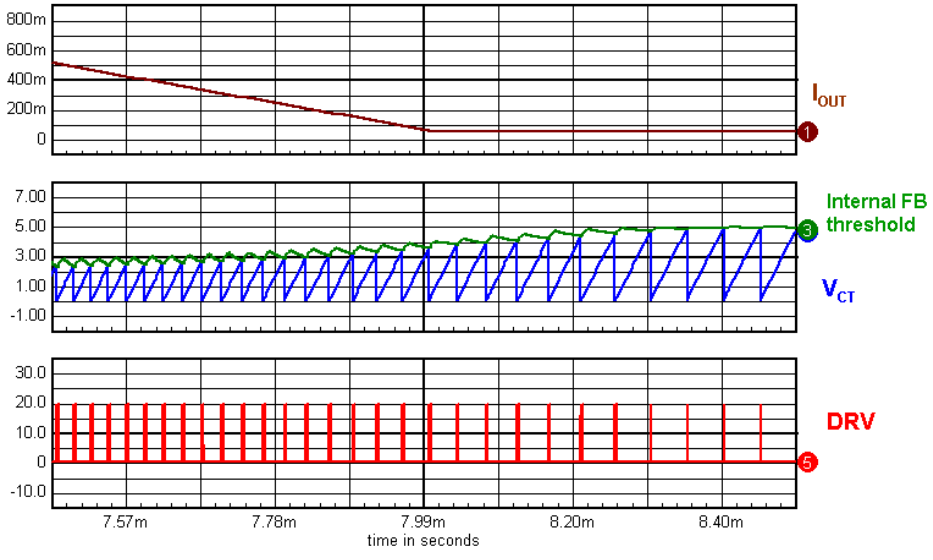



**Figure 32. In VCO Mode, as the Power Output Decreases the Frequency Expands**

## SHORT−CIRCUIT OR OVERLOAD MODE

Figure 33 shows the implementation of the fault timer.

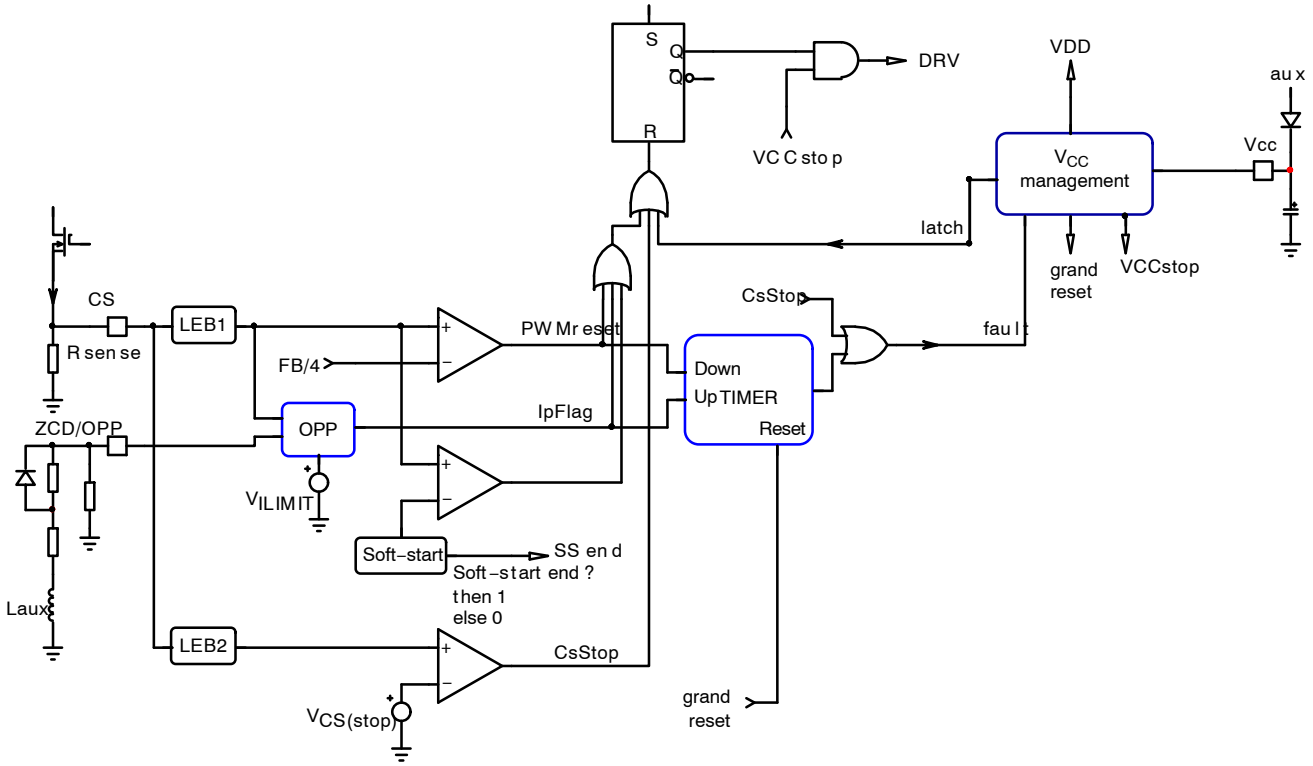



**Figure 33. Fault Detection Schematic**

When the current in the MOSFET is higher than $V_{ILIM}$ /$R_{sense}$, “Max Ip” comparator trips and the digital timer starts counting: the timer count is incremented each 10 ms. When the current comes back within safe limits, “Max Ip” comparator becomes silent and the timer count down: the timer count is decremented each 10 ms. In normal overload conditions the timer reaches its completion when it has counted up 8 times 10 ms.

When the timers reaches its completion, the circuit enter auto−recovery mode: the circuit stops all operations during 1.2 s typically and re−start. This ensures a low duty−cycle burst operation in fault mode (around 6.7%).

In parallel to the cycle−by−cycle sensing of the CS pin, another comparator with a reduced LEB ($t_{BCS}$) and a threshold of 1.2 V is able to sense winding short−circuit and immediately stop the controller. This additional protection is also auto−recovery.

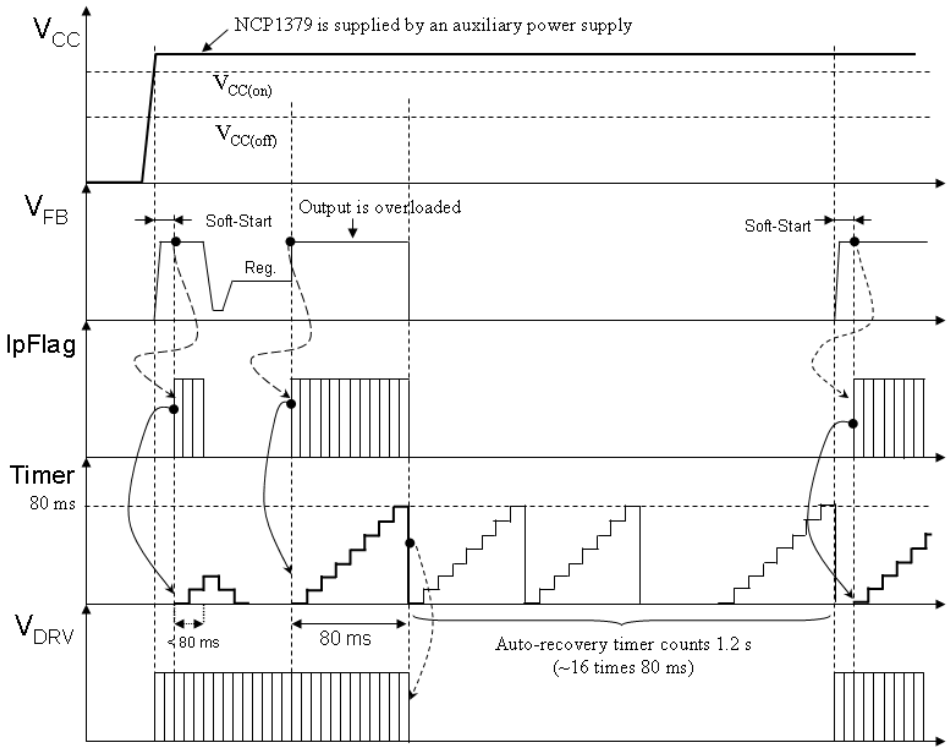



**Figure 34. Auto−Recovery Overload Protection Chronograms**

## OVER POWER COMPENSATION

The over power compensation is achieved by monitoring the signal on ZCD pin (pin 1). Indeed, a negative voltage applied on this pin directly affects the internal voltage reference setting the maximum peak current (Figure 35).

When the power MOSFET is turned−on, the auxiliary winding voltage becomes a negative voltage proportional to the input voltage. As the auxiliary winding is already connected to ZCD pin for the valley detection, by selecting the right values for $R_{opu}$ and $R_{opl}$, we can easily perform over power compensation.

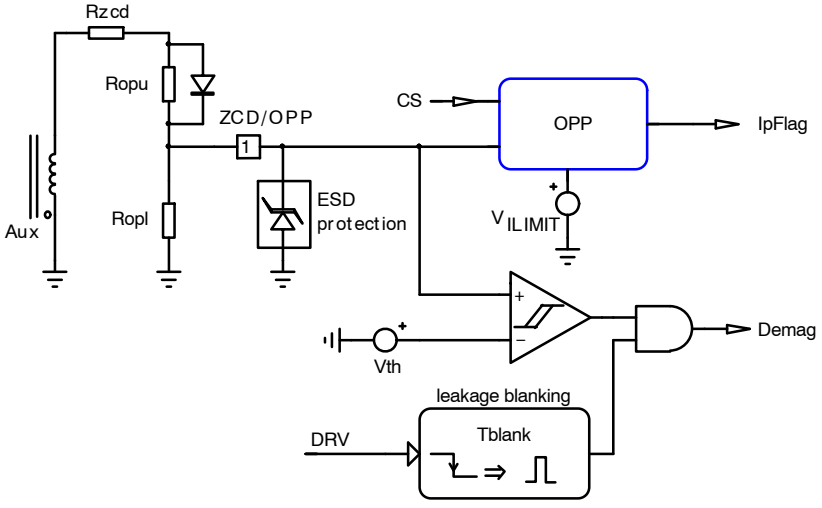



**Figure 35. Over Power Compensation Circuit**

To ensure optimal zero−crossing detection, a diode is needed to bypass $R_{opu}$ during the off−time.

If we apply the resistor divider law on pin 1 during the on−time, we obtain the following relationship:

$$\frac{R_{zcd} + R_{opu}}{R_{opl}} = -\frac{N_{p,aux}V_{IN} - V_{OPP}}{V_{OPP}} \quad \text{(eq. 2)}$$

Where:
$N_{p,aux}$ is the auxiliary to primary turn ration: $N_{p,aux} = N_{aux} / N_p$
$V_{IN}$ is the DC input voltage
$V_{OPP}$ is the negative OPP voltage

By selecting a value for $R_{opl}$, we can easily deduce $R_{opu}$ using Equation 2. While selecting the value for $R_{opl}$, we must be careful not choosing a too low value for this resistor in order to have enough voltage for zero−crossing detection during the off−time. We recommend having at least 8 V on ZCD pin, the maximum voltage being 10 V.

During the off−time, ZCD pin voltage can be expressed as follows:

$$V_{ZCD} = \frac{R_{opl}}{R_{ZCD} + Ropl}(V_{auz} - V_d) \quad \text{(eq. 3)}$$

We can thus deduce the relationship between $R_{opl}$ and $R_{zcd}$:

$$\frac{R_{ZCD}}{R_{opl}} = \frac{V_{aux} - V_d - V_{ZCD}}{V_{ZCD}} \quad \text{(eq. 4)}$$

Design example:

- $V_{aux}$ = 18 V
- $V_d$ = 0.6 V
- $N_{p,aux}$ = 0.18

If we want at least 8 V on ZCD pin, we have:

$$\frac{R_{ZCD}}{R_{opl}} = \frac{V_{aux} - V_d - V_{ZCD}}{V_{ZCD}} = \frac{18 - 0.6 - 8}{8} = 1.2 \quad \text{(eq. 5)}$$

We can choose: $R_{zcd}$ = 1 kΩ and $R_{opl}$ = 1 kΩ.

For the over power compensation, we need to decrease the peak current by 37.5% at high line (370 Vdc). The corresponding OPP voltage is:

$$V_{OPP} = 0.375 \times V_{ILIM} = -300\ mV \quad \text{(eq. 6)}$$

Using Equation 2, we have:

$$\frac{R_{ZCD} + R_{opu}}{R_{opl}} = -\frac{N_{p,aux}V_{IN} - V_{OPP}}{V_{OPP}} = \frac{-0.18 \times 370 - (-0.3)}{(-0.3)} = 221 \quad \text{(eq. 7)}$$

Thus,

$$R_{opu} = 221_{Ropl} - R_{ZCD} = 221 \times 1k - 1k = 220\ k\Omega \quad \text{(eq. 8)}$$

## OVERVOLTAGE PROTECTION / BROWN−OUT

NCP1379 combine brown−out and overvoltage detection on the pin Fault.

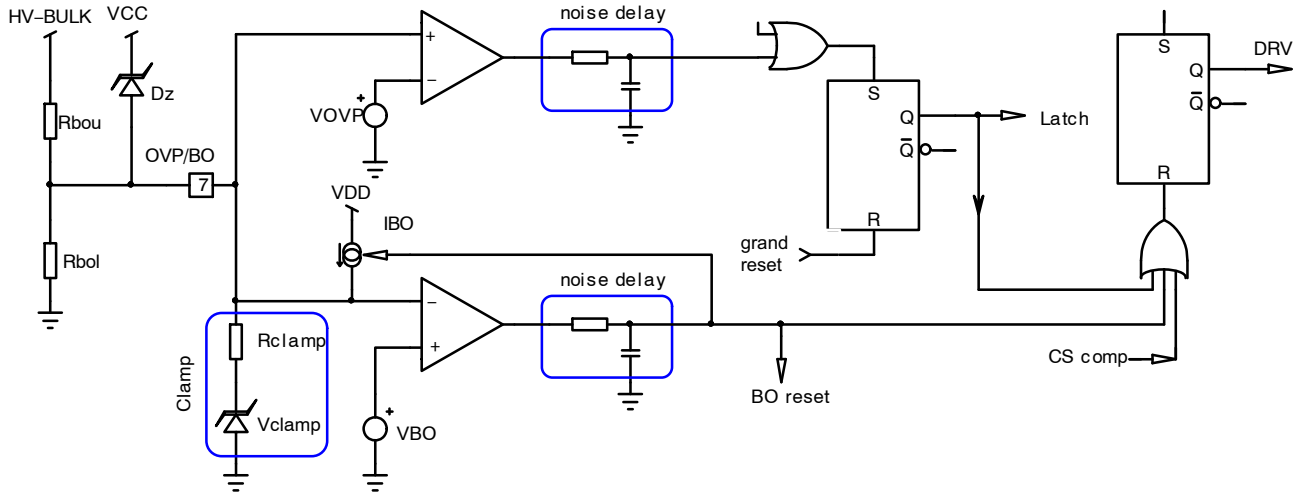



**Figure 36. Brown−out and Overvoltage Protection**

In order to protect the power supply against low input voltage condition, the pin 7 permanently monitors a fraction of the bulk voltage through a voltage divider. When this image of bulk voltage is below the $V_{BO}$ threshold, the controller stops switching. When the bulk voltage comes back within safe limits, the circuit restarts pulsing. The hysteresis for the brown−out function is implemented with a high side current source sinking 10 μA when the brown−out comparator is high ($V_{bulk} > V_{bulk(on)}$)

In order to avoid having a too high voltage on pin 7 if the bulk voltage is high, an internal clamp limits the voltage.

In case of over voltage, the zener diode will start to conduct and inject current inside the internal clamp resistor $R_{clamp}$ thus causing pin 7 voltage to increase. When this voltage reaches $V_{OVP}$, the controller latches−off and stays latched. The controller will be reset if $V_{CC}$ falls bellow $V_{CC(reset)}$ or if a brown−out occurs (Figure 37).

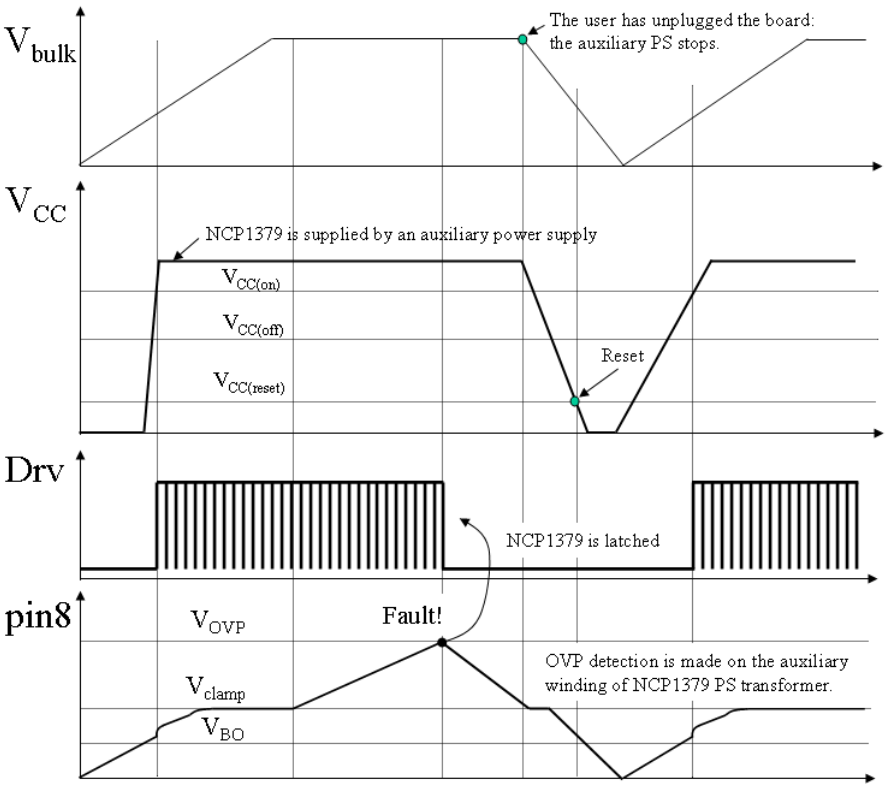



**Figure 37. Operating Chronograms in Case of Overvoltage with NCP1379 Supplied by an Auxiliary Power Supply**

The following equations show how to calculate the brown−out resistors.

First of all, select the bulk voltage value at which the controller must start switching ($V_{bulk(on)}$) and the bulk voltage for shutdown ($V_{bulk(off)}$). Then use the following equation to calculate $R_{bou}$ and $R_{bol}$.

$$R_{bol} = \frac{V_{BO}\left(V_{bulk(on)} - V_{bulk(off)}\right)}{I_{BO}\left(V_{bulk(on)} - V_{BO}\right)} \quad \text{(eq. 9)}$$

$$R_{bou} = \frac{R_{bol}\left(V_{bulk(on)} - V_{BO}\right)}{V_{BO}} \quad \text{(eq. 10)}$$

## DESIGN EXAMPLE

$V_{BO}$ = 0.8 V
$I_{BO}$ = 10 μA
We select: $V_{bulk(on)}$ = 120 V, $V_{bulk(off)}$ = 60 V

$$R_{bol} = \frac{V_{BO}\left(V_{bulk(on)} - V_{bulk(off)}\right)}{I_{BO}\left(V_{bulk(on)} - V_{BO}\right)} \quad \text{(eq. 11)}$$

$$= \frac{0.8(120 - 60)}{10x10^{-6}(120 - 0.8)} = 40.3\ k\Omega$$

$$R_{bou} = \frac{R_{bol}\left(V_{bulk(on)} - V_{BO}\right)}{V_{BO}} \quad \text{(eq. 12)}$$

$$= \frac{40.3x10^{3}(120 - 0.8)}{0.8} = 6\ M\Omega$$

### ORDERING INFORMATION

| Device | Package Type | Shipping† |
|---|---|---|
| NCP1379DR2G | SOIC−8 (Pb free) | 2500 / Tape & Reel |

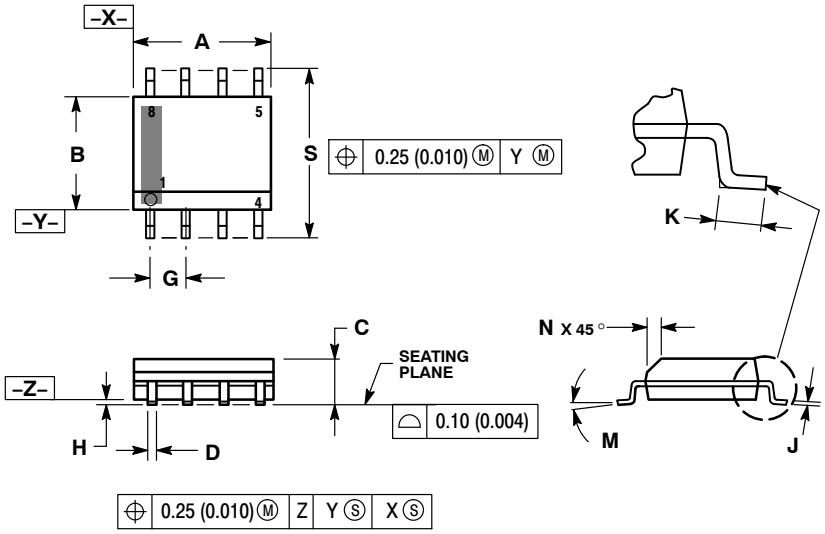
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The products described herein (NCP1379), may be covered by one or more of the following U.S. patents; 6,362,067 and 5,073,850. There may be other patents pending.

SCALE 1:1

**SOIC−8 NB**
CASE 751−07
ISSUE AK

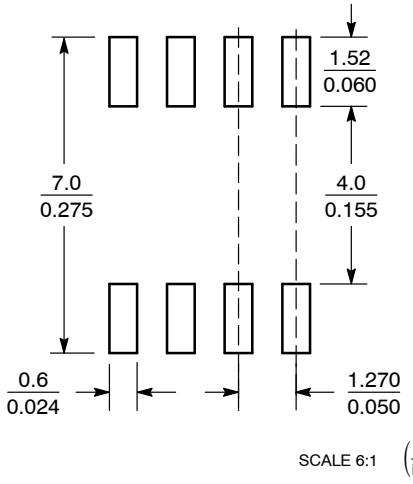
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

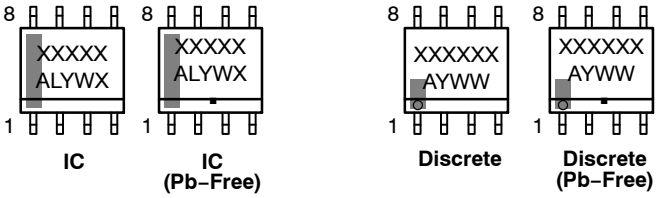
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
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**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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