CrM Totem Pole PFC IC

Totem Pole CrM Power Factor Correction Controller

NCP1680

The NCP1680 is a Critical Conduction Mode (CrM) Power Factor Correction (PFC) controller IC designed to drive the bridgeless totem pole PFC topology. The bridgeless totem pole PFC consists of two totem pole legs: a fast switching leg driven at the PWM switching frequency and a second leg that operates at the AC line frequency. This topology eliminates the diode bridge present at the input of a conventional PFC circuit, allowing significant improvement in efficiency and power density.

Features

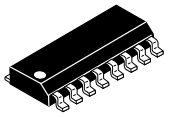
- Totem Pole PFC Topology Eliminates Input Diode Bridge Enabling Very High Efficiency & Compact Design
- AC Line Monitoring Circuit & AC Phase Detection
- Brownout Detection
- Critical Conduction Mode (CrM) Operation
- Discontinuous Conduction Mode (DCM) with Valley Turn On under Light Load Conditions
- Frequency Foldback in DCM with 25 kHz Minimum Frequency
- Digital Loop Compensation
- Simplified Valley Sensing
- Novel Current Limit Scheme Eliminates the Needs for Hall Effect Sensors
- Soft Skip Mode with a Skip Flag for Optimizing Light Load Performance
- Near Unity Power Factor in All Operating Modes
- PFCOK Indicator

Safety Features

- Soft and Fast Overvoltage Protection
- 2−Level Latch Input for OVP & OTP
- Bulk Undervoltage Protection
- Internal Thermal Shutdown
- Cycle−by−Cycle Current Limit

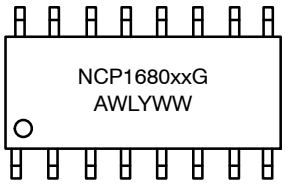
Applications

- 5 G/Telecom Power Supplies
- Industrial Power Supplies
- Gaming Console Power Supplies
- Ultra High Density (UHD) Power Supplies
- Merchant Power



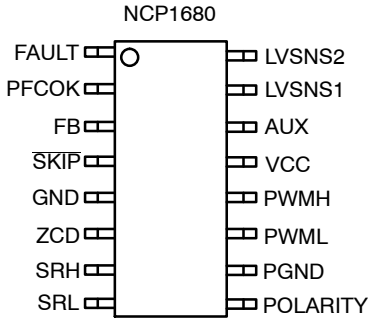
SOIC−16
CASE 751B−05

MARKING DIAGRAM



NCP1680	= Specific Device Code
xx	= AA, AB, or AC
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 36 of this data sheet.

DRAWING / PINOUT

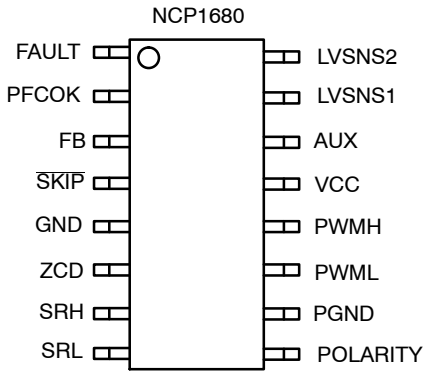


Figure 1. NCP1680 Controller Pinout

TYPICAL APPLICATION SCHEMATIC

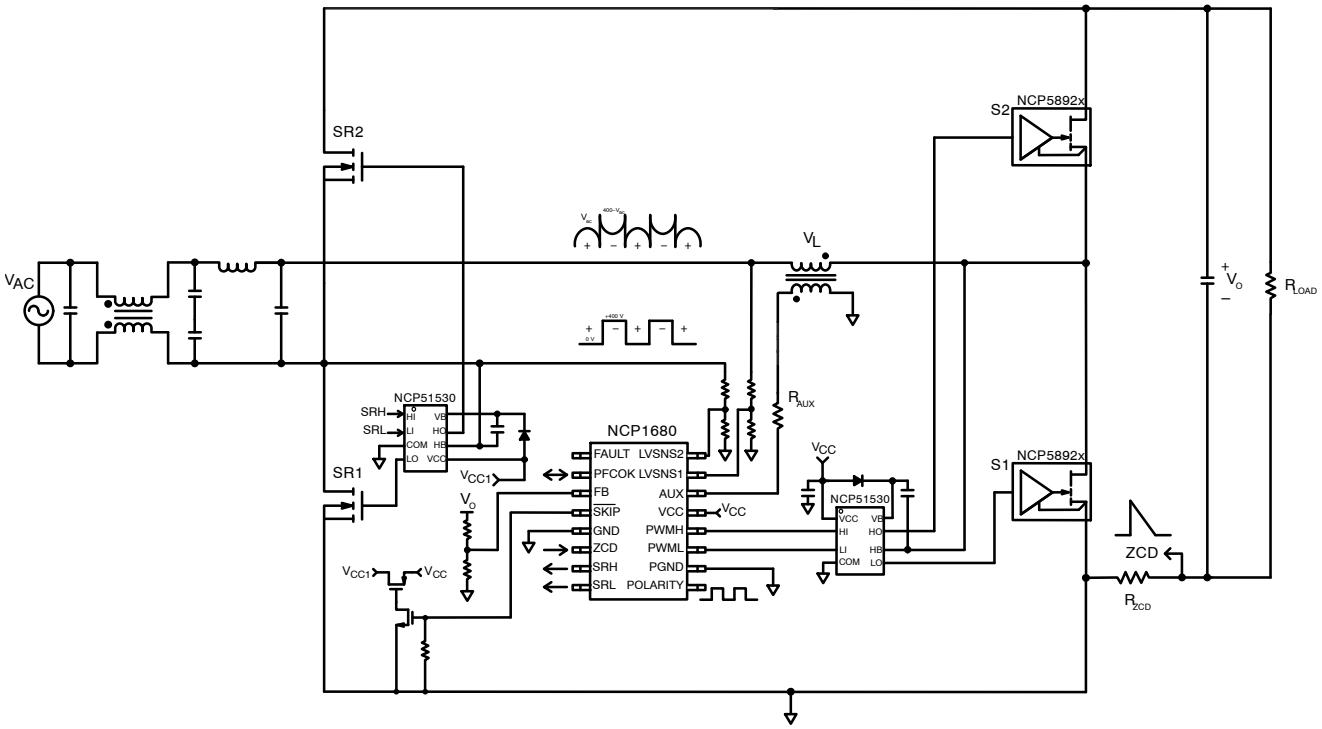


Figure 2. Typical Application Schematic

FUNCTIONAL BLOCK DIAGRAM

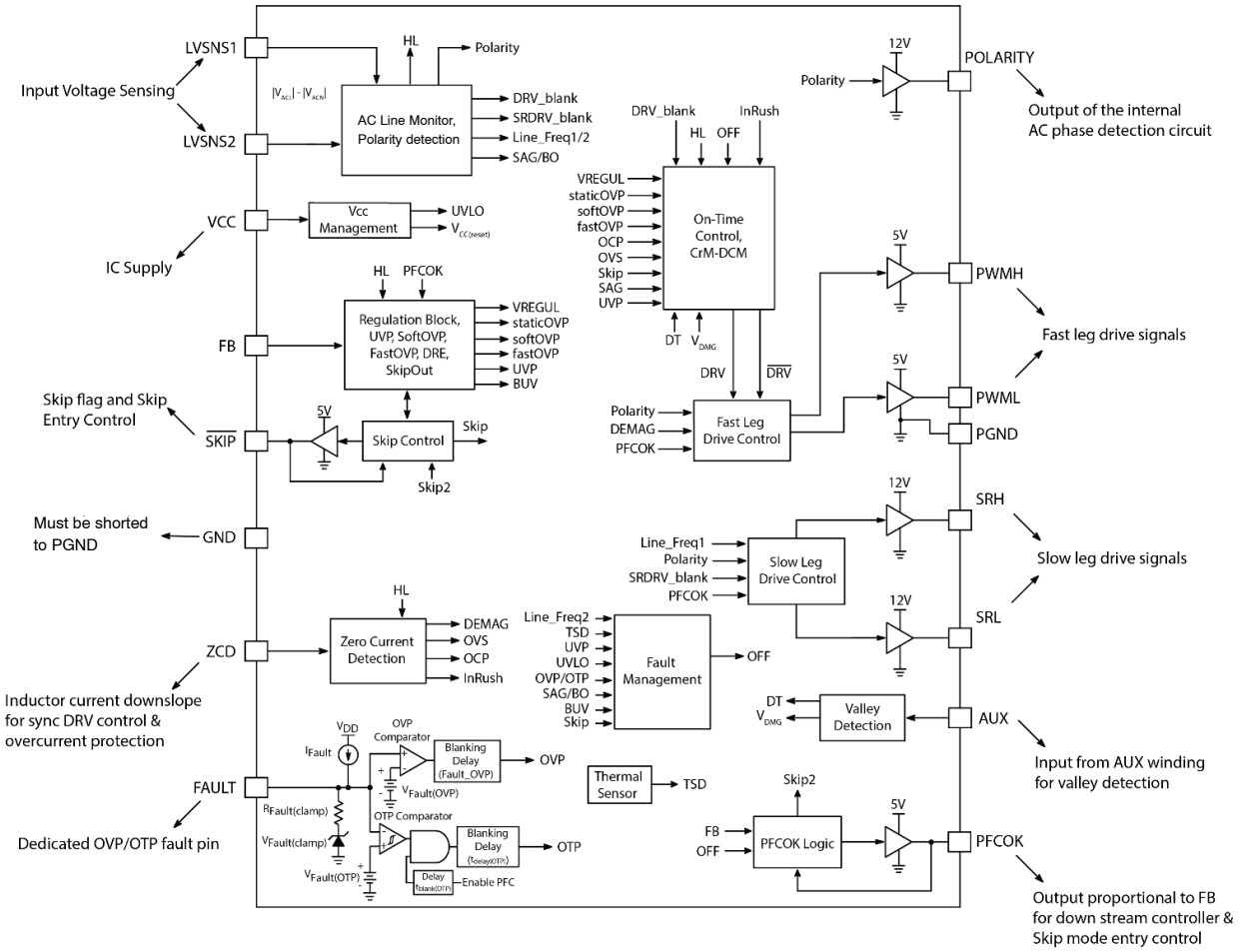


Figure 3. Block Diagram

PIN DESCRIPTION

Table 1. PIN DESCRIPTIONS

Pin Number	Pin Name	Function
1	FAULT	Combined OVP/OTP fault pin.
2	PFCOK	The PFCOK pin is held low when the PFC output voltage is out of regulation and during fault conditions. The pin becomes active when the PFC output achieves regulation in nominal operation, sourcing a current proportional to the feedback voltage, V_{FB}. The PFCOK pin is bidirectional; it can be used to enable a downstream converter and can be used by the downstream converter to force the NCP1680 into Soft Skip Mode operation.
3	FB	This pin senses the PFC output voltage for loop regulation.
4	$\overline{\text{Skip}}$	The $\overline{\text{Skip}}$ pin is a 5 V signal that goes high when the device enables PWML/H pulses. When the device enters Soft Skip Mode or is in Fault Mode, the pin will pull to GND. The $\overline{\text{Skip}}$ pin is bidirectional; it can be used to enable/disable peripheral circuitry, reducing I_{CC} consumption in Soft Skip Mode. The pin can also be used to force the NCP1680 into skip mode by externally grounding the pin for at least 56 μs.
5	GND	GND pin should be shorted to PGND.
6	ZCD	The pin senses the inductor current downslope. It is used to detect demagnetization and turn−off the (1−D) switch. Current limit is also based on the signal on this pin. Use of a low inductance current sensing resistor is recommended.
7	SRH	Control signal for high side slow leg device.

Table 1. PIN DESCRIPTIONS (continued)

Pin Number	Pin Name	Function
8	SRL	Control signal for low side slow leg device.
9	POLARITY	Output of the internal AC polarity detection circuit.
10	PGND	Power ground reference.
11	PWML	PWM logic level output for control of low side fast leg switch.
12	PWMH	PWM logic level output for control of high side fast leg switch.
13	VCC	IC supply pin.
14	AUX	The pin is used to monitor the switch node resonance on the auxiliary winding and enable valley turn−on during CrM and frequency foldback operation.
15	LVSNS1	Low voltage input for AC line voltage monitoring. LVSNS1 resistor divider should be connected to AC line side of the boost inductor.
16	LVSNS2	Low voltage input for AC line voltage monitoring. LVSNS2 resistor divider should be connected to the neutral of the AC line voltage.

Table 2. MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Supply Input Voltage, V_{CC} Pin	VCC	$V_{CC(MAX)}$	−0.3 to 30	V
PWML Pin Maximum Voltage	PWML	$V_{PWML(MAX)}$	−0.3 to 5.5	V
PWML Pin Maximum Current	PWML	$I_{PWML(SRC\_MAX)}$ $I_{PWML(SNK\_MAX)}$	−100 +160	mA
PWMH Pin Maximum Voltage	PWMH	$V_{PWMH(MAX)}$	−0.3 to 5.5	V
PWMH Pin Maximum Current	PWMH	$I_{PWMH(SRC\_MAX)}$ $I_{PWMH(SNK\_MAX)}$	−100 +160	mA
SRx, Polarity Pin Maximum Voltage	SRL, SRH, Polarity	$V_{SRx(MAX)}$	−0.3 to 14	V
SRx, Polarity Pin Maximum Current	SRL, SRH, Polarity	$I_{SRx(SRC\_MAX)}$ $I_{SRx(SNK\_MAX)}$	−100 +160	mA
AUX Pin Input Voltage	AUX	V_{AUX}	−0.3 to 5.5 (Note 1)	V
AUX Pin Input Current	AUX	I_{AUX}	−2 / +5	mA
ZCD Pin Input Voltage Range	ZCD	V_{ZCD}	−0.3 to 5.5 (Note 1)	V
ZCD Pin Maximum Current	ZCD	$I_{ZCD(MAX)}$	−2 / +5	mA
Maximum Input Voltage Other Pins	LVSNS1, LVSNS2, $\overline{Skip}$, FB, FAULT	V_{MAX}	−0.3 to 5.5 (Note 1)	V
Maximum Current Other Pins	LVSNS1, LVSNS2, $\overline{Skip}$, FB, FAULT	I_{MAX}	−2 to +5	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation at T_A = 70°C Thermal Resistance Junction−to−Air (1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad)		P_D $R_{\theta JA}$	550 145	mW °C/W
Maximum Junction Temperature		$T_{J(MAX)}$	150	°C
Operating Temperature Range			−40 to +125	°C
Storage Temperature Range			−60 to +150	°C

Table 2. MAXIMUM RATINGS (continued)

Rating	Pin	Symbol	Value	Unit
ESD Capability, HBM Model (Note 2)			3.5	kV
ESD Capability, CDM Model (Note 2)			1.25	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This level is low enough to guarantee not to exceed the internal ESD diode and 5.5 V ZENER diode. More positive and negative voltages can be applied if the pin current stays within the −2 mA / +5 mA range.
2. This device contains ESD protection and exceeds the following tests: Human Body Model 3500 V per JEDEC Standard JESD22−A114E, Charged Device Model 1250 V per JEDEC Standard JESD22−C101E.
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 3. ELECTRICAL CHARACTERISTICS
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START−UP & SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	9.75	10.5	11.25	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.2	8.8	9.4	
V_{CC} Hysteresis ($V_{CC(on)}$ − $V_{CC(off)}$)	V_{CC} decreasing	$V_{CC(HYS)}$	1.2	1.7	–	
Internal Latch / Logic Reset Level	V_{CC} decreasing	$V_{CC(reset)}$	2.5	4	6	
Supply Voltage						mA
Before Startup	V_{CC} = 9.5 V	I_{CC1}	–	1.8	2.2	
Fault or Latch	V_{FLT} = 0 V	I_{CC2}	–	1.8	2.2	
Operational, Switching at 100 kHz	All DRVs Open	I_{CC3}	–	3.3	4	
Operational, Skipping	V_{PFCOK} = 0 V	I_{CC4}	–	0.54	0.9	
AC ZERO CROSSING MANAGEMENT						
Recommended External Divider Ratio		K_{L_DIV}	–	100	–	
Main PWM Drive Control						
PWM Zero Crossing Blanking Thresholds						mV
Threshold to Stop PWML/H Pulses	V_{ZCB_STOP} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V	$V_{ZCB\_STOP1(LL)}$ $V_{ZCB\_STOP2(LL)}$		100		
Threshold to Start PWML/H Pulses	V_{ZCB_START} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Increasing, V_{LVSNS2} = 0 V V_{LVSNS1} Decreasing, V_{LVSNS2} = 4 V	$V_{ZCB\_START1(LL)}$ $V_{ZCB\_START2(LL)}$		$V_{ZCB\_STOPx(LL)}$ + 20		
Zero Crossing Blanking Filter NCP1680AA, AB: NCP1680AC:		$t_{FILT(ZCB)}$	–	 20 Disabled	25	µs
Polarity Detection Control						
Polarity Detection Filter NCP1680AA, AB: NCP1680AC:		t_{POL_FILTER}	–	 200 50		µs
Polarity Detection Threshold	V_{POL_DETx} = V_{LVSNS1} − V_{LVSNS2} V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V	V_{POL_DET1} V_{POL_DET2}	−55 −20	−15 15	20 55	mV

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is –40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
AC ZERO CROSSING MANAGEMENT						
Slow Leg (SR) Drive Control						
Slow Leg Zero Crossing Blanking Thresholds						mV
Threshold to Stop SRx Pulses	$V_{SR\_STOP} = \lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V	$V_{SR\_STOP1(LL)}$ $V_{SR\_STOP2(LL)}$		180		
Threshold to Start SRx Pulses	$V_{SR\_START} = \lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Increasing, V_{LVSNS2} = 0 V V_{LVSNS1} Decreasing, V_{LVSNS2} = 4 V	$V_{SR\_START1(LL)}$ $V_{SR\_START2(LL)}$		$V_{SR\_STOPx(LL)}$ + 20		
Synchronous (1 – d) Drive Control						
Sync Zero Crossing Blanking Thresholds						mV
Threshold to Stop Sync Pulses	$V_{SYNC\_STOP} = \lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V	$V_{SYNC\_STOP1(LL)}$ $V_{SYNC\_STOP2(LL)}$		200		
Threshold to Start Sync Pulses	$V_{SYNC\_START} = \lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Increasing, V_{LVSNS2} = 0 V V_{LVSNS1} Decreasing, V_{LVSNS2} = 4 V	$V_{SYNC\_START1(LL)}$ $V_{SYNC\_START2(LL)}$		$V_{SYNC\_STOPx(LL)}$ + 20		
BROWN−OUT, LINE SAG AND LINE RANGE DETECTION						
Line Sag and Brown−Out Detection Upper Threshold	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Increasing	$V_{BO(START)}$	1.02	1.10	1.18	V
Line Sag and Brown−Out Detection Lower Threshold	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Decreasing	$V_{BO(STOP)}$	0.92	1.00	1.08	V
Brown−Out Detection Hysteresis	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Increasing	$V_{BO(HYS)}$	60	100		mV
Line Sag Detection Blanking Timer	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert < V_{BO(STOP)}$, Delay to Soft Stop Enable	$t_{SAG(blank)}$	20	25	30	ms
Brown−Out Detection Blanking Timer	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Decreasing, Delay to Polarity Disable	$t_{BO(blank)}$	520	650	780	ms
High−Line Level Detection Threshold	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Increasing	V_{HL}	2.20	2.36	2.52	V
Low−Line Level Detection Threshold	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Decreasing	V_{LL}	2.07	2.22	2.37	V
Line Range Select Hysteresis	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Increasing	$V_{LR(HYS)}$	100	140		mV
High to Low Line Mode Selector Timer	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert < V_{LL}$	$t_{blank(LL)}$	20	25	30	ms
Low to High Line Mode Selector Timer Filter	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert > V_{HL}$	$t_{filter(HV)}$	200	300	400	μs
Lockout Timer for Low to High Line Mode Transition	Low Line Mode, $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert > V_{HL}$	$t_{line(lockout)}$	400	500	600	ms
AC LINE FREQUENCY MONITORING						
Line Frequency Upper Threshold		$t_{LINE(65)}$	66	72	78	Hz
Line Frequency Lower Threshold		$t_{LINE(45)}$	37	41	45	Hz
Device Enable Counter		N_{DRV_EN}		4		
Slow Leg Disable Counter		N_{SR_DIS}		1		

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
AC LINE FREQUENCY MONITORING						
Line Frequency2 Timer	Delay to PWM Disable	$t_{LINEFREQ(DLY)}$	60	100	165	ms
VALLEY DETECTION CIRCUIT						
Valley Detection Thresholds in Positive Half Line Cycle	V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{AUX} Rising (Arm) V_{AUX} Falling (Trigger)	 $V_{VD1\_TH(rising)}$ $V_{VD1\_TH(falling)}$	 150 50	 200 100	 250 150	mV
Valley Detection Hysteresis in Positive Half Line Cycle		$V_{VD1(HYS)}$	50	100		mV
Propagation Delay of Valley Detection in Positive Half Line Cycle	Step V_{AUX} 1.5 V to −0.2 V, Time to PWML = 2.5 V	T_{VD1}		50	80	ns
Valley Detection Thresholds in Negative Half Line Cycle	V_{LVSNS1} = 0 V, V_{LVSNS2} = 1.2 V, V_{AUX} Falling (Arm) V_{AUX} Rising (Trigger)	 $V_{VD2\_TH(falling)}$ $V_{VD2\_TH(rising)}$	 50 150	 100 200	 150 250	mV
Valley Detection Hysteresis in Negative Half Line Cycle		$V_{VD2(HYS)}$	50	100		mV
Propagation Delay of Valley Detection in Negative Half Line Cycle	Step V_{AUX} 0 V to 1.5 V, Time to PWMH = 2.5 V	T_{VD2}		45	75	ns
Minimum AUX Pulse Width		T_{SYNC}		95	155	ns
AUX Pin Bias Current, V_{AUX} = $V_{VD1\_TH(rising)}$		$I_{AUX(bias1)}$	0.5	1	2	μA
AUX Pin Bias Current, V_{AUX} = $V_{VD1\_TH(falling)}$		$I_{AUX(bias2)}$	0.5	1	2	μA
FAST LEG DRIVE SIGNALS (PWML & PWMH)						
PWMx Rise Time, x = L, H	V_{PWMx} = 10% to 90% of 5 V, C_{PWMx} = 1 nF	$T_{PWMx(rise)}$		95		ns
PWMx Fall Time	V_{PWMx} = 90% to 10% of 5 V, C_{PWMx} = 1 nF	$T_{PWMx(fall)}$		30		ns
Source Resistance		ROH	–	15	25	Ω
Sink Resistance		ROL	–	5	10	Ω
Peak Source Current (Guaranteed by Design)	V_{PWMx} = 0 V	$I_{PWMx(SRC)}$		100		mA
Peak Sink Current (Guaranteed by Design)	V_{PWMx} = 5 V	$I_{PWMx(SNK)}$		160		mA
PWMx Clamp Voltage	R_{PWMx} = 10 kΩ	$V_{PWMx(high)}$	4.5	5	5.5	V
Non−overlap Time between Falling Edge of PWMd & Rising Edge of PWM(1−d)	V_{ZCD} = 0.5 V	T_{DT1}	90	130	170	ns
SLOW LEG DRIVE SIGNALS (SRL & SRH)						
SRx Rise Time x = L, H	V_{PWMSRx} = 10% to 90% of 12 V C_{PWMSRx} = 1 nF	$T_{PWMSRx(rise)}$		185		ns
SRx Fall Time	V_{PWMSRx} = 90% to 10% of 12 V C_{PWMSRx} = 1 nF	$T_{PWMSRx(fall)}$		125		ns
Source Resistance		ROH2	–	45	85	Ω
Sink Resistance		ROL2	–	30	60	Ω

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
SLOW LEG DRIVE SIGNALS (SRL & SRH)						
SRx Peak Source Current (Guaranteed by Design)	V_{PWMSRx} = 0 V	$I_{PWMSRx(SRC)}$		100		mA
SRx Peak Sink Current (Guaranteed by Design)	V_{PWMSRx} = 12 V	$I_{PWMSRx(SNK)}$		160		mA
SRx Clamp Voltage	R_{PWMSRx} = 10 kΩ, V_{CC} = 30 V	$V_{PWMSRx(high)}$	10	12	14	V
SRx Minimum Drive Voltage	R_{PWMSRx} = 10 kΩ, V_{CC} = $V_{CC(off)}$ + 100 mV	$V_{PWMSRx(MIN)}$	7.8	9		V
POLARITY OUTPUT						
POLARITY Rise Time	$V_{POLARITY}$ = 10% to 90% of 12 V, $C_{POLARITY}$ = 1 nF	$T_{POLARITY(rise)}$		185		ns
POLARITY Fall Time	$V_{POLARITY}$ = 10% to 90% of 12 V, $C_{POLARITY}$ = 1 nF	$T_{POLARITY(fall)}$		125		ns
Source Resistance		ROH3	–	45	85	Ω
Sink Resistance		ROL3	–	30	60	Ω
POLARITY Peak Source Current (Guaranteed by Design)	$V_{POLARITY}$ = 0 V	$I_{POLARITY(SRC)}$		100		mA
POLARITY Peak Sink Current (Guaranteed by Design)	$V_{POLARITY}$ = 12 V	$I_{POLARITY(SNK)}$		160		mA
POLARITY Clamp Voltage	$R_{POLARITY}$ = 10 kΩ V_{CC} = 30 V	$V_{POLARITY(high)}$	10	12	14	V
POLARITY Minimum Drive Voltage	$R_{POLARITY}$ = 10 kΩ V_{CC} = $V_{CC(off)}$ + 100 mV	$V_{POLARITY(MIN)}$	7.8	9		V
ON TIME MODULATION CIRCUIT						
Maximum On Time in CrM NCP1680AA NCP1680AB, AC	V_{FB} < V_{REF}, V_{LVSNS1} = 1.20 V, V_{LVSNS2} = 0 V	$T_{on, max, CrM}$	 15.5 9	 17.2 10.2	 18.9 11.4	µs
Maximum Frequency Clamp NCP1680AA NCP1680AB, AC		F_{clamp1}		 130 275		kHz
On−Time Below Which Frequency Foldback is Engaged NCP1680AA NCP1680AB, AC	 Low Line High Line Low Line High Line	$(t_{ON\_FF})_{LL}$ $(t_{ON\_FF})_{HL}$		 3.84 1.92 1.82 0.91		µs
Minimum Frequency Clamp		F_{MIN}	25	30.5	36	kHz
Minimum On−Time	V_{FB} > V_{REF}, C_{PWMx} = Open	$T_{on, min}$	200	260	320	ns
Maximum On Time in DCM NCP1680AA NCP1680AB, AC		$T_{on, max, DCM}$		 20 12.7		µs
REGULATION BLOCK						
Feedback Voltage Reference: @ 25°C Over the Temperature Range		V_{REF}	 2.475 2.44	 2.50 2.50	 2.525 2.56	V

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is –40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
REGULATION BLOCK						
Ratio (V_{OUT} Low Detect Lower Threshold / V_{REF}) (Guaranteed by Design)	V_{FB} Decreasing	$V_{DRE}L$ / V_{REF}	95.0	95.5	96.0	%
Ratio (V_{OUT} Low Detect Higher Threshold / V_{REF} (Guaranteed by Design)	V_{FB} Increasing	$V_{DRE}H$ / V_{REF}	97.5	98.0	98.5	%
Ratio (V_{OUT} Low Detect Hysteresis / V_{REF}) (Guaranteed by Design)	V_{FB} Increasing	H_{DRE} / V_{REF}	2	2.5	–	%
Loop Gain Increase due to Dynamic Response Enhancer NCP1680AA, AB NCP1680AC All Devices	 PFCOK = High PFCOK = Low	 K_{DRE1} K_{DRE0}		 5x 10x 2.5x		–
STATIC OVP						
Duty Ratio	V_{FB} = 3 V	D_{MIN}	–	–	0	%
SOFT SKIP CIRCUIT						
$\overline{SKIP}$ Voltage in CrM/DCM		$V_{\overline{SKIP}}$	4.5	5	5.5	V
$\overline{SKIP}$ Current Capability		$I_{\overline{SKIP}}$	450	700	–	μA
$\overline{SKIP}$ Threshold Voltage to Enter Skip Mode		$V_{SKIP(th)}$	1.2	1.5	1.8	V
$\overline{SKIP}$ Minimum Pulse Duration for SKIP Detection	$V_{\overline{SKIP}} < V_{SKIP(th)}$	T_{SKIP1}	56			μs
PFCOK SKIP Threshold		V_{SKIP2}	0.4	0.5	0.6	V
Minimum PFCOK Negative Pulse Duration for SKIP Detection		T_{SKIP2}	10	30	50	μs
V_{FB} Lower Value at the End of a Soft Skip Cycle Burst Defined as a V_{REF} Percentage		$(R_{FB})_{recover}$	92.5	94	95.5	%
V_{FB} Restart Level in Skip Cycle		$V_{RESTART}$		2.35		V
Blanking Time for Operation Recovery		$T_{recover}$	400	500	600	ms
$\overline{SKIP}$ Confirmation Window		T_{WINDOW}		400		μs
ZCD PIN						
ZCD Arming Threshold NCP1680AA NCP1680AB, AC	V_{ZCD} Increasing	$V_{ZCD(ARM)}$		 300 100		mV
ZCD Trigger Threshold	V_{ZCD} Decreasing	$V_{ZCD(TRG)}$		50		mV
Threshold for Inrush Current Protection		$V_{ZCD(INRUSH)}$		50		mV
Propagation Delay to (1–D) Drive Pulse	Step V_{ZCD} 0 V to $V_{ZCD(ARM)}$ + 250 mV Time to PWMx = 2.5 V	$T_{ZCD(ARM)}$	–	45	75	ns
Propagation Delay (1–D) Drive Termination	Step V_{ZCD} 1 V to $V_{ZCD(TRIG)}$ – 250 mV; Time to PWMx = 2.5 V	$T_{ZCD(TRG)}$	–	45	75	ns

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is –40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
ZCD PIN						
Low−Line Range ZCD Protection Threshold NCP1680AA NCP1680AB, AC		$V_{ZCDLIM1(LL)}$	 1.33 0.56	 1.4 0.6	 1.47 0.64	V
High−Line Range ZCD Protection Threshold NCP1680AA NCP1680AB, AC		$V_{ZCDLIM1(HL)}$	 0.80 0.325	 0.84 0.36	 0.88 0.395	V
On−Time in CrM Current Limit	V_{FB} = 2.0, V_{ZCD} pulse 0–2 V LVSNS1 = 1.626, Pulse for 16 μs LVSNS1 = 3.253, Pulse for 14 μs	 $T_{ON\_ZCDLIM(LL)}$ $T_{ON\_ZCDLIM(HL)}$		 1.9 1.3		μs
ZCD Pullup Current Source	V_{ZCD} = 0 V V_{ZCD} = 2.7 V	I_{ZCD}	0.7 0.7	1 1	1.3 1.3	μA
ZCD Minimum Current Threshold for THD Enhancer Enable NCP1680AA NCP1680AB, AC	V_{ZCD} Increasing	$V_{ZCD(MIN)}$	 45 5	 70 30	 95 55	mV
ZCD Minimum Current Ratio	$K_{ZCD(MIN)}$ = $V_{ZCD(MIN)}/V_{ZCDLIM1(LL)}$	$K_{ZCD(MIN)}$		5		%
UNDERVOLTAGE & OVERVOLTAGE PROTECTION						
UVP Threshold	V_{FB} Decreasing	V_{UVP}	–	0.3	–	V
Ratio (UVP Threshold) over V_{REF} (V_{UVP}/V_{REF})	V_{FB} Decreasing	R_{UVP}	8	12	16	%
UVP Hysteresis	V_{FB} Increasing	$V_{UVP(HYST)}$	–	50	100	mV
Soft OVP Threshold	V_{FB} Increasing	$V_{softOVP}$	–	2.625	–	V
Ratio (soft OVP Threshold) over V_{REF} ($V_{softOVP}/V_{REF}$)	V_{FB} Increasing	$R_{softOVP}$	104	105	106	%
Ratio (soft OVP Hysteresis) over V_{REF}	V_{FB} Decreasing	$R_{softOVP(H)}$	1.5	2	2.5	%
Fast OVP Threshold	V_{FB} Increasing	$R_{fastOVP}$	–	2.7	–	V
Ratio (Fast OVP Threshold) over (soft OVP Upper Threshold) ($V_{fastOVP}/V_{softOVP}$)	V_{FB} Increasing	$R_{fastOVP1}$	102.4	103	103.4	%
Ratio (Fast OVP Threshold) over V_{REF} ($V_{fastOVP}/V_{REF}$)	V_{FB} Increasing	$R_{fastOVP2}$	106.5	108	109.5	%
FB Threshold for Recovery from a Soft or Fast OVP	V_{FB} Decreasing	$V_{OVPrecover}$		2.575		V
FB Bias Current @ V_{FB} = $V_{softOVP}$ and V_{FB} = V_{UVP}		$(I_B)_{FB}$	50	250	450	nA
PFCOK & BUV PROTECTION						
PFCOK Voltage in OFF Mode	PFCOK Pin Sink Current = 1 mA	$V_{PFCOK(low)}$	–	–	100	mV
PFCOK Current	V_{FB} = 2.5 V, V_{PFCOK} = 1 V	I_{PFCOK}	23	25	27	μA
BUV Threshold NCP1680AA, AB NCP1680AC	V_{FB} Decreasing	V_{BUV}	 1.95 1.45	 2.0 1.5	 2.05 1.55	V

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT}= open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is –40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
PFCOK & BUV PROTECTION						
BUV Delay During Which Operation Is Disabled		T_{BUV}	400	500	600	ms
FAULT PROTECTION						
OTP Fault Threshold	V_{Fault} Decreasing	$V_{FLT(OTP)}$	0.38	0.40	0.42	V
OTP Fault Source Current	V_{Fault} = $V_{FLT(OTP)}$ + 200 mV	I_{FLT}	43	46	49	μA
OTP Detection Filter Delay	V_{Fault} Decreasing	$t_{OTP(DLY)}$	22.5	30	37.5	μs
OTP Blanking During Startup		$t_{OTP(BLANK)}$	4	5	6	ms
OTP Fault Recovery Threshold	V_{Fault} Increasing	$V_{FLT(REC)}$	0.874	0.92	0.966	V
OVP Fault Threshold	V_{Fault} Increasing	$V_{FLT(OVP)}$	2.88	3	3.12	V
OVP Detection Filter Delay	V_{Fault} Increasing	$t_{OVP(DLY)}$	22.5	30	37.5	μs
Fault Clamp Voltage	V_{Fault} = Open	$V_{FLT(CLAMP)}$	1.15	1.7	2.25	V
Fault Clamp Resistance		$R_{FLT(CLAMP)}$	1.32	1.55	1.78	kΩ
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	Temperature Increasing	T_{SHDN}	–	150	–	°C
Thermal Shutdown Hysteresis	Temperature Decreasing	$T_{SHDN(HYS)}$	–	50	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TOTEM POLE THEORY OF OPERATION

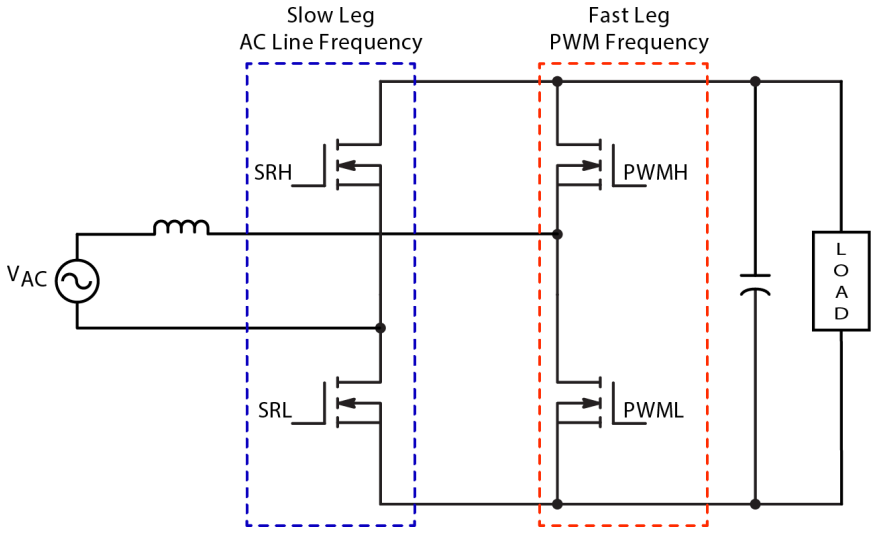


Figure 4. Block Diagram

The Totem Pole PFC (TPFC) circuit is shown in Figure 4. The topology consists of two half−bridge configurations; one half bridge, commonly referred to as the “Fast Leg” switches at the PWM frequency and the other, commonly referred to as the “Slow Leg” switches at the AC line frequency. The fast leg switches perform the role of the switch and the diode in a classical boost PFC, that is these switches function to regulate the output voltage and shape the input current to provide high power factor and low harmonic distortion. The slow leg switches perform the role of the diode bridge in a classical boost PFC. Active switches with low ON resistance are utilized instead of diodes resulting in improved efficiency. Also, as will be described in the discussion below, the TPFC operates with only one

slow leg and one fast leg device in the conduction path whereas the conventional boost PFC operates with two bridge diodes and one active switch or boost diode in the conduction path. Fewer devices in the conduction path and active switches replacing bridge diodes allow the TPFC topology to achieve higher system efficiency and power density than the classical boost PFC.

The fast leg switches are represented as MOSFETs in this particular figure, but the type of switch used for these devices is adaptable and either silicon FETs or Wide Bandgap (WBG) transistors can be used. Silicon FETs specified as fast recovery and/or low reverse recovery charge (Q_{rr}) are suitable for this topology. WBG devices, whether Silicon Carbide (SiC) or Gallium Nitride (GaN), offer excellent $Q_g{*}R_{ds(on)}$ figure of merit and virtually no Q_{rr}, making them optimal devices for the TPFC fast leg. The NCP1680 is designed for Critical Conduction Mode (CrM) and the PWM drive signals are logic level signals so there is no restriction on using either Si or WBG devices with the selection of an appropriate external half bridge driver.

The TPFC operates with bidirectional current flow in the inductor and the command of the fast and slow leg switches changes depending on the polarity of the AC line cycle. Operation of the TPFC during the positive and negative half line cycles is illustrated in Figure 5 and Figure 6, respectively.

Positive Half Cycle Operation

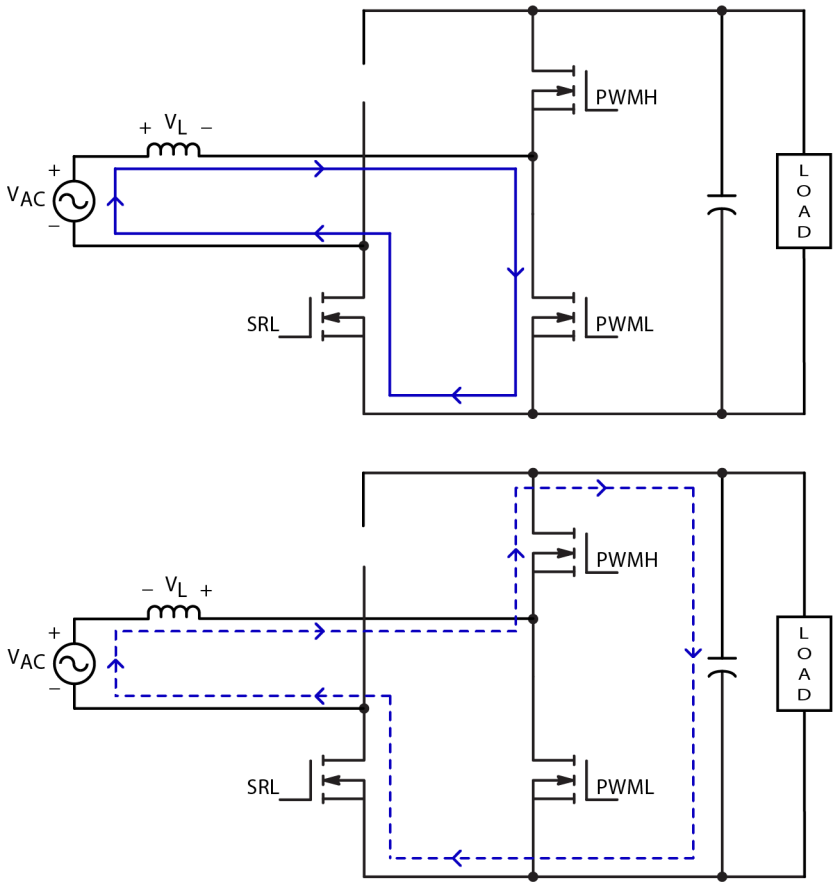


Figure 5. Positive Half Cycle Operation

During the positive AC line cycle the PWML signal is responsible for performing pulse width modulation or duty cycle control of the converter. PWML toggles high turning on the low side fast leg device, allowing current to charge and store energy in the inductor, as shown by the solid blue line in Figure 5. When the PWML signal toggles low the inductor current diverts through the high side fast leg switch, transferring energy from the inductor to the load, as shown by the dashed blue line. In this half line cycle the high side fast leg device does not need to conduct for proper PFC operation, however the PWMH signal can toggle high to turn on the high side device, providing enhanced system efficiency at medium to high load levels. Throughout the positive half line cycle current is flowing left to right through the inductor and always returning to the source through the low side slow leg device, hence the SRL signal can toggle high to turn on the respective slow leg device for optimum converter efficiency.

Negative Half Cycle Operation

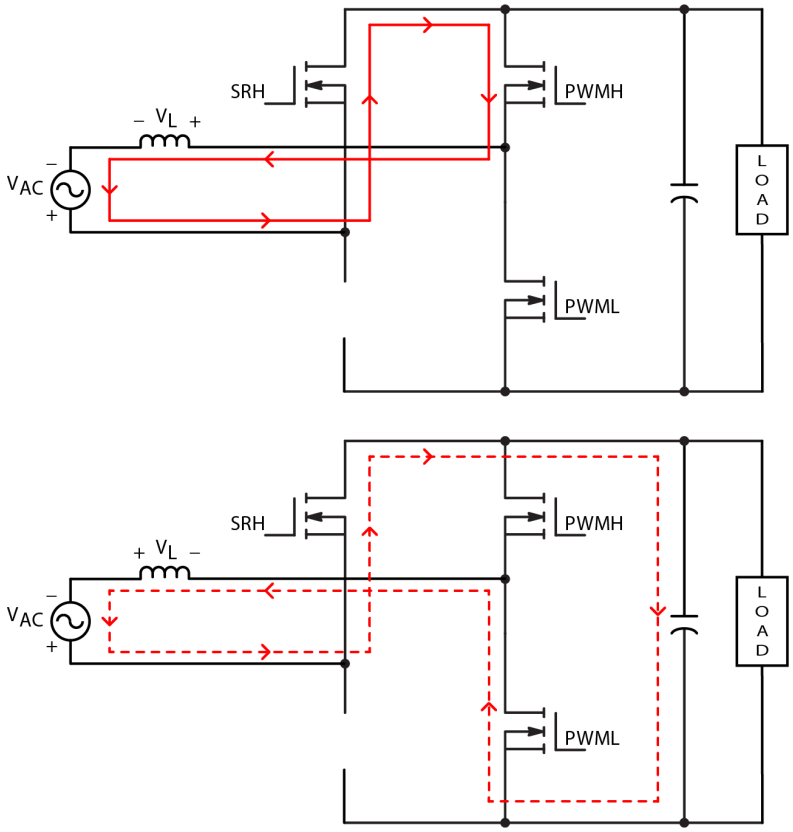


Figure 6. Negative Half Cycle Operation

During the negative AC line cycle the PWMH signal is responsible for performing pulse width modulation or duty cycle control of the converter. PWMH toggles high commanding the high side fast leg device to conduct, allowing current to charge and store energy in the inductor, as shown by the solid red line in Figure 6. When the PWMH signal toggles low the inductor current diverts through the low side fast leg switch, transferring energy from the inductor to the load, as shown with the dashed red line. In this half line cycle the low side fast leg device does not need to conduct for proper PFC operation, however the PWML signal can toggle high to turn on the low side device, providing enhanced system efficiency at medium to high load levels. Throughout the negative half line cycle current is flowing right to left through the inductor and always returning to the source through the high side slow leg device, hence the SRH signal can toggle high to turn on the respective slow leg device for optimum converter efficiency.

V_{CC} Management and Startup Sequence

The NCP1680 controller requires a supply bias of at least $V_{CC(ON)}$, typically 10.5 V, to enable and begin normal operation. Since the controller does not include an internal high voltage startup, the bias supply will have to come from an external source such as a dedicated auxiliary supply or from a downstream converter. Additionally, the controller must have sufficient input voltage (BONOK cleared) and validation that the ac line frequency is within the expected operating range ($N_{DRV\_EN} \geq 4$), then the control can power up on the next rising polarity edge, synchronizing the startup to a positive half line cycle. The startup requirements are summarized:

- Brown−out protection, BONOK, is cleared
- $V_{CC} > V_{CC(ON)}$
- $N_{DRV\_EN} \geq 4$
- Polarity rising edge

If the supply voltage is in the hysteresis band, i.e. if $V_{CC(OFF)} < V_{CC} < V_{CC(ON)}$ then the controller will not start up. This is done to ensure that the minimum specified hysteresis between $V_{CC(ON)}$ and $V_{CC(OFF)}$ of 1.2 V, is available for the device so that the increased current consumption at startup doesn't pull V_{CC} below $V_{CC(OFF)}$, typically 8.8 V. Once the device has been enabled then the V_{CC} voltage can fall to as low as $V_{CC(OFF)}$ without disabling but for startup the V_{CC} voltage has to exceed and remain above $V_{CC(ON)}$.

Line Voltage Sensing

Figure 7 shows the recommended application configuration for the line voltage sensing scheme. External resistor dividers are required to divide down two high voltage nodes to perform differential line sensing. The recommended divide down factor for universal input consumer applications is K_{L_DIV}, typically 100; i.e. $\frac{R_{LOWERx}}{(R_{LOWERx} + R_{UPPERx})} = \frac{1}{K_{L\_DIV}}$ such that the low voltage signals which interface to the NCP1680 are approximately 1% of the high voltage signals that are being monitored. The LVSNS1 pin is intended to interface with the low frequency node of the main boost inductor, L_{BOOST}, and the LVSNS2 pin is intended to interface with the bridge voltage of the slow leg power switches. The internal Line Detector circuit is designed with substantially high input impedance allowing for large external resistors to minimize the power dissipation in the dividers, enabling the application to achieve low no load power consumption. Typical values for R_{UPPERx} can be in the range of 5 MΩ to 10 MΩ while R_{LOWERx} can be 50 kΩ to 100 kΩ. In practice the upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop.

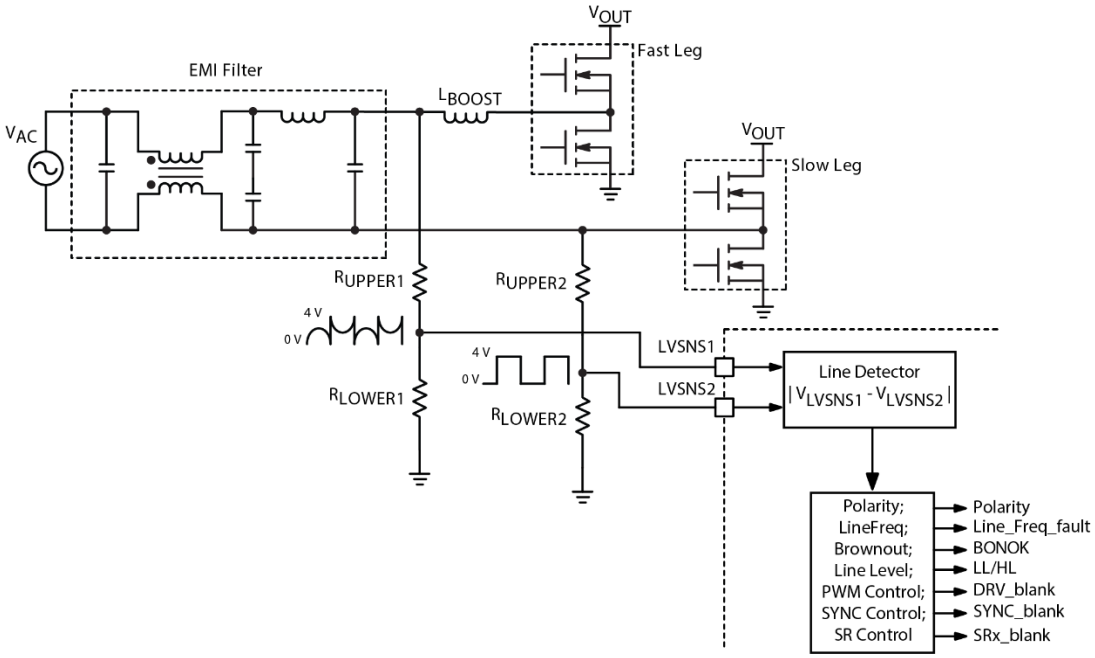


Figure 7. Line Sensing Configuration

In the Totem Pole topology the AC line voltage floats with respect to the controller ground. This necessitates a differential measurement technique to determine the AC line voltage magnitude. The NCP1680 employs differential voltage detection and rectification to reconstruct a waveform equal to $|V_{LVSNS1} - V_{LVSNS2}|$. For simplicity $|V_{LVSNS1} - V_{LVSNS2}|$ will be referred to as V_{LINE}. The key waveforms are shown in Figure 8. The reconstructed waveform is utilized to perform functions such as brown−out and line level detection where it is necessary to measure the amplitude of the line voltage. The line voltage sensing will additionally be responsible for determining the polarity (i.e. positive or negative half−line cycle) of the AC voltage and for measuring the frequency of the AC line voltage. In total, the line sense will be utilized for the following functions:

a. Polarity detection
b. AC Line Frequency Monitoring
c. Brownout protection feature
d. Line level detection
e. AC zero crossing drive management

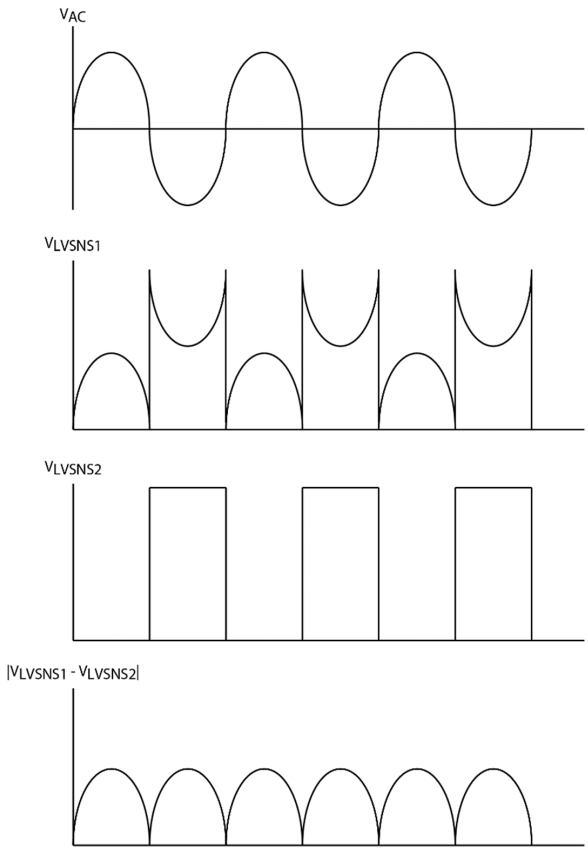


Figure 8. Line Sense Waveforms

Polarity Detection

Figure 9 shows a simplified diagram of the polarity detection circuitry. The two line sense signals are compared directly against each other to determine when they intersect. The intersection or crossover of the two signals indicates that the AC line voltage has changed polarity. External filter capacitance may be added to improve noise immunity of the polarity detection circuitry; the recommend time constant of the RC filter is about 50 μs to 200 μs, enough to provide noise immunity from the switching frequency of the power supply but not such a large time constant so as to introduce significant lag in the line sense signals.

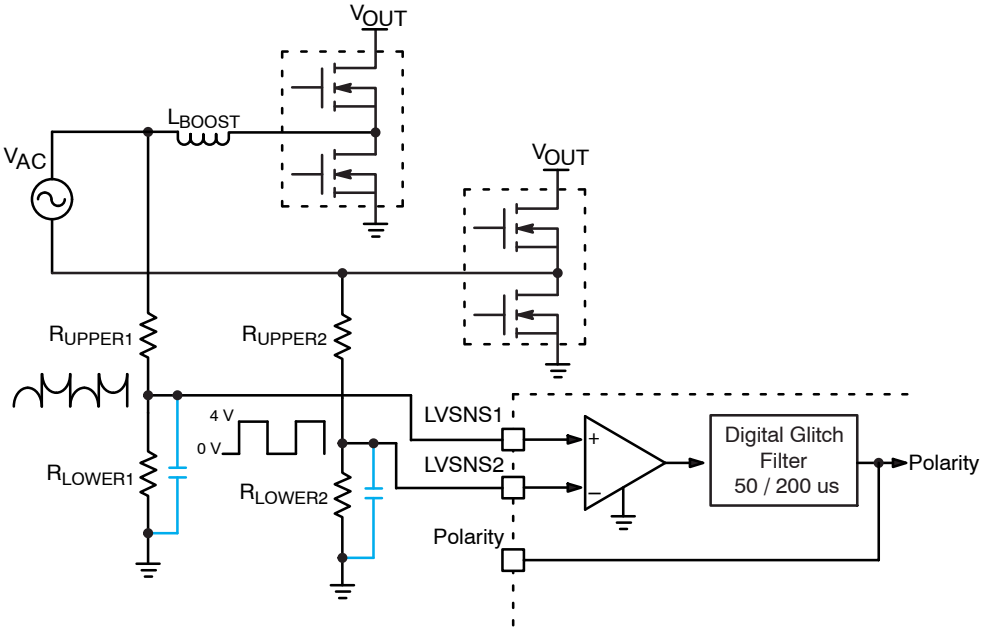


Figure 9. Polarity Detection Diagram

Additionally, the output of the polarity sense comparison circuit is passed through a digital glitch filter which will provide additional immunity if the comparison circuit is toggling repeatedly. The glitch filter has a timer, T_{POL_FILTER}, of 50 or 200 μs depending on the device variant. The behavior of the filter is shown below in Figure 10. The input to the filter must remain at a logic state (high or low) for greater than the filter's timer for the output to transition to that state. If the input transitions from high to low (or vice versa) but does not remain in that state for a time greater than T_{POL_FILTER}, then the output will remain in its previous logic state and the timer will effectively reset. In Figure 10, time durations t1, t2, t3 and t5, t6, t7 are all less than T_{POL_FILTER} and hence the output of the filter remains unchanged. Time durations t4 and t8 are greater than T_{POL_FILTER}, causing the output to transition to the new state.

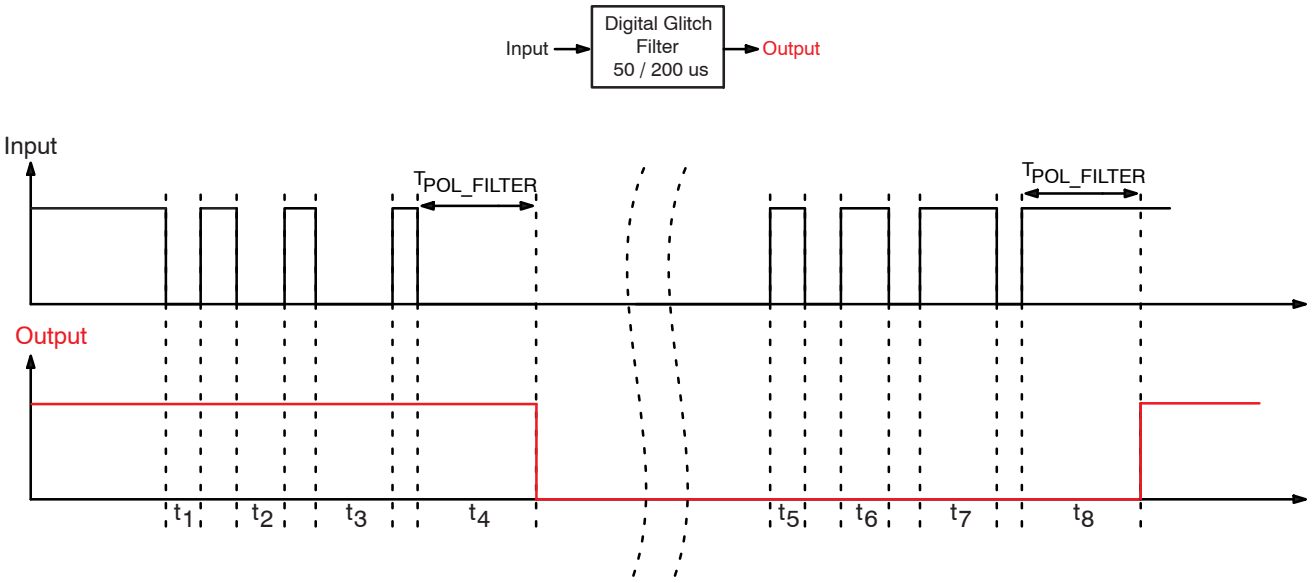


Figure 10. Polarity Glitch Filter Operation

AC Line Frequency Monitoring

The NCP1680 controller comes with an optional line frequency monitoring circuit. The NCP1680 utilizes timers & counters to monitor the AC line frequency ($T_{LINEFREQ}$) to ensure that the polarity comparator output toggles at a rate consistent with the mains frequency specification of 45 Hz to 65 Hz. A timing diagram of the AC line frequency monitor operation is shown in Figure 11. Practically the controller measures the time between every edge transition of the filtered polarity signal. If one timing interval, such as t_1, measures outside of the expected frequency range then the controller will disable the slow leg drive signals, SRL and SRH, and start a 100 ms timer, $t_{LINEFREQ(DLY)}$. If a timing interval within the specification is measured prior to $t_{LINEFREQ(DLY)}$ expiring, then $t_{LINEFREQ(DLY)}$ is reset and slow leg drive pulses are again enabled. This is shown with timing interval t_2 and t_3.

Should the polarity toggles continue to measure outside of the mains frequency specification and the timer expires then the controller will disable fast leg drive pulses and enter fault mode as shown after t_5. Note that throughout timing interval t_5 the slow leg pulses are disabled. While in fault mode the polarity signal and the line frequency monitor will remain active, performing continuous time interval measurements of the polarity signal. The device will auto−recover from the fault mode once the device detects 4 consecutive polarity edges that are within the line frequency specification, same as a new startup. The thresholds for the AC line frequency monitor are given by $t_{LINE(65)}$, nominally 72 Hz, and $t_{LINE(45)}$, nominally 42 Hz. These thresholds are designed to provide some margin so that under worst case tolerance the AC line frequency can always operate from 45 Hz to 65 Hz.

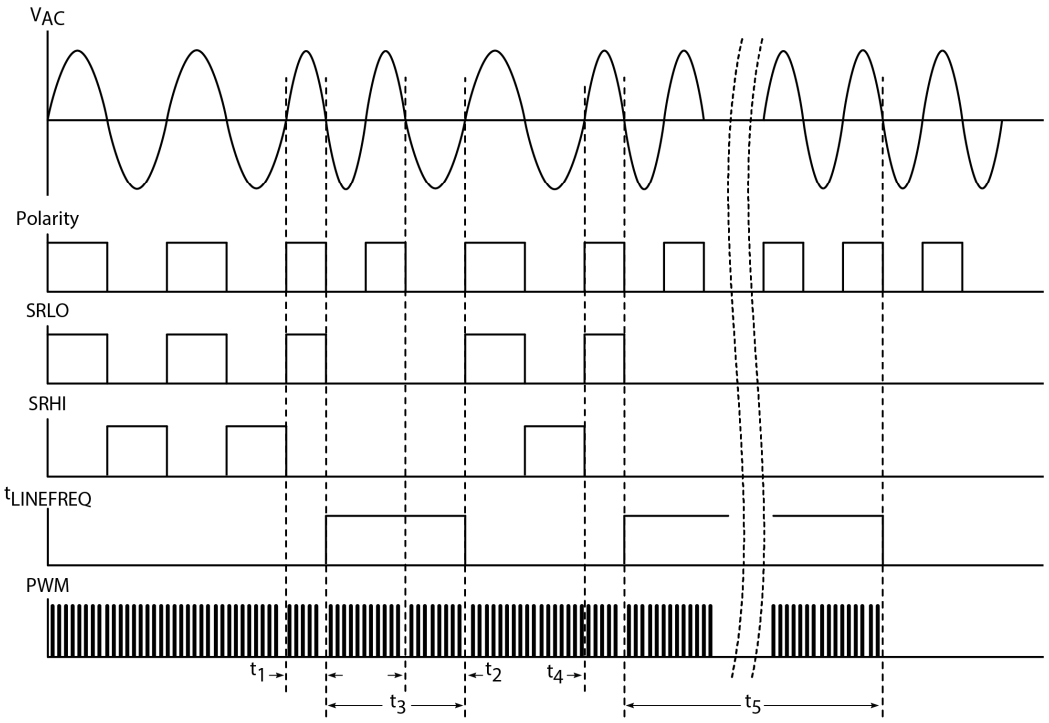


Figure 11. Line Frequency Faults Timing Diagram

As previously mentioned, startup of the NCP1680 controller is synchronized to the rising edge of the filtered polarity signal and requires at least 4 consecutive half−line cycles (polarity toggles) to be within the valid $T_{LINEFREQ}$ duration. The controller enable counter is denoted as N_{DRV_EN} in the electrical table. Line Frequency operation is shown in Figure 12 where the Line Freq OK flag is set high on the rising edge of the 4th consecutive polarity toggle with valid time duration. The rising edge of the polarity signal indicates that the AC line is entering a positive half line cycle which is the preferred conduction angle for starting up the application because the low−side fast leg device will be the duty cycle controlled device.

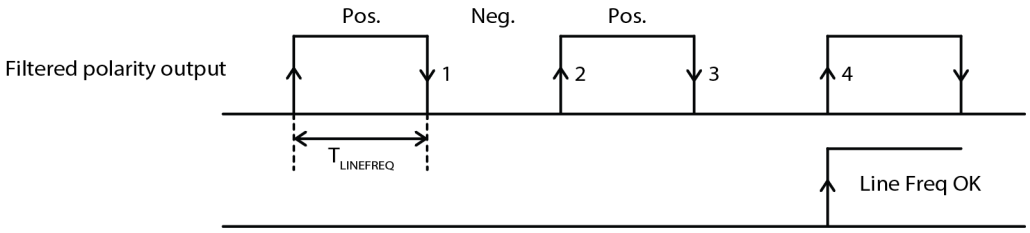


Figure 12. Polarity Startup Timing Diagram

Brown−Out and Line Sag Protection

The NCP1680 feature set includes line voltage Brown−out (BO) and Line sag (SAG) detection. These detection circuits function collaboratively as a line voltage UVLO, enabling drive pulses when the peak line voltage exceeds the $V_{BO(start)}$ threshold, typically 1.1 V, and disabling drive pulses when the line voltage falls below the $V_{BO(stop)}$ threshold, typically 1 V, for a given timer duration. Considering that the LVSNSx inputs are recommended to be 1% of the AC line voltage, this translates to a nominal enable threshold of ~ 110 V, or ~ 78 V_{AC}, and a nominal disable threshold of ~ 100 V, or ~ 71 V_{AC}.

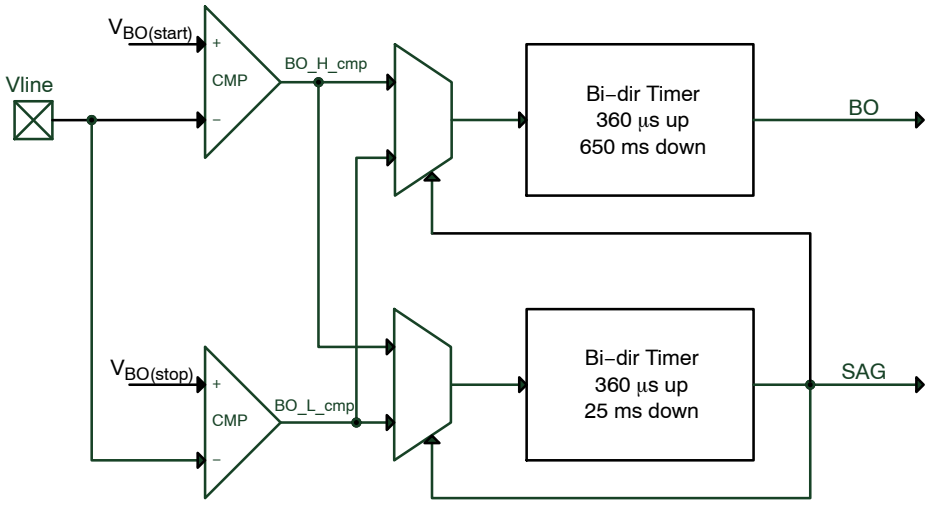


Figure 13. BO/SAG Detection Circuit

Figure 13 is a representative schematic of the NCP1680 BO/SAG detection circuitry. The circuitry monitors the line voltage, V_{LINE}, generated by the NCP1680's internal differential line sensing. V_{LINE} is compared against the two V_{BO} thresholds. Both the BO and SAG voltage thresholds are the same, with the difference between the two features being the timing after which the respective output is set high, and the action taken by the controller after each of the respective outputs. Figure 14 illustrates the controller response during a line sag and brownout.

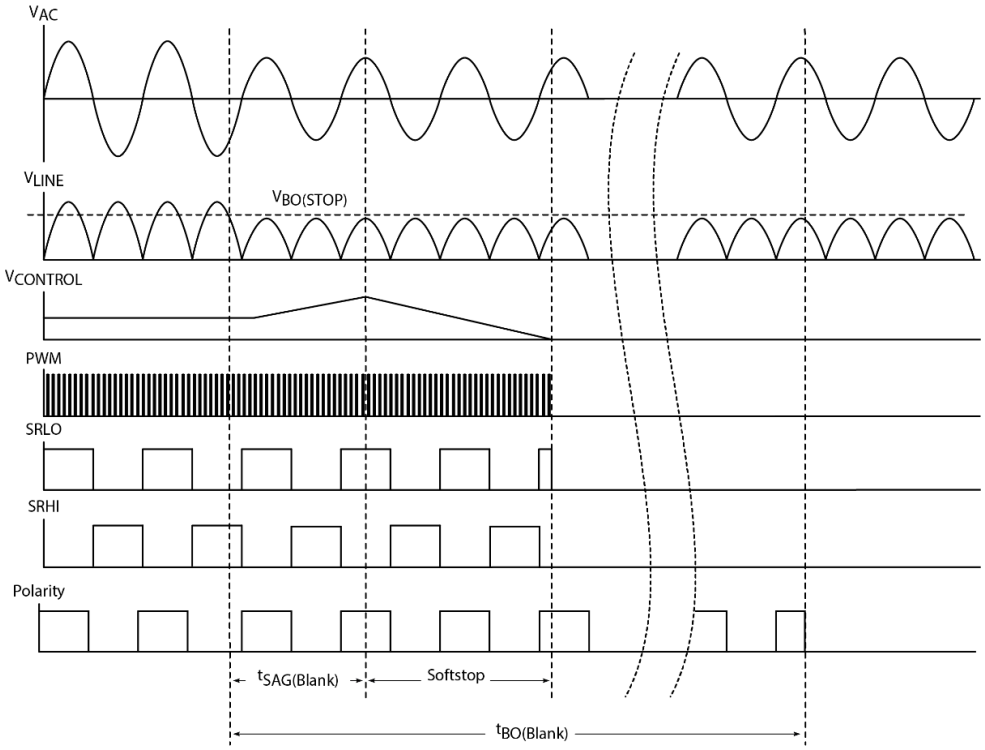


Figure 14. Line Sag and Brownout Timing Diagram

The 25 ms SAG timer, $t_{SAG(blank)}$, allows the application to sustain a line voltage dropout for a single AC line cycle while the NCP1680 continues to deliver drive pulses. If the SAG timer expires, the controller will enter a soft stop period where the internal control voltage is slowly discharged to 0 V and the pulse width of the PWM is gradually narrowed, reducing the power delivery of the application. After the soft stop period the polarity signal remains active and the controller will be ready for immediate restart should the line voltage exceed the $V_{BO(start)}$ threshold. If the 650 ms brown−out timer expires, the NCP1680 will disable the polarity detection circuit and

reset the device, including any latching faults. When the application restarts from a BO the controller functions as it would for an initial power up.

Line Range Detection

The NCP1680 features input voltage range detection, which distinguishes between high line (nominally 230 V_{AC}) and low line (nominally 115 V_{AC}) input voltages. The input voltage range is detected based on the peak voltage measured with the reconstructed V_{LINE} signal. By default the controller will power up into low line mode. If V_{LINE} exceeds the high line threshold, V_{HL}, typically 2.36 V, for a duration longer than $t_{filter(HV)}$, typically 300 μs, the controller transitions to high line mode. Once in high line mode the peak line voltage must fall below V_{LL}, typically 2.22 V, for a duration longer than $t_{blank(LL)}$, typically 25 ms, to enter back into the low line mode. The blanking duration, $t_{blank(LL)}$, is set long enough to allow the controller to remain in high line mode in the event of a single line cycle dropout. Should the controller transition from high line to low line mode, a lockout timer $t_{line(lockout)}$, typically 500 ms, is enabled. The lockout timer blocks the controller from transitioning back to high line immediately after a low line transition for the duration of the timer, preventing the controller from oscillating between low line and high line mode. The transition thresholds of 2.36 V and 2.22 V typically translate to line voltages of 167 and 157 V_{AC}, respectively, which are intermediate voltages that do not correspond to any national standard for AC mains, leaving little likelihood that the input voltage to the application will operate near the transition thresholds. Further, the transition thresholds have a minimum hysteresis, $V_{LR(HYS)}$, of 100 mV to act as another protection against the device oscillating back and forth between low and high line.

The purpose of line range detection is that the controller modifies the gain of the internal digital compensator in order to optimize performance and operation of the PFC for universal, wide−input mains applications. Specifically, the loop gain of the digital compensator is reduced by a factor of 4 when the device detects that it is in the high line range.

AC Zero Crossing Management

AC zero crossing management is the feature in the NCP1680 that determines when to enable and disable the various drive signals at the beginning and end of each of the half line cycles. This feature is critical to the robustness and performance of the Totem pole topology. The NCP1680 features 6 drive signals that can be divided into three classes:

1. The primary or duty−cycle controlled PWM drive signal.
2. The synchronous (sync) PWM drive signal that occurs during the (1 − d) portion of the switching period.
3. The slow leg “rectifier” or SR drive signal that switches once per half line cycle.

Each drive signal has a respective stop and start threshold, which is a function of the line voltage amplitude, V_{LINE}, where $V_{LINE} = |V_{LVSNS1} - V_{LVSNS2}|$ as previously mentioned.

Figure 15 illustrates the zero crossing management thresholds for the primary PWM drive, denoted as PWMd. The same stop and start principle applies to the Synchronous PWM and SR drives, although with different thresholds.

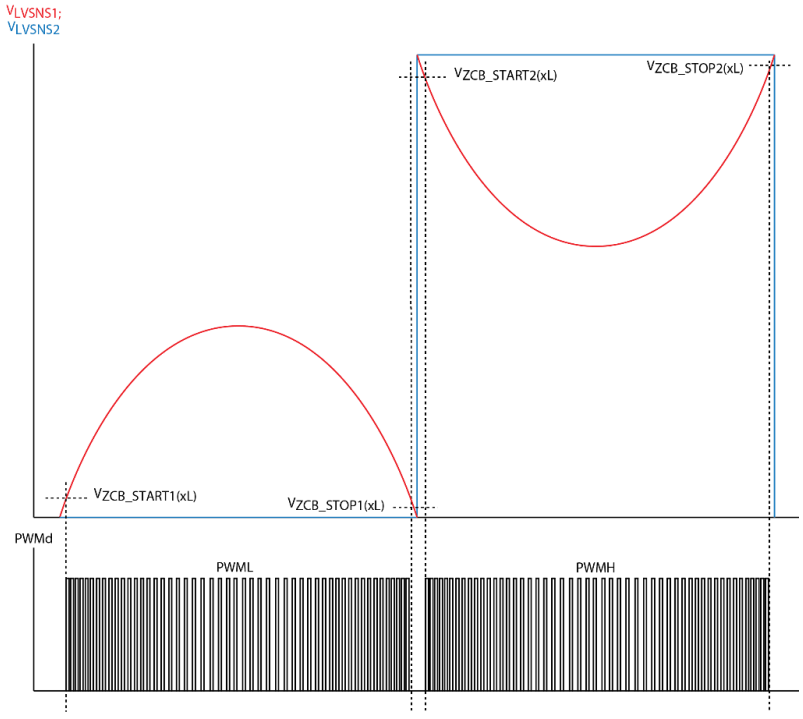


Figure 15. AC Zero Crossing Management Thresholds

Figure 15 shows a full AC line cycle beginning with a positive half−line cycle, i.e. conduction angle between 0° to 180°. In the positive half−line cycle the voltage at the LVSNS2 pin is pulled to 0 V and the voltage at LVSNS1 is increasing proportional to the AC line amplitude. When the AC line amplitude exceeds the threshold $V_{ZCB\_START1(xL)}$, typically 120 mV, the controller begins issuing drive signals to the duty−controlled device, PWML in this case. As the conduction angle approaches 180°, V_{LINE} will eventually fall below the $V_{ZCB\_STOP1(xL)}$ threshold, typically 100 mV, and the controller will blank drive pulses to the duty−controlled device.

In the negative half line cycle the zero crossing management works largely the same as positive half line cycle with the controller processing the different LVSNS signals that are unique to negative half line cycle operation. In this half line cycle LVSNS2 is pulled up to a voltage proportional to about 1% of the PFC bulk voltage, and the LVSNS1 decreases in amplitude relative to the controller GND pin, but increases in amplitude relative to the LVSNS2 signal. The controller's differential line sensing reconstructs $V_{LINE} = |V_{LVSNS1} - V_{LVSNS2}|$ so that V_{LINE} is symmetrical in positive and negative half line cycle and the zero crossing management can use the same comparison thresholds for both half line cycles. The $V_{ZCB\_START2(xL)}$ threshold is 120 mV, and the $V_{ZCB\_STOP2(xL)}$ threshold is 100 mV, same as the start and stop thresholds in positive half line cycle, ensuring that the zero crossing management is symmetric across a full AC line cycle.

Zero crossing management of the synchronous PWM and SR drives follows the same principle as that used to manage the primary PWM drive, however the thresholds are higher as the primary PWM switches for a greater portion of the half line cycle. For the slow leg SR drive, $V_{SR\_START1(xL)}$ is typically 200 mV and $V_{SR\_STOP1(xL)}$ is typically 180 mV and because operation is symmetric the start and stop thresholds in negative half line cycle are the same. For the sync drive, the start threshold, $V_{SYNC\_START1(xL)}$, is typically 220 mV and the stop threshold is typically 200 mV.

All of the thresholds in the AC zero crossing management block include hysteresis to ensure stable operation without repeated enabling and disabling should noise corrupt the LVSNS signals. Also, all of the drive signals are disabled before the AC line voltage reaches its true zero crossing. While this can lead to a small amount of increased zero crossing distortion, the benefit of disabling all drives is to create a quite environment to ensure the precision and robustness of the polarity signal which is critical to guarantee that the PWM and SR drive signals are directed to the proper device during the respective half line cycle.

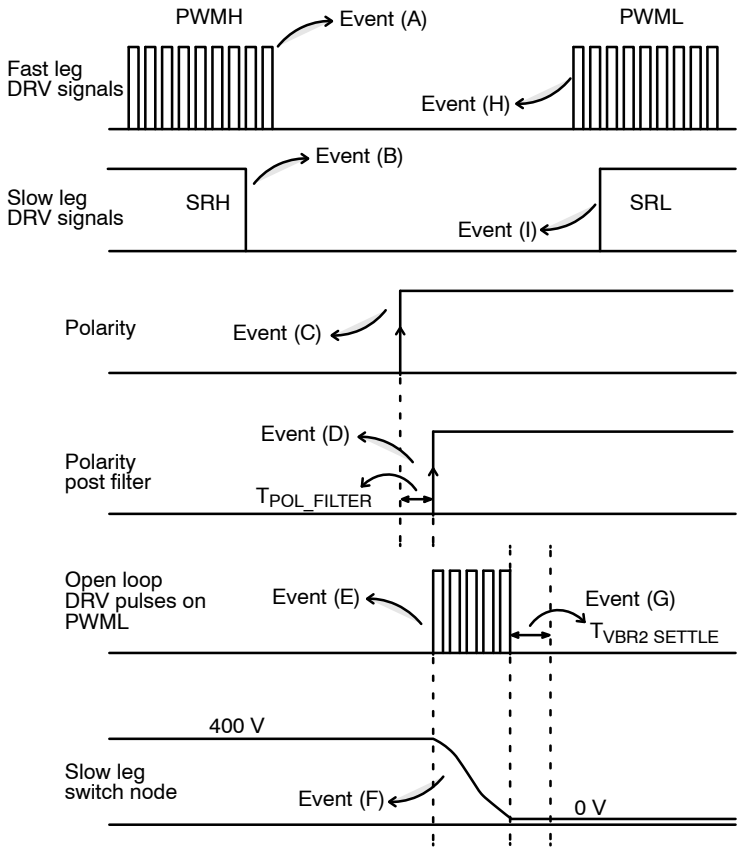
Open Loop Drive Pulses

Another critical feature of the NCP1680 is the open loop drive pulses that are issued immediately following a polarity transition. After the AC line zero crossing, the slow leg bridge maintains a residual voltage charge from the previous half line cycle and must be transitioned from V_{BULK} to 0 V (or vice versa) during the upcoming half line cycle. Considering that PWM−controlled drive pulses near an AC line zero crossing would typically operate with a high duty cycle, using these pulses to transition the slow bridge voltage can result in excessively high current spikes in the inductor; hence it is beneficial use shorter drive pulses with a smaller, fixed duty cycle to initiate the slow leg bridge node transition. The ON time of the main duty−controlled FET is gradually increased during this phase to assist the slow leg bridge node voltage in transitioning between the bulk voltage and ground. The OFF time of the main duty−controlled FET is also gradually increased during this phase to maintain the same duty ratio. During the open loop drive pulses the slow leg drive and (1−d) drives are held at 0. The duration and period of the open loop drive pulses is captured in Table 4.

Table 4. OPEN LOOP DRIVE PULSES

	Ton (μs)	Toff (μs)	Period (μs)	
1st Pulse	1	4	5	
2nd Pulse	2	8	10	
3rd Pulse	3	12	15	
4th Pulse	4	16	20	
			50	total

Figure 16 provides an annotated timing diagram of a zero crossing transition including the open loop drive pulses. For simplicity, the sync PWM (1−D) drive signals are not shown in this figure.



Event (A) – When the sensed line voltage falls below $V_{ZCB\_STOP2(xL)}$, the "D" drive signal is disabled.

Event (B) – When the sensed line voltage falls below $V_{SR\_STOP2(xL)}$, the slow leg drive signal is disabled. Note that Event (B) occurs before Event (A).

Event (C) – The two sense nodes cross over, representing the actual AC phase reversal instant.

Event (D) – The polarity edge after the filter.

Event (E) – Open Loop Drive pulses issued on the low side (PWML) drive during the negative to positive half line cycle transition or on the high side (PWMH) drive during the positive to negative half line cycle transition.

Event (F) – The open loop drive pulses assist the slow leg switch node transition from 400 V to 0 V or from 0 V to 400 V.

Event (G) – Settling of the slow leg switch node voltage.

Event (H) – Fast leg drive (PWML) is enabled if the line voltage exceeds $V_{ZCB\_START1(xL)}$

Event (I) – Low side slow leg (SRL) is enabled if the line voltage exceeds $V_{SR\_START(xL)}$.

Figure 16. AC Zero Crossing Timing Diagram

Operating Modes

The NCP1680 achieves power factor correction by operating in a Frequency Clamped Critical Conduction Mode (FCCrM). An illustration of FCCrM operation is shown in Figure 17. In FCCrM the controller operates in critical conduction mode (CrM) at higher load levels where the peak inductor current is high, and the switching frequency is slower. As the load level decreases the peak inductor current decreases which naturally forces the application to operate at higher switching frequencies. The switching frequency will continue to increase until a maximum frequency clamp, F_{CLAMP}, is reached, after which the controller transitions into a discontinuous conduction mode (DCM) of operation. F_{CLAMP} is 130 kHz for the NCP1680AA and 275 kHz for the NCP1680AB and NCP1680AC.

Once in DCM the switching frequency will decrease, gradually, as the load decreases. The frequency reduction in DCM is achieved by a novel ramp modulation circuit that forces longer switching periods, and more resonant valleys as the load is decreasing. While in DCM the controller mitigates against hard switching operation by continuously tracking the resonant valleys and always beginning a new switching cycle during a valley as shown in Figure 17. As the load decreases towards 0, the controller clamps the switching frequency to a minimum, F_{MIN}, typically ~ 30 kHz, to mitigate audible noise.

Note that frequency−clamped operation is controlled by novel circuitry which modulates the on−time and switching period on a cycle−by−cycle basis to prevent any discontinuity in operation and ensure proper current shaping. Within any AC half−line cycle of operation, the circuit can readily transition between CrM and DCM, often operating in DCM near the AC line zero crossings and in CrM at the peak of the AC line as the inductor currents are larger, forcing lower switching frequencies. These transitions between CrM and DCM should occur seamlessly, causing no discontinuity or oscillation in the operation.

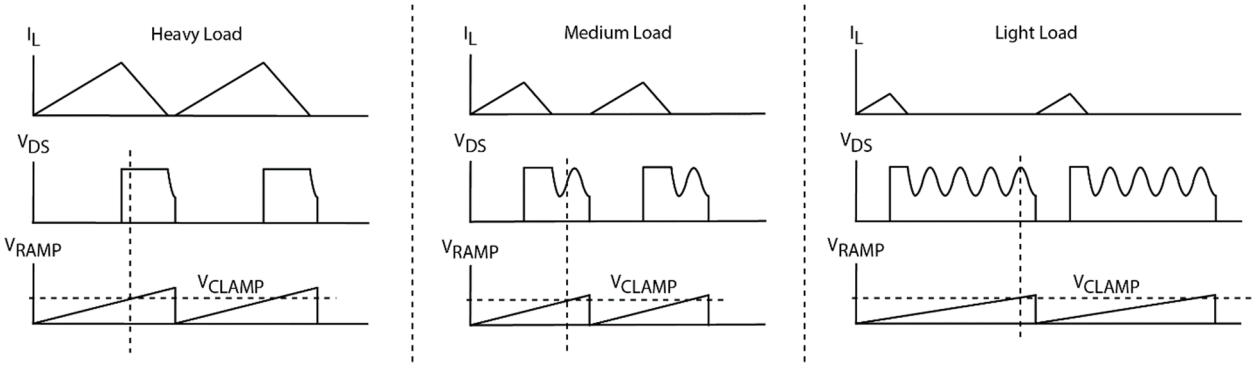


Figure 17. FCCrM Operating Modes

On Time Modulation Block

The NCP1680 operates with a constant on−time control algorithm. The on−time of the main PWM switch is controlled by the compensation voltage and a modulating ramp as shown in Figure 18.

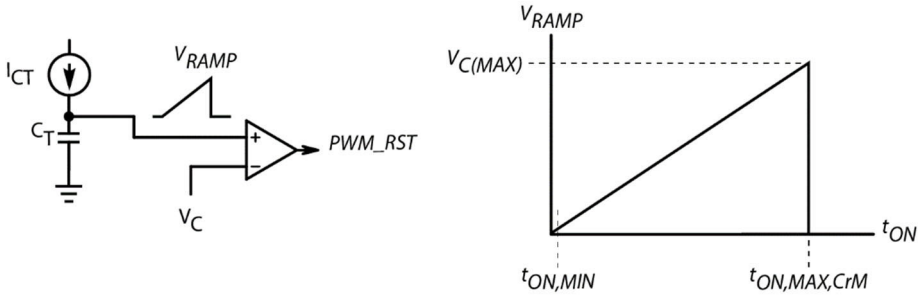


Figure 18. On Time Modulation

The circuitry for the on time modulator is internal to the NCP1680; the compensation voltage is generated by the internal digital compensator and translated into the analog domain, and the timing components for the modulator ramp are also internal. In CrM the slope of the modulating ramp is fixed and the maximum on time, $T_{on,max,CrM}$, occurs when the compensation voltage has railed to $V_{C(MAX)}$ of 4.2 V. The different available NCP1680 devices have different on time capabilities and are tuned to operate with different inductance values. Equation 1 can be used to approximate the maximum allowable inductor value for the respective devices given the estimated system efficiency (η), minimum AC line voltage, and the maximum output power requirements of the application.

$$L < \frac{\eta \cdot V_{ac}^{2} \cdot T_{on,\,max,\,CrM}}{2 \cdot P_{o}} \qquad \text{(eq. 1)}$$

As long as the application remains in CrM operation the average input current to the PFC is approximately equal to half of the peak inductor current, i.e. $I_{in} = \frac{I_{L,PK}}{2}$, and a modulating ramp with a fixed slope will continue to achieve good power factor. However, when the application transitions to DCM operation the inductor current remains at zero for some portion of the switching cycle and the input current will begin to distort unless that portion of the switching cycle is compensated out. Figure 19 shows a sample inductor current in DCM operation and the associated dead time that occurs prior to the next drive pulse.

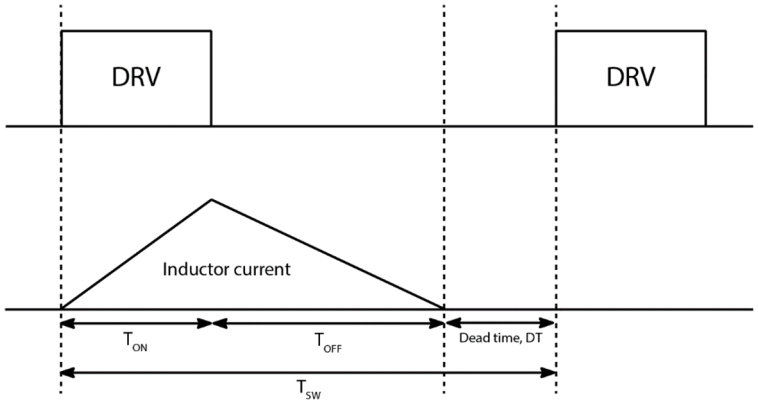


Figure 19. DCM Operation and Dead Time Compensation

In DCM the average input current is now a function of the dead time, specifically $I_{in} = \frac{I_{L,PK}}{2} \cdot \frac{T_{ON} + T_{OFF}}{T_{SW}}$, and the input current will begin to distort if the on−time generator continues using a modulating ramp with a fixed slope. The NCP1680 dead time compensation mitigates input current distortion, retaining good power factor across all operating modes, by adjusting the slope of the modulating ramp by a factor equal to $k_{DT} = \frac{T_{ON} + T_{OFF}}{T_{SW}}$. Multiplying the slope of the modulating ramp by a factor of k_{DT} increases the on−time inversely proportionally to k_{DT} compensating out the effects of the inductor current dead time and allowing the application to maintain good power factor performance across CrM and DCM operation.

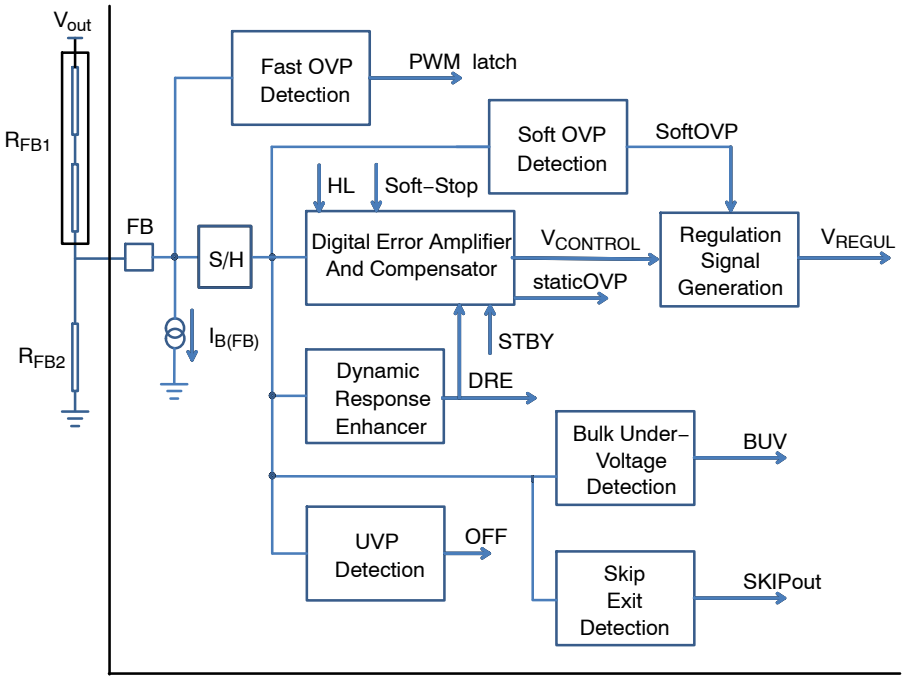


Figure 20. FB and Regulation Architecture

The general structure of the feedback and regulation architecture is shown in Figure 20. The bulk voltage is divided down via a resistor divider and input to a sample and hold circuit which passes the sensed voltage to the input of the error amplifier where it is compared against a 2.5 reference voltage.

The NCP1680 is internally compensated with a digital error amplifier and a control voltage ripple cancellation circuit. The “Digital Error Amplifier and Compensator” block performs the compensation generating the error voltage, $V_{CONTROL}$, and the “Regulation Signal Generation” block performs additional processing of the error voltage, including the ripple voltage cancellation, to generate the V_{REGUL} signal. Practically, in FFCrM operation the V_{REGUL} signal is the digital domain version of V_C signal from Figure 18 which dictates the on−time of the application.

The compensation in NCP1680 is equivalent to a Type−II analog compensator as shown in Figure 21 with the following component values: G_{OTA} = 200 μS, R_Z = 24 kΩ, C_Z = 4.62 μF, C_P = 97.24 nF. Based on these values the key characteristics of the compensator are the following:

- Mid−band gain = 20*log10(R_Z*G_{OTA}) = ~ 13.6 dB
- Compensation zero location = = 1/(2*π*R_Z*C_Z) = ~1.44 Hz
- High frequency pole location = = 1/(2*π*R_Z*C_P) = ~ 68.2 Hz

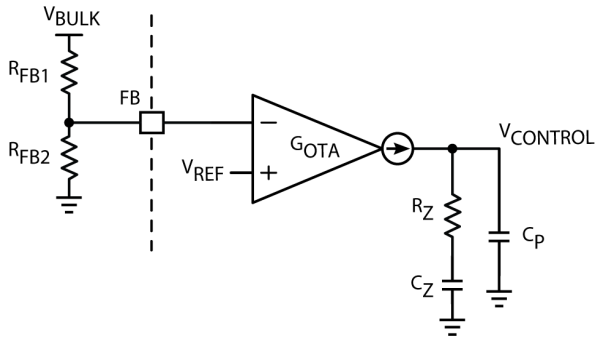


Figure 21. Equivalent Analog Compensator

This compensator provides greater than 50° of phase boost at 2 Hz, over 70° of phase boost between 5 to 10 Hz, and the mid−band gain measures at 13.4 dB. For most PFC applications, having a mid−band gain between 10 to 15 dB will ensure a loop crossover frequency in the range of 5 Hz to 10 Hz, hence the NCP1680 compensator is designed to satisfy a 5 Hz to 10 Hz loop bandwidth with > 60° of phase margin.

Additionally, the $V_{CONTROL}$ voltage is passed through an optional line frequency ripple cancellation circuit which is designed to eliminate the AC ripple present on the $V_{CONTROL}$ voltage. High amplitude AC ripple on the control voltage can increase harmonic distortion of the AC line current, hence the desire to eliminate this ripple component. However, a side effect of the ripple cancellation circuit is that it behaves as another filter in the control loop, degrading the phase boost provided by the compensator. Figure 22 provides a Bode plot of the transfer function from FB to V_{REGUL} including the effects of sampling, compensation, and ripple cancellation. The overall compensation loop is optimized for a crossover point of ~ 5 Hz where 60° phase margin can be achieved and bandwidths up to ~ 14 Hz can be designed with an acceptable 45° phase margin.

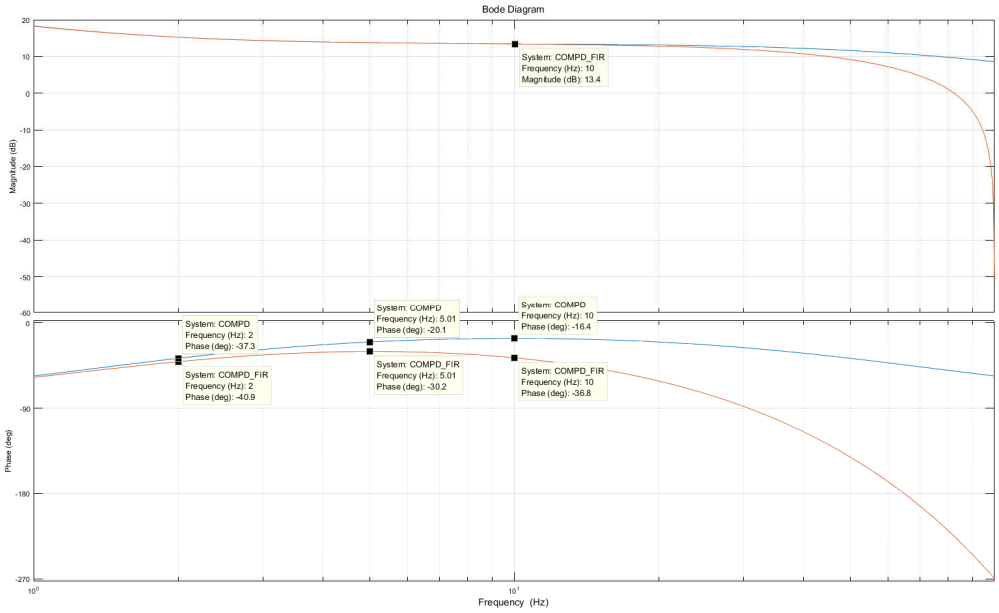


Figure 22. Bode Plots with Ripple Cancellation Filter

Output Voltage Protection Features

The NCP1680 features multiple protection and enhancement features for improved performance and robustness of the application. The soft OVP, UVP and DRE comparators monitor the sampled FB pin voltage. Based on the typical value of their parameters and if ($V_{out,nom}$) is the output voltage nominal value (e.g., 395 V), we can deduce the following levels:

- Output Regulation Level: $V_{out,\,nom} = \frac{V_{REF}}{k_{FB}}$
- Output soft OVP Level: $V_{out,\,SOVP} = 105\% \cdot V_{out,\,nom}$
- Output Fast OVP Level: $V_{out,\,FOVP} = 108\% \cdot V_{out,\,nom}$
- Output UVP Level: $V_{out,\,UVP} = 12\% \cdot V_{out,\,nom}$
- Output DRE Level: $V_{out,\,DRE} = 95.5\% \cdot V_{out,\,nom}$
- Output BUV Level: $V_{out,\,BUV} = \frac{V_{BUV}}{V_{REF}} \cdot V_{out,\,nom}$
- Output Upper Soft−SKIP Level: $\left(V_{out,\,softSKIP}\right)_H = V_{out,\,nom}$
- Output Lower Soft−SKIP Level: $\left(V_{out,\,softSKIP}\right)_L = 94\% \cdot V_{out,\,nom}$

V_{REF} is the regulation reference (2.5 V typically) and R_{FB1} and R_{FB2} are the feedback resistors per Figure 20; k_{FB} is the scale down factor of the feedback resistors $\left(k_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)$.

V_{BUV} is the internal threshold for the bulk under−voltage protection (BUV). Its typical value is 1.5 or 2 V, depending on the device variant. The BUV protection thus typically trips when the output voltage drops to 60% or 80% of its nominal level.

$\left(V_{out,\,softSKIP}\right)_H$ and $\left(V_{out,\,softSKIP}\right)_L$ are the levels between which the output voltage swings when in soft−SKIP mode (see the “Soft−SKIP Mode” section).

The soft−OVP trips when the feedback voltage exceeds 105% of V_{REF} and remains in this mode until V_{FB} drops below 103% of V_{REF}. When the soft−OVP trips, it reduces the power delivery down to zero in 4 steps as shown in Figure 23.

- Step 1: V_{REGUL} drops to 75% of the $V_{CONTROL}$ value for 100 µs
- Step 2: V_{REGUL} drops to 50% of the $V_{CONTROL}$ value for 100 µs
- Step 3: V_{REGUL} drops to 25% of the $V_{CONTROL}$ value for 100 µs
- Step 4: V_{REGUL} drops to 0 until the soft−OVP fault is over, that is, when the output voltage drops below 103% of its regulation level

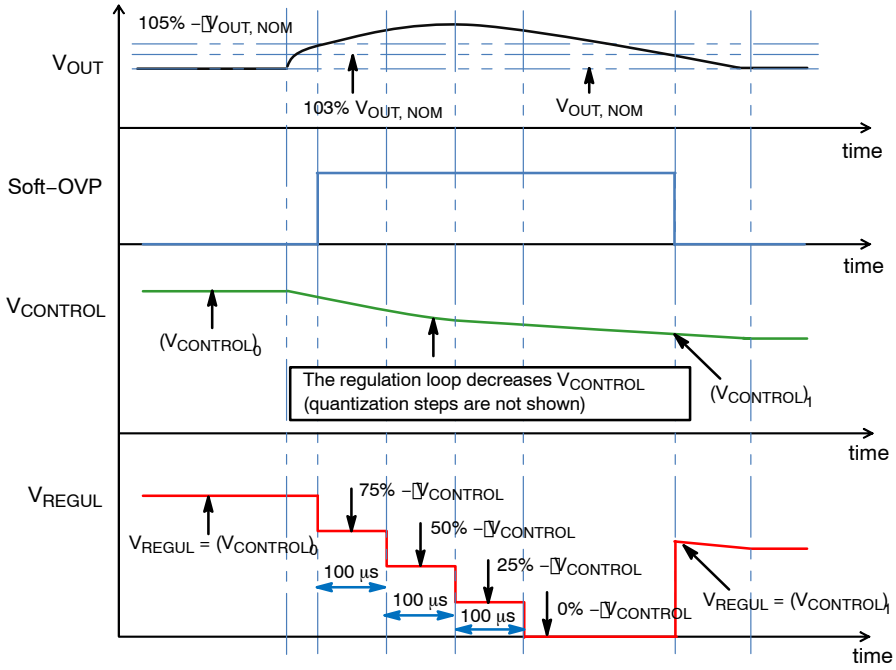


Figure 23. Soft−OVP Timing Diagram

The fast OVP comparator is analog and directly monitors the feedback pin voltage for immediate blanking of the drive pulses. The Fast OVP comparator trips when the feedback voltage exceeds 108% of V_{REF} and does not allow drive pulses until the feedback voltage falls below 103% of V_{REF}.

The dynamic response enhancer circuit functions to firmly contain undershoot of the output by increasing the gain of the control loop in response to the bulk voltage falling below a percentage of the desired regulation voltage. Practically when the FB pin voltage falls below 95.5% of V_{REF}, the DRE speeds up the charge of the compensation network until the FB pin voltage exceeds 98% of V_{REF}.

The FB pin also features a small 250 nA sink current for protection against an open FB pin, in which case V_{FB} will be pulled below the V_{UVP} (300 mV typically) threshold tripping the UVP protection. The UVP feature further works as a protection in the case of a FB pin that is shorted to GND.

AUXILIARY WINDING AND VALLEY DETECTION BLOCK

The TPFC topology presents a unique challenge to the use of an auxiliary winding for valley detection. Unlike the classical bridged CrM boost PFC, the TPFC operates differently in the positive and negative AC line cycles. The PWM−controlled switch changes from the low side switch to the high side switch, the inductor current changes from 1st to 3rd quadrant operation, and the "valley" of the switch node does not always occur when the auxiliary winding voltage approaches zero. Specifically, in negative half line cycle, the "valley" is really a peak and the desired turn−on of the PWM switch occurs when the switch node voltage is approaching the bulk voltage. This is illustrated in Figure 24 where the switch node voltage is depicted in both positive and negative half line cycles.

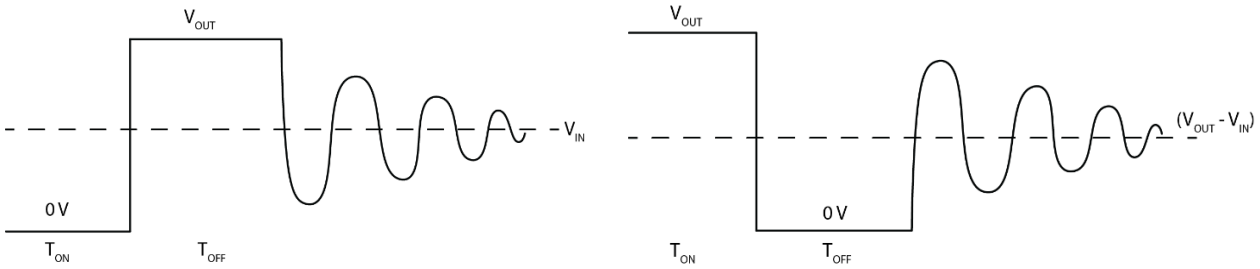


Figure 24. Switch Node Voltage in Positive (Left) and Negative (Right) Half Line Cycles

To adapt to the changing operation of the TPFC, while maintaining the use of a single low−cost auxiliary winding, the NCP1680 implements a novel "valley" sensing scheme combining edge detection with threshold detection. The NCP1680 accomplishes this by changing the "Arming" and "Triggering" thresholds depending on the polarity of the AC line. During positive half line cycle, the valley detection arms when the aux voltage goes above 200 mV, and triggers when the aux voltage falls below 100 mV. During negative half line cycle the opposite occurs, namely the valley detection arms when the aux voltage goes below 100 mV and triggers when the aux voltage comes back above 200 mV. By reusing the same comparators and thresholds, and only changing the function of the thresholds, the NCP1680 effectively combines edge and threshold detection to achieve a robust, low−cost solution that overcomes the bidirectional operation of the TPFC.

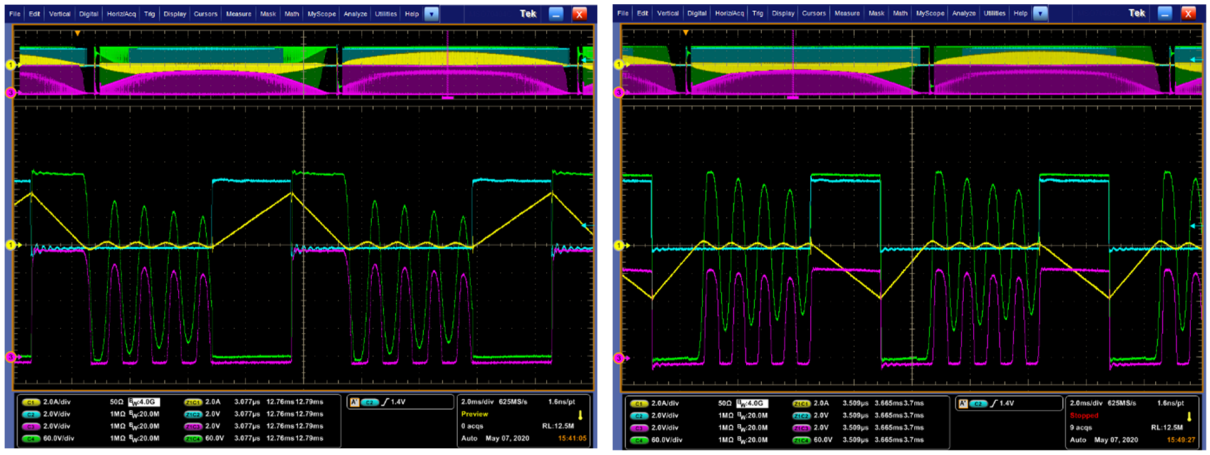


Figure 25. Valley Detection in DCM. Positive Line Cycle on Left, Negative on Right

Figure 25 shows waveforms demonstrating the valley detection implementation of the NCP1680 in DCM operation. The waveforms show the switch node voltage (Ch.4) and the auxiliary winding voltage (Ch.3) as its image traversing through 5 valleys before the respective PWM signal sets high. In both positive and negative half line cycle the turn on occurs on the correct edge of the auxiliary winding voltage.

Figure 26 is an example of valley detection in CrM operation. The switch node voltage is again shown on channel 4 and although there is no image of the auxiliary winding voltage, it can be seen that the turn−on of the PWML (Ch.2) on the left, and PWMH (Ch.3) on the right are coordinated to the “valley” of the switch node enabling very low turn−on voltage for optimized efficiency.

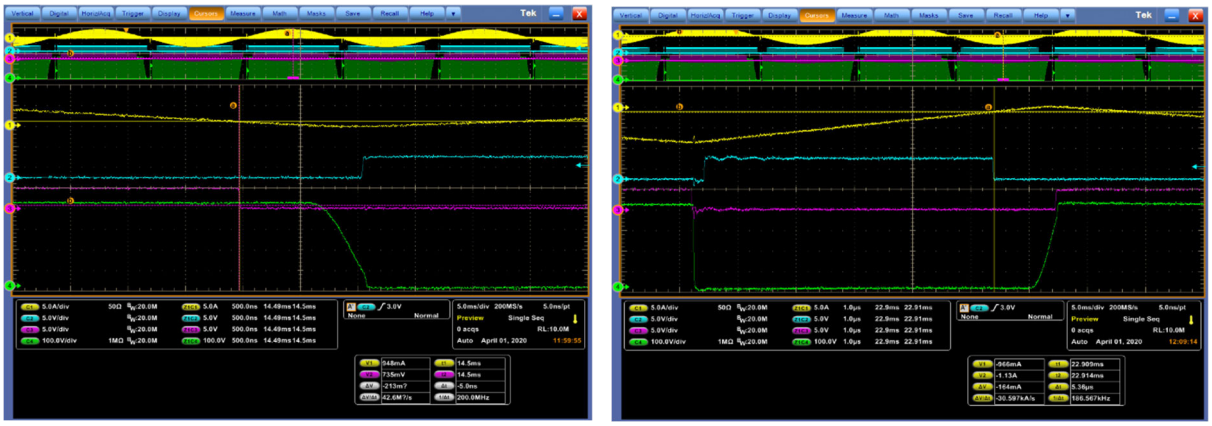


Figure 26. Valley Detection in CrM. Positive Half Line Cycle on Left, Negative on Right

The recommended auxiliary winding connection is shown in Figure 27. To optimize the symmetry of the valley detection between positive and negative half line cycles, a resistance, R_{AUX1}, with no series blocking diode is recommended between the auxiliary winding and the AUX pin. A pulldown resistance at the pin, R_{AUX2}, helps divert current to ground when the auxiliary winding voltage swings high, reducing the current into the ESD protection of the valley detect circuit. A Schottky diode, D_{AUX}, is recommended to protect the AUX pin voltage from going too far below ground when the auxiliary winding voltage goes negative. Finally, a capacitor to ground, C_{AUX}, can be used to tune the valley detection for optimizing valley switching and efficiency in the fast leg.

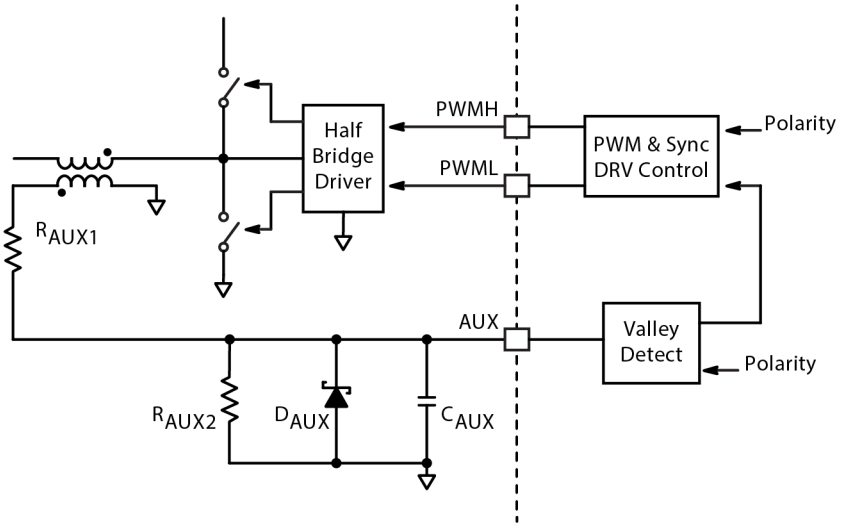


Figure 27. Recommended Auxiliary Winding Circuit

Zero Current Detection Block

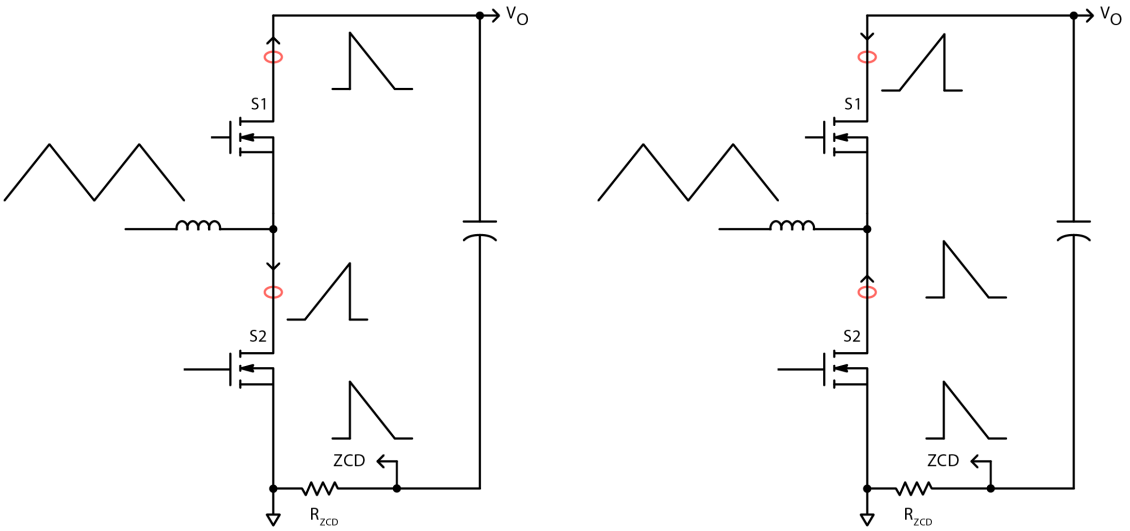


Figure 28. Zero Current Detection in Positive and Negative Half Line Cycle

The zero current detection feature utilizes a series sensing element to detect the inductor discharge current that flows to the load during the 1−D period of the switching cycle. This is shown in Figure 28. During the PWM on−time the current follows a different path through a different switch when in positive half line cycle as compared to negative half line cycle, however the inductor discharge current is consistently observable, regardless of the AC line conduction angle, in the return path from the bulk capacitor to the half bridge switching cell. A series element such as a current sense resistor or current transformer placed in this return path allows the controller to sense a portion of the inductor current and take action to control the (1−D) transistor, enable some form of peak current limiting in the application, and also enhancing THD performance.

Synchronous PWM Drive Control

The synchronous PWM or (1−D) device in the TPFC topology enables higher efficiency performance but proper gating of the device is necessary for optimizing efficiency and ensuring robustness in the application. A diagram of the sync control methodology is shown in Figure 29. First, the NCP1680 employs a dead time, T_{DT1}, typically 130 ns, following the falling edge of the PWM duty−controlled drive to prevent cross conduction. After the dead time has expired the controller looks for the ZCD voltage to exceed the $V_{ZCD(ARM)}$ threshold to enable the sync drive. In lighter loads, the ZCD voltage may never exceed this $V_{ZCD(ARM)}$ threshold and the sync device will never enable. This is done to prevent switching of the sync device at light loads where the associated switching losses could negatively impact the overall efficiency of the application.

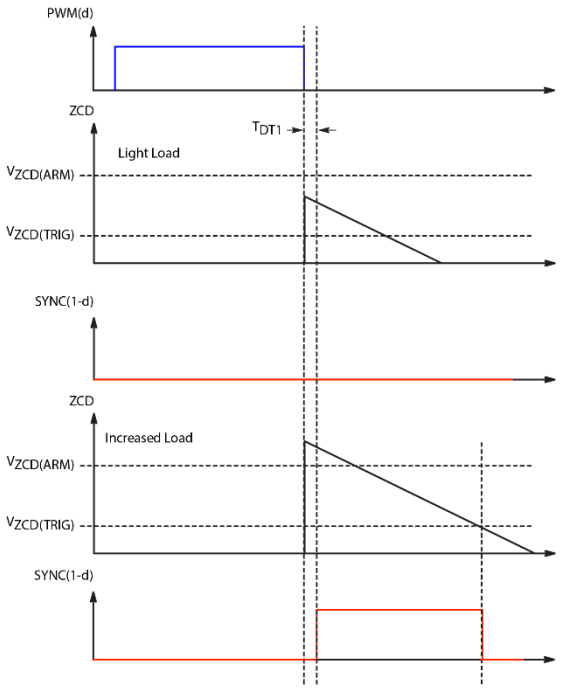


Figure 29. Synchronous PWM Drive Control

At increasing loads the ZCD voltage will exceed the arming threshold and the sync drive will remain enabled until the ZCD falls below the $V_{ZCD(TRIG)}$ threshold of 50 mV. The trigger threshold has been set close to 0 to keep the sync conduction period as long as possible but without letting the inductor current reverse polarity. Should the sync device remain on for too long the inductor current would

reverse polarity and begin cycling energy from the bulk capacitance. This would lead to increased RMS currents in the system and diminish overall efficiency.

The $V_{ZCD(TRIG)}$ threshold also gates the turn−on of the subsequent PWM(d) pulse, regardless of whether the sync pulse was ever enabled. If the ZCD voltage is held above this threshold, the device blanks PWM pulses indefinitely. This feature is intended to reduce the stress of hard switching events at power up of the application when the peak of the AC line voltage and the bulk voltage are approximately equal. It is also beneficial in the case of differential line surge events where the AC mains can peak charge the bulk capacitor. In the event of a surge, if there is current flowing to the bulk capacitor this will be detected by the NCP1680 through the ZCD resistor, and the controller will disable PWM(d) pulses until the surge event subsides.

Summarizing, the sync (1−D) pulses are gated by the following criteria:

- A delay, t_{DT1}, of 125 ns (typical) after the PWM(d) turn−off – This prevents cross conduction
- ZCD voltage crosses the $V_{ZCD(ARM)}$ threshold – This ensures sync pulses are enabled only at higher loads for efficiency improvement across all load conditions
- V_{LINE} voltage crossing 220 mV which is 22 V on the AC line with a 100:1 divider – This avoids premature enabling of the sync pulses and enhances efficiency
- PFCOK sets high – To avoid reverse currents during startup

Overload and Peak Current Limit Protection

Overload and peak current limiting are necessary features in any application to protect the system from destructive damage due to either overcurrent or excessive thermal stress. The NCP1680 features a novel protection algorithm which utilizes the inductor discharge current detected through the ZCD sensing element. A circuit representation of the algorithm is shown in Figure 30. The ZCD voltage at the beginning of the (1−D) period is representative of the peak inductor current. The NCP1680 measures the time duration, ΔT_{OS}, that the ZCD voltage exceeds the $V_{ZCDLIM1}$ threshold and integrates the time duration into a voltage, ΔV_{OS}. This voltage is then subtracted from a 5 V rail and the difference becomes the threshold for the ZCD current limit comparator. Higher peak currents result in longer time durations and hence lower thresholds for the ZCD current limit comparator.

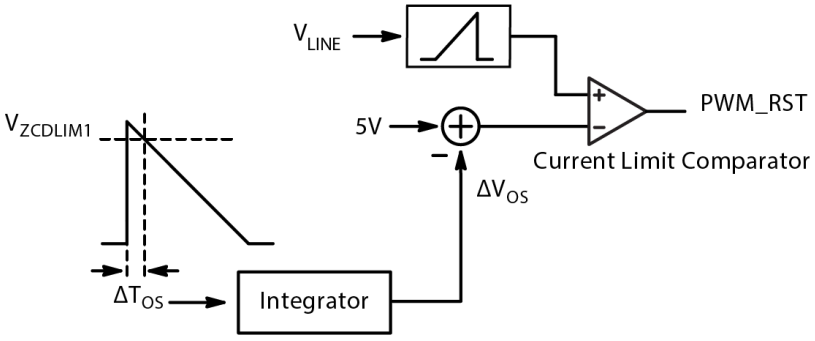


Figure 30. ZCD Current Limit Schematic

The noninverting input of the current limit comparator is fed a ramp voltage, different than the modulating ramp used for the PWM on−time control. The ramp in the current limit circuit has a slope proportional to the instantaneous line voltage, hence as the AC line voltage increases the current limit ramp becomes faster allowing the current limit circuit to produce shorter on times at higher line voltages. The ramp characteristics and maximum allowable on times is shown in Table 5. This novel current limit scheme eliminates the need for Hall effect sensors and current sense transformers, thereby significantly reducing the system BOM cost.

Table 5. CURRENT LIMIT CHARACTERISTICS

V_{ac}	$V_{ac, PK}$	$V_{LINE, PK}$	Ramp Slope [V/μs]	$T_{ON,MAX}$ [μs]
85	120.2	1.20	0.246	20.34
115	162.6	1.63	0.333	15.04
230	325.3	3.25	0.909	5.50
265	374.8	3.75	1.048	4.77

ZCD Resistor Calculation

To calculate the ZCD resistor value one must first calculate the maximum peak inductor current in the application using Equation 2. The maximum inductor current is determined by maximum output power, minimum AC input voltage, and an estimate of the application efficiency, η. Once the maximum peak current is determined, Equation 3 is used to find an upper limit on the ZCD resistor based on the ZCD current limit threshold, $V_{ZCDLIM(xL)}$). Typically this calculation is only needed at the minimum AC voltage, usually 90 V_{AC}, however the calculation should also be repeated at the minimum high line voltage in the application because the NCP1680 has an optional 60% reduction of the ZCD current limit at high line to provide power limiting at high line.

$$I_{L,PK} = \frac{2\sqrt{2} \cdot P_O}{\eta \cdot V_{ac}} \quad \text{(eq. 2)}$$

$$R_{ZCD} < \frac{V_{ZCDLIM(xL)}}{I_{L,PK}} \quad \text{(eq. 3)}$$

THD Enhancer

Another feature of the NCP1680 that is derived from the ZCD voltage is the THD enhancer, which produces a small on−time extension proportional to the time duration that the ZCD voltage is less than the $V_{ZCD(MIN)}$ threshold. This is shown in Figure 31 where the orange square represents the time duration that the THD enhancer integrates to produce an on−time extension. Typically, at lighter loads and near the AC zero crossings the amplitude of the inductor current reduces and the ZCD voltage will spend longer durations below this minimum threshold resulting in larger on−time extensions. Note that the THD enhancer does not compensate for the dead time period shown in Figure 31 as this is handled by the dead time compensation circuit. The THD enhancer working in conjunction with the dead time compensation circuit allows the NCP1680 to achieve THD <10% at medium to heavy loads across the universal input range.

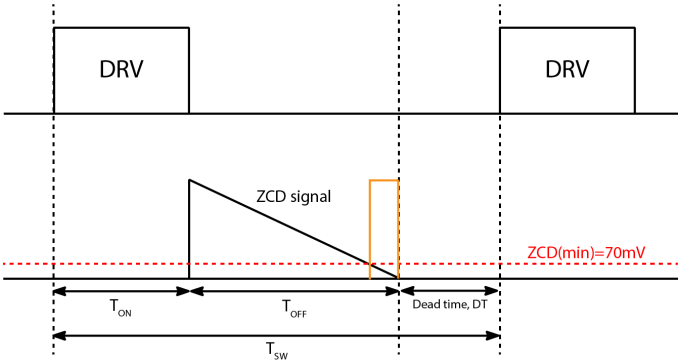


Figure 31. ZCD THD Enhancer Diagram

Soft Skip Mode

The NCP1680 features a Soft Skip mode which enables the application to achieve very good no load and light load performance. The device must be externally commanded to enter the Skip mode by pulsing of either the PFCOK or $\overline{SKIP}$ pins. When the device enters the Skip mode, it sheds much of its functionality except for FB and V_{CC} monitoring, and the internal consumption of the device is reduced to I_{CC4}, typically 540 μA. While in Skip mode the output voltage decays to 94% of the regulation voltage allowing for a long period, sometimes up to 1 minute, of inactivity. When the output voltage reaches 94% of its nominal value, the device exists Skip mode for a brief burst period during which drives are enabled and the output voltage is pushed back up to the nominal regulation value. Provided that the NCP1680 continues to receive Skip command pulses from an external source, the device will continue to operate in this Skip−burst−skip mode indefinitely. A timing diagram of the Skip operation is shown in Figure 32.

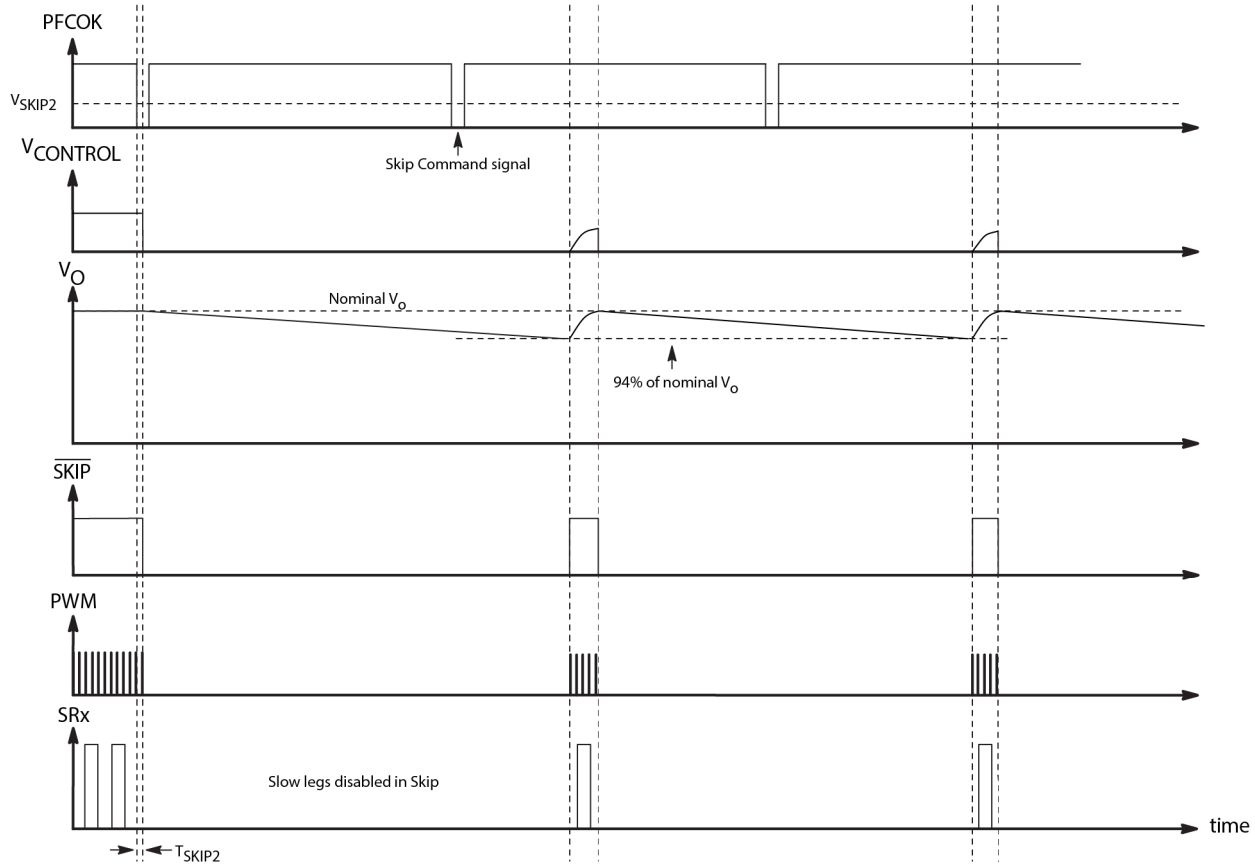


Figure 32. Skip Operation Timing Diagram

Skip Command Pulses

The command pulses needed to force the NCP1680 into skip can be delivered to either the $\overline{\text{Skip}}$ or the PFCOK pin. A schematic and timing diagram for $\overline{\text{Skip}}$ is shown in Figure 33. To command the NCP1680 into the skip mode an external pulldown signal must be applied to the pin. The signal can be applied directly or through a diode if the pulldown signal exceeds the 5 V absolute maximum rating of the pin. The pulldown must overcome the current sourcing capability of the pin, $I_{\overline{SKIP}}$, typically 700 μA, in order to pull the pin below the $V_{SKIP(th)}$ voltage of 1.5 V. The pin voltage is filtered by a minimum 56 μs filter preventing false skip commands in the event of a noisy environment. One the device enters the skip mode the $\overline{\text{Skip}}$ output buffer is turned off to minimize current consumption in the controller. The NCP1680 also starts a recovery timer, typically 500 ms, and enables the $\overline{\text{Skip}}$ output buffer for a 400 μs window every 500 ms to check whether the external pulldown signal is still commanding the device into skip mode. If the device detects that the external pulldown has been disabled within the 400 μs window then the device will exit the skip mode and resume normal operation.

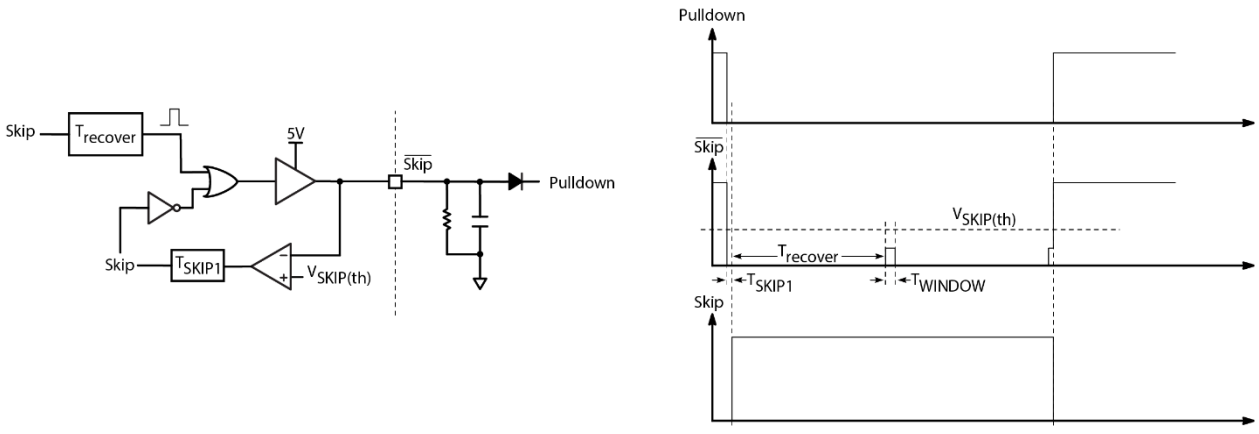


Figure 33. $\overline{\text{Skip}}$ Schematic and Timing Diagram

The $\overline{\text{Skip}}$ pin can also be utilized, along with some external circuitry, to further optimize the no load performance of the application. Many external gate driver circuits such as the NCP51820 have an Enable/Disable input that can be toggled to bring the respective device into a low consumption state. The $\overline{\text{Skip}}$ pin, which is a 0 to 5 V signal can be used to control the external driver by directly connecting the pin to the Enable pin of the driver. A small RC resistor at the enable pin is recommended for decoupling.

For gate driver circuits that do not have an Enable/Disable pin, such as the NCP51530 or the NCP5183, which can be used to drive the slow leg transistors, a V_{CC} pass−through circuit can be used to disable the drivers when the NCP1680 is in the Skip mode. An example pass−through circuit is shown in Figure 34 where the $\overline{\text{Skip}}$ pin directly drives a smaller signal NMOS transistor. When the NMOS is conducting, current is pulled from the base of the PNP transistor allowing it to conduct so that $V_{CC1} = V_{CC}$. In skip mode the $\overline{\text{Skip}}$ pin will pull low shutting off both NMOS and the PNP pass transistor.

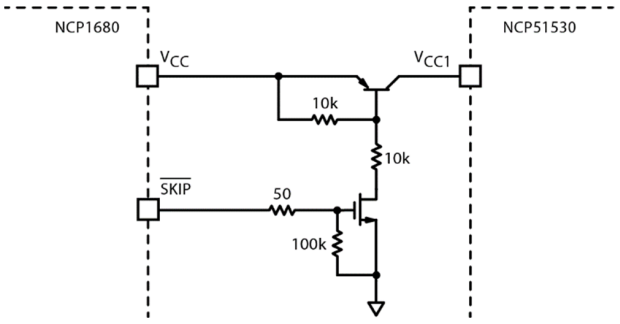


Figure 34. V_{CC} Pass−Through Circuit

The PFCOK pin is typically utilized for communication to a downstream converter, acting as an enable or UVLO. In this case it may be necessary for the PFCOK pin to remain high during the skip mode so that the downstream converter does not shutdown. For that reason, the command pulse logic for the PFCOK pin is optimized for a pulse train, rather than for a pulldown to ground like the $\overline{\text{Skip}}$ pin. For the NCP1680 to enter skip mode the PFCOK pin must be pulled below the $V_{SKIP2(th)}$, typically 0.5 V, for a duration greater than T_{SKIP2}, typically 30 μs. The frequency of the PFCOK pulse train needs to be faster than the burst frequency of the PFC. Figure 35 shows a sample schematic and timing diagram for the interface between the downstream converter and the PFCOK pin of the NCP1680.

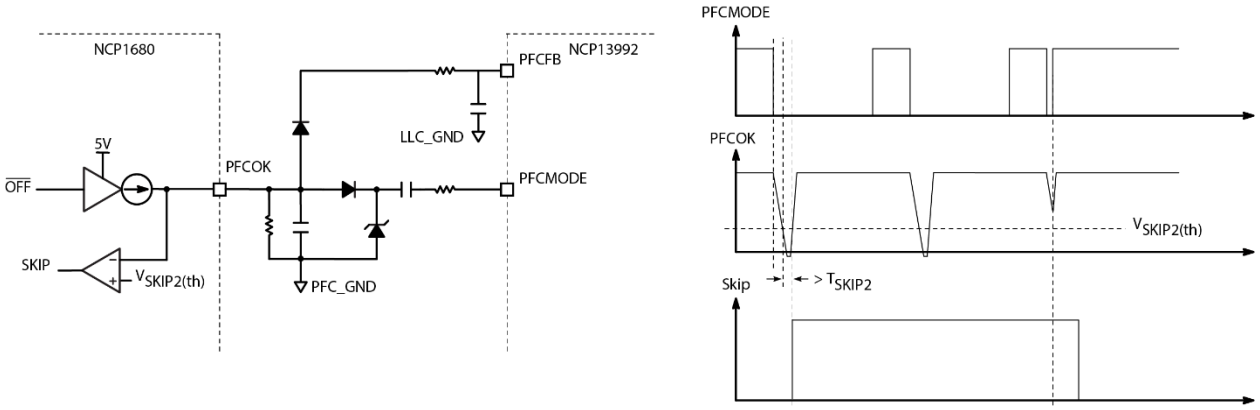


Figure 35. PFCOK Schematic and Timing Diagram

PFCOK Operation

The PFCOK pin is intended to control operation of a downstream DC−DC converter by acting as an enable or UVLO signal. The pin output is high when the application is in nominal operation and low when the application is in startup or when the device detects a fault condition. The output of the pin is a current source proportional to the FB pin voltage with a gain of 10 μA/V. A resistor to ground placed at the pin will give the downstream converter an image of the bulk voltage for use as a UVLO or as a logic enable.

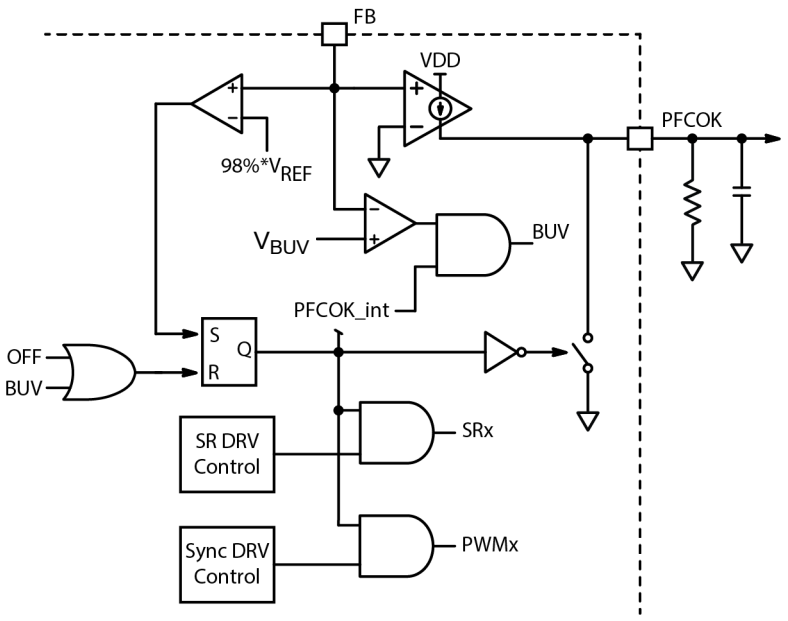


Figure 36. PFCOK Schematic

A logic diagram detailing the PFCOK pin operation is shown in Figure 36. Worth noting is that at startup of the application the PFCOK pin remains pulled to ground until the V_{FB} voltage reaches 98% of V_{REF}. Once the FB voltage exceeds 98% of V_{REF} the internal PFCOK flag goes high which enables the sync PWM and slow leg SR drive pulses. Sync PWM and slow leg SR pulses are also gated by other criteria but prior to achieving regulation, they are completely disabled. The PFCOK flag also gates skip mode operation and the bulk undervoltage (BUV) fault so that the device is unable to enter skip mode or declare a BUV fault until having first achieved regulation.

Fault Pin and Fault Matrix

Fault Pin

The NCP1680 includes a dedicated fault input accessible via the Fault pin. The controller can be latched off by pulling the pin up above the upper fault threshold, $V_{FLT(OVP)}$, typically 3.0 V. The controller is disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{FLT(OTP)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 37 shows the architecture of the Fault input.

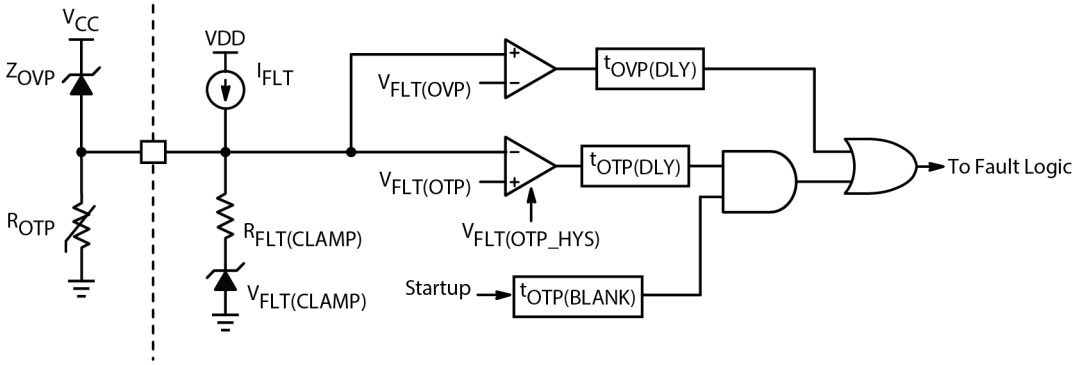


Figure 37. Fault Pin Schematic

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source I_{FLT}, (typically 46 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{FLT(OTP)}$. The OTP fault is an auto−recoverable fault so the NCP1680 will enable switching once the fault pin voltage exceeds the $V_{FLT(REC)}$ threshold, typically 0.92 V. The OTP fault also includes a 5 ms blanking circuit, $t_{OTP(BLANK)}$, which prevents the OTP fault from being asserted when the device first powers up. The blanking period is needed to allow any external pin capacitance to be charged up above the OTP threshold.

A clamp circuit prevents the Fault pin voltage from reaching the upper latch threshold if the pin is left open. To reach the upper threshold, the external pull−up current must be higher than the pull−down capability of the clamp (set by $R_{FLT(CLAMP)}$ at $V_{FLT(CLAMP)}$. The upper fault threshold can be used for V_{CC} over−voltage protection in the application, particularly for protecting external gate drivers. The NCP1680 V_{CC} pin is rated for 30 V, however external devices used to drive either the fast of slow leg transistors often have V_{CC} pins rated only up to 20 V so a simple Zener diode connected between V_{CC} and the FAULT pin can protect those external devices. The controller is latched once V_{Fault} exceeds $V_{FLT(OVP)}$. Both of the Fault signals include internal filtering to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{OVP(DLY)}$ and $t_{OTP(DLY)}$ are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay. Some external capacitance is also recommended at the FAULT pin to provide additional noise immunity.

Fault Matrix

The NCP1680 has an extensive suite of fault handling capabilities designed to enable a robust application design utilizing the Totem Pole PFC topology. Although much of the fault handling has been described in some detail throughout the datasheet, Table 6 is provided as a Fault Handling Matrix summarizing all of the key protection features including the conditions needed to set the fault, reset the fault, and the specific action taken by the controller for the given fault.

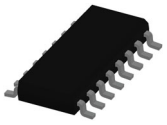
Table 6. NCP1680 FAULT HANDLING MATRIX

Fault	Set	Reset	Controller Action
Line SAG	(V_{LINE} < $V_{BO(STOP)}$) + $t_{SAG(blank)}$ expires	V_{LINE} > $V_{BO(START)}$	– Begin soft stop sequence – PWM and SR drives disabled after soft stop – PFCOK pulled low if StaticOVP or BUV (OFF Mode) –Cancels T_{BUV}
BO Fault	(V_{LINE} < $V_{BO(STOP)}$) + $t_{BO(blank)}$ expires	V_{LINE} > $V_{BO(START)}$	– Resets Controller – Polarity signal disabled – PFCOK pulled low if StaticOVP (OFF Mode)
Line Frequency 1	t_{LINE} < $t_{LINE(45)}$ or > $t_{LINE(65)}$	$t_{LINE(45)}$ < t_{LINE} < $t_{LINE(65)}$	– SR drives disabled – Starts $t_{LINEFREQ(DLY)}$ timer
Line Frequency 2	$T_{LINEFREQ(DLY)}$ timer expires	N_{DRV_EN} = 4 : $t_{LINE(45)}$ < t_{LINE} < $t_{LINE(65)}$ for 4 consecutive polarity toggles	– PWM Drive disables – Polarity signal remains active – PFCOK pulled low (OFFF Mode)
UVP	V_{FB} < V_{UVP}	V_{FB} > V_{UVP} + $V_{UVP(HYS)}$	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
Bulk Under – Voltage (BUV)	PFCOK high & (V_{FB} < V_{BUV})	T_{BUV} expires	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode) – Automatic restart after T_{BUV}
Soft OVP	V_{FB} > $V_{softOVP}$	V_{FB} < $V_{OVPrecover}$	– Begin soft OVP sequence – PWM Drive disables after soft OVP sequence – Polarity & SR remains active
Hard OVP	V_{FB} > $V_{hardOVP}$	V_{FB} < $V_{OVPrecover}$	– PWM Drive disables immediately – Polarity & SR remains active
V_{CC} UVLO	V_{CC} < $V_{CC(OFF)}$	V_{CC} > $V_{CC(ON)}$	– PWM and SR drives disabled – Polarity signal disabled – PFCOK pulled low (OFF Mode)
Fault OTP	$t_{OTP(BLANK)}$ expires + V_{FLT} < ($V_{FLT(OTP)}$ + $t_{OTP(DLY)}$)	V_{FLT} > $V_{FLT(REC)}$	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
Fault OVP	V_{FLT} > $V_{FLT(OVP)}$ + $t_{OVP(DLY)}$	Master Reset	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
TSD	T_J > T_{SHDN}	T_J < (T_{SHDN} − $T_{SHDN(HYS)}$)	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)

Table 7. ORDERING INFORMATION TABLE

OPN	$T_{ONMAX, CRM}$ (μs)	F_{CLAMP} (kHz)	$V_{ZCDILIM}$ (V)	$V_{ZCD(ARM)}$ (mV)	T_{POL_FILTER} (μs)	Package	Shipping†
NCP1680AA	17.2	130	1.4	300	200	SOIC16 (Pb−Free)	2500 / Tape & Reel
NCP1680AB	10.2	275	0.6	100	200		
NCP1680AC	10.2	275	0.6	100	50		

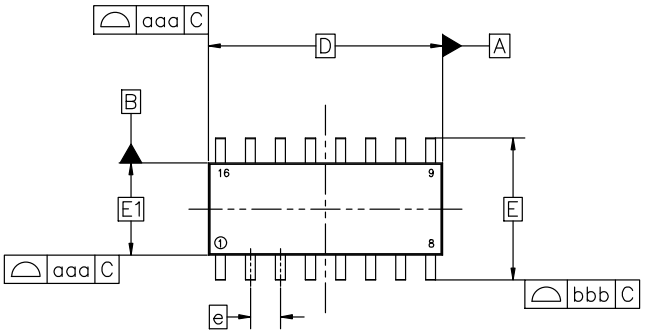
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



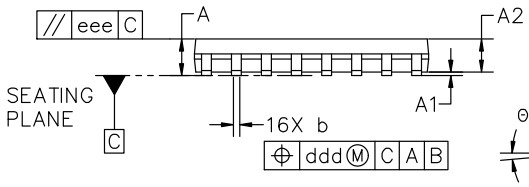
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

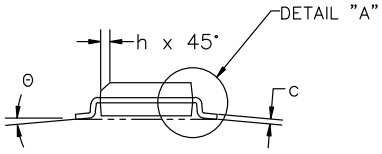
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



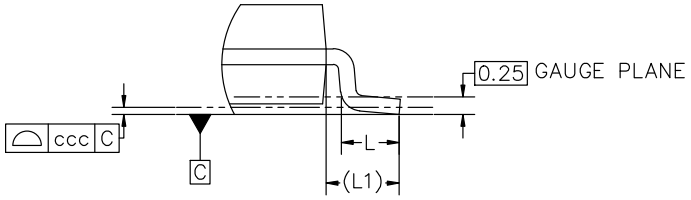
TOP VIEW



SIDE VIEW

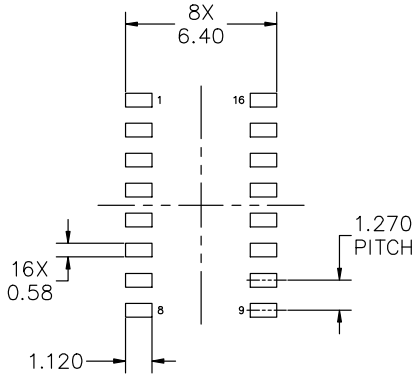


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

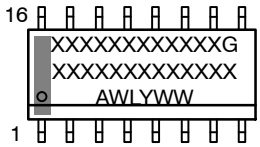
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales