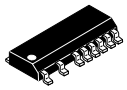
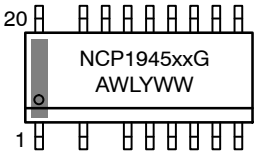
Combination Power Factor Correction and Quasi-Resonant Flyback Controllers for Adapters

NCP1945



SOIC20 NB LESS PINS 2, 4 & 19
Narrow Body
CASE 751BS

MARKING DIAGRAM



NCP1945	= Specific Device Code
xx	= AA, BA, FA, LA
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

The NCP1945 is a combination IC which integrates power factor correction (PFC) and quasi-resonant flyback functionality for designing high-performance off-line USB-PD and USB Type-C power converters.

The NCP1945 has optimized circuitry for a Boost PFC with features to ensure near-unity power factor while optimizing efficiency at all loads. The PFC operates in critical conduction mode (CrM) until the power drops below a threshold level at which time innovative Valley Synchronized Frequency Fold-back (VSFF) method is used. Using the VSFF the PFC stage enters the discontinuous conduction mode (DCM) with a dead-time which increases as the load decreases (frequency foldback) reducing switching losses.

The NCP1945 also supports a quasi-resonant (QR) current-mode flyback stage featuring proprietary valley-lockout circuitry to ensure stable valley switching down to the 6th valley, then transitions to frequency foldback mode to reduce switching losses. When the load decreases further, the NCP1945 QR section enters skip mode to manage the power delivery with special minimum peak current modulation circuitry. The minimum peak current modulation circuitry reduces the switching frequency quickly improving light load performance with high frequency designs. The QR circuitry automatically senses reflected output voltage and adjusts features or optimal performance including minimum peak current in light loads, current limiting circuitry to ensure a constant output current limit regardless of programmed output voltage, or nameplate output power.

To help ensure converter ruggedness, the NCP1945 implements several key protective features such as internal brownout detection, a non-dissipative Overpower Protection (OPP) for constant maximum output power regardless of input voltage, a latched over voltage and NTC-ready overtemperature protection through a dedicated pin, and line removal detection to safely discharge the X2 capacitors when the line is removed.

Features

- PFC: Follower Boost Capability
- PFC: Fast Line /Load Transient Compensation (Dynamic Response Enhancer)
- PFC: Adjustable Enable Threshold
- Integrated High-voltage Startup Circuit with Brownout Detection
- Integrated X2 Capacitor Discharge Capability
- Dual Range Vcc, with 150 V VccH Pin for Connection to High Voltage Aux Winding
- Primary Side Based Constant Output Current Limiting
- Latching or Auto-recovery Timer-Based Overload Protection
- Fault Pin for Severe Fault Conditions, NTC Compatible for OTP
- QR: Abnormal Overcurrent Fault Protection for Winding Short Circuit Detection
- QR: Valley Switching Operation with Valley-lockout for Noise-free Operation
- QR: Frequency Foldback with 25 kHz Minimum Frequency
- QR: Rapid Frequency Foldback for Fast Reduction of Switching Frequency
- QR: Frequency Jittering for Reduced EMI Signature
- QR: Adjustable Overpower Protection
- QR: Fixed Maximum Frequency Clamp in Power Excursion Mode (PEM)
- PONOFF Pin to Set the PFC Entry and Exit Point
- PEM Enables Use of Low Bulk Capacitance

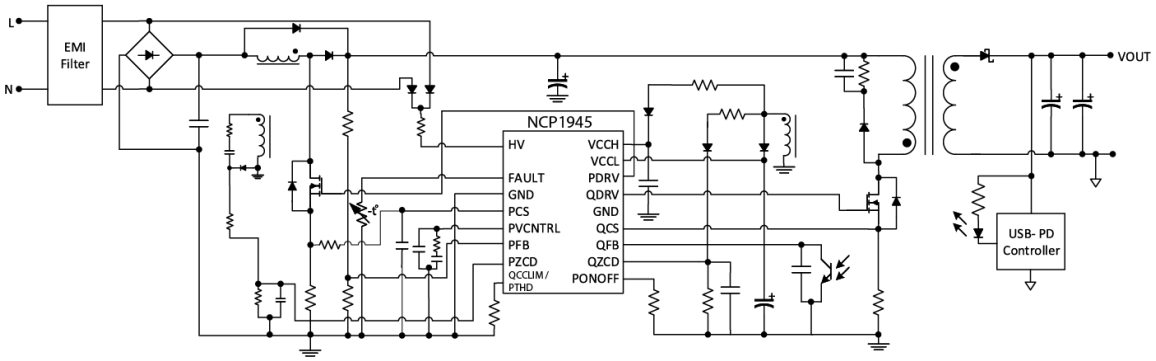


Figure 1. Typical Application Circuit

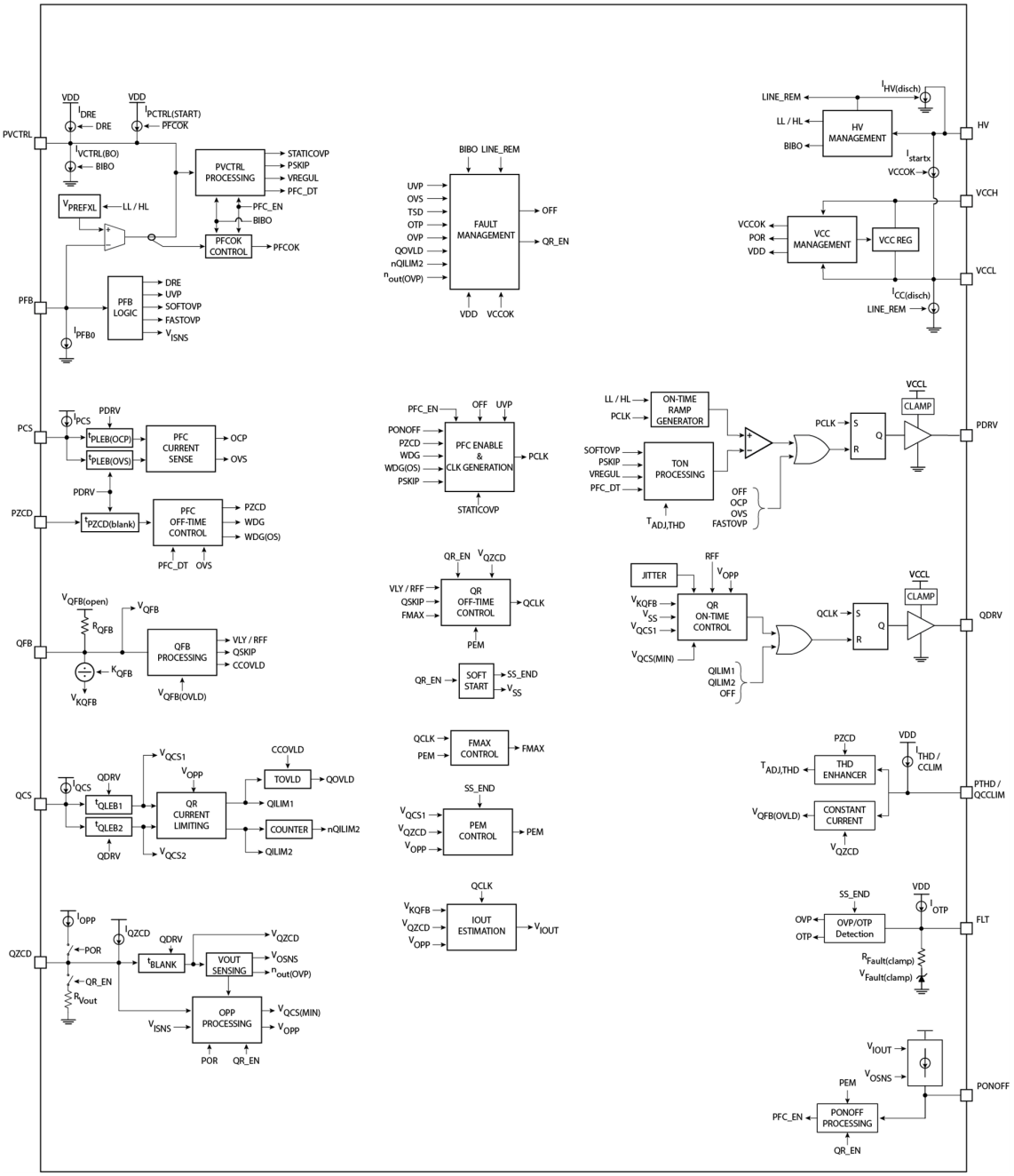


Figure 2. NCP1945 Simplified Block Diagram

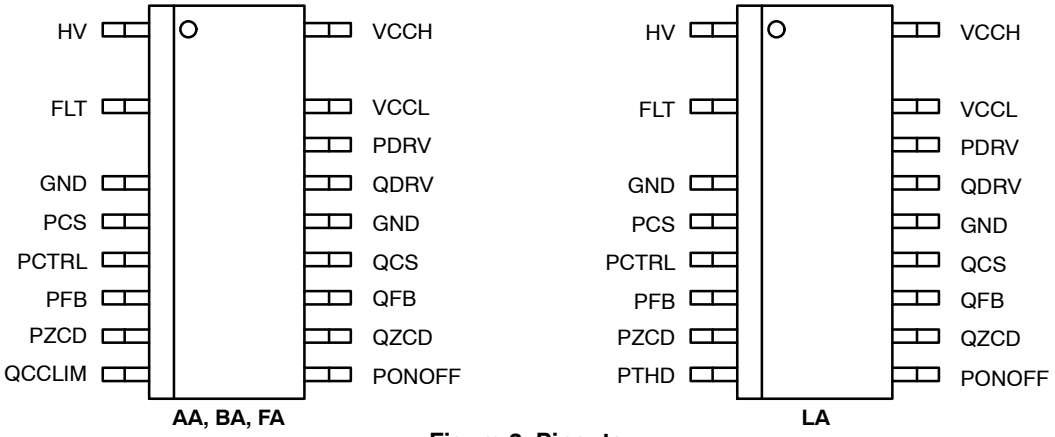


Figure 3. Pinouts

Table 1. PIN DESCRIPTION

Pin Name	Pin Number	Function
HV	1	Input to the high voltage startup and AC line detection circuitry. This pin is used for brownout and line removal detection.
Fault	2	The controller enters fault mode if the voltage on this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor.
GND	3, 13	Power Supply Ground reference.
PCS	4	Input to the cycle-by-cycle current limit comparator for PFC. A small RC filter should be used to interface the current sense component to the PCS pin
PVCTRL	5	Output of the PFC transconductance error amplifier. A compensation network is connected between this pin and ground to set the loop bandwidth.
PFB	6	PFC feedback input. An external resistor divider is used to sense the PFC bulk voltage. This voltage is compared to an internal reference for regulating the PFC output. Voltage on this pin also determines the amount of OPP applied to the QR converter.
PZCD	7	Based on a novel circuit configuration, this pin detects demagnetization of the PFC inductor. This pin can also be used to detect the AC input voltage for the THD enhancer feature.
PTHD/ QCCLIM	8	A resistor to GND sets the voltage on this pin. The voltage is used to program either the PFC THD enhancer or QR Constant Current Limit, depending on the OPN
PONOFF	9	This pin outputs a current source representative of the QR output power. A resistor to GND sets the power level to enable/disable the PFC.
QZCD	10	This pin is used for QR valley detection, output voltage sampling, and programming OPP compensation. The pin should connect to the QR auxiliary winding through a resistor divider.
QFB	11	Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.
QCS	12	Input to the cycle-by-cycle current limit comparator for QR Flyback. A small RC filter should be used to interface the current sense component to the QCS pin
QDRV	14	This is the drive pin for the QR switch. The driver features a well-regulated voltage clamp that can be programmed to either 12 V for Si FETs or 6.5 V for GaN HEMTs.
PDRV	15	This is the drive pin for the PFC switch. The driver features a well-regulated voltage clamp that can be programmed to either 12 V for Si FETs or 6.5 V for GaN HEMTs.
VCCL	16	This pin is the positive supply of the IC and is intended to interface with the lower Auxiliary winding from the QR transformer.
VCCH	17	This pin is intended to interface with the high voltage Auxiliary winding from the QR transformer and utilizes a linear regulator to bias VCCL when the lower auxiliary winding voltage is below Vcc(off). This pin is rated up to 150 V.

Table 2. NCP1945 DEVICE OPTION

	NCP1945 Versions			
Device Options	**NCP1945AADR2G**	**NCP1945BADR2G**	**NCP1945FADR2G**	**NCP1945LADR2G**
Power Excursion Mode	Enabled	Enabled	Enabled	Disabled
Rapid Frequency Foldback	Enabled	Enabled	Enabled	Disabled
t_ZCD(Blank)	1.2 μs	1.2 μs	1.2 μs	3 μs
Gate Drive Clamp	Si – 12 V	GaN – 6.5 V	Si – 12 V	Si – 12 V
Weak Drive	Disabled	Disabled	Enabled	Enabled
PFC Boost Follower – V_{PREFLL}	Enabled – 1.6 V	Enabled – 1.6 V	Enabled – 1.8 V	Disabled – 2.5 V
QR Constant Current OVLD	Programmable	Programmable	Programmable	Disabled
THD Enhancer	Disabled	Disabled	Disabled	Programmable

Table 3. ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
NCP1945AADR2G	SOIC20 NB (Pb−Free)	2500 / Tape & Reel
NCP1945BADR2G	SOIC20 NB (Pb−Free)	
NCP1945LADR2G	SOIC20 NB (Pb−Free)	
NCP1945FADR2G	SOIC20 NB (Pb−Free)	

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 4. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	$V_{HV(MAX)}$	−0.3 to 700	V
High Voltage Startup Circuit Input Current	$I_{HV(MAX)}$	30	mA
Supply Input Voltage	$V_{CCH(MAX)}$	−0.3 to 150	V
Supply Input Current	$I_{CCH(MAX)}$	30	mA
Supply Input Voltage	$V_{CCL(MAX)}$	−0.3 to 30	V
Supply Input Current	$I_{CCL(MAX)}$	30	mA
Supply Input Voltage Slew Rate	dV_{CC}/dt	1	V/μs
Fault Input Voltage	$V_{Fault(MAX)}$	−0.3 to V_{CC} + 0.7	V
Fault Input Current	$I_{Fault(MAX)}$	10	mA
QR Zero Current Detection Input Voltage	$V_{QZCD(MAX)}$	$V_{QZCD(MIN)}$ to V_{CC} + 0.7	V
PFC Zero Current Detection Input Voltage	$V_{PZCD(MAX)}$	−0.3 to V_{CC} + 0.7	V
QR Zero Current Detection and OPP Input Current	$I_{QZCD(MAX)}$	−2/+5	mA
PFC Zero Current Detection Input Current	$I_{PZCD(MAX)}$	−2/+5	mA
Driver Maximum Voltage (Note 1)	V_{xDRV}	−0.3 to $V_{xDRV(high)}$	V
Driver Maximum Current	$I_{xDRV(SRC)}$	500	mA
	$I_{xDRV(SNK)}$	800	mA
Maximum Input Voltage (All Other Pins)	V_{MAX}	−0.3 to 5.5	V
Maximum Input Current (All Other Pins)	I_{MAX}	10	mA
Operating Junction Temperature	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Power Dissipation (T_A = 25 °C, 1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad) D Suffix, SOIC-8 and D1 Suffix, SOIC-9	$P_{D(MAX)}$	450	mW
Thermal Resistance, Junction to Ambient (1 Oz Cu Printed Circuit Copper Clad) Suffix, SOIC-8 and D1 Suffix, SOIC-9	$R_{\theta JA}$	225	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22-A114E Charge Device Model per JEDEC Standard JESD22-C101E Latch-Up Protection per JEDEC Standard JESD78		 2000 1000 ±100	 V V mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applies to both QDRV and PDRV. Maximum driver voltage is limited by the driver clamp voltage, $V_{xDRV(high)}$, when V_{CCL} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CCL}.

Table 5. ELECTRICAL CHARACTERISTICS
(V_{CCL} = 12 V, V_{CCH} = V_{CCL}, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCCL} = 100 nF, C_{VCCH} = 100 nF, C_{xDRV} = 100 pF, for typical values T_J = 25 °C, for min/max values, T_J is –40 °C to 125 °C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START-UP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Operating Hysteresis ($V_{CC(on)}$ – $V_{CC(off)}$) Internal Latch / Logic Reset Level Transition from I_{start1} to I_{start2}	dV/dt = 0.1 V/ms V_{CC} increasing V_{CC} decreasing V_{CC} decreasing V_{CC} decreasing V_{CC} increasing, I_{HV} = 650 μA	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(reset)}$ $V_{CC(inhibit)}$	 16.0 8.5 7.5 6.0 0.40	 17.0 9.0 – 6.5 0.70	 18.0 9.5 – 7.0 1.05	V
$V_{CC(off)}$ Delay	V_{CC} decreasing	$t_{delay(VCC\_off)}$	25	32	40	μs
Minimum Voltage for Start-Up Current Source		$V_{HV(MIN)}$	–	–	40	V
Inhibit Current Sourced to V_{CC} Pin	V_{CCL} = 0 V	I_{start1}	0.2	0.5	0.65	mA
Start-Up Current Sourced to V_{CC} Pin	V_{CCL} = $V_{cc(on)}$ – 0.5 V HV Discharge Active	I_{start2} I_{start3}	2.4 –	3.75 –	5.8 0	mA
Start-Up Circuit Off-State Leakage Current	V_{HV} = 700 V	$I_{HV(off)}$	–	–	30	μA
Supply Current Fault or Latch Skip Mode (excluding QFB current), PFC disabled Operating Current, QR and PFC Enabled	 V_{CCL} = $V_{CC(on)}$ – 0.5 V V_{QFB} = 0 V QR & PFC F_{sw} = 50 kHz, C_{xDRV} = open	 I_{CCL1} I_{CCL2} I_{CCL3}	 – – –	 0.115 0.35 2.6	 0.250 0.55 3.65	mA
DUAL VCC MANAGEMENT						
Regulation Voltage	I_{CCH} = 5 mA, V_{CCH} = 30 V	V_{REG}	9.5	10.0	10.6	V
Dropout Voltage (V_{VCCH} – V_{VCCL})	Adjust V_{CCH} such that V_{CCL} = V_{REG} – 1 V I_{CCH} = 5 mA I_{CCH} = 500 μA	V_{DO}	 – –	 600 75	 1300 200	mV
Input Off-State Leakage Current	V_{CCH} = 150 V	$I_{VCCH(off)}$	–	–	15	μA
INPUT FILTER CAPACITOR DISCHARGE						
Line Voltage Removal Detection Timer		$t_{line(removal)}$	80	100	120	ms
Upslope Detection Reset Timer	HV increasing	$t_{HV(up)}$	–	14.0	–	ms
Downslope Detection Reset Timer	HV decreasing	$t_{HV(down)}$	–	1.0	–	ms
HV Discharge Current	 V_{HV} = $V_{HVdisch(end)}$ + 100 mV	$I_{HV(disch)}$	 0.75 0.04	 2 –	 3.75 0.6	mA
V_{CC} Discharge Current	V_{CCL} = $V_{CC(on)}$	$I_{CC(disch)}$	13	18	23	mA
Minimum Voltage for Discharge Current Source	I_{HV} = 0.8 x $I_{HV(disch)}$ HV Discharge Active	$V_{HVdisch(min)}$	–	–	40	V
HV Discharge Stop Level		$V_{HVdisch(end)}$	–	–	30	V
Delta Between $V_{CC(on)}$ and HV Discharge Stop Level		$\Delta_{discharge}$	–0.2	–	–	V
BROWNOUT DETECTION						
System Start-Up Threshold	V_{HV} increasing	$V_{BO(start)}$	107	112	117	V
Brownout Threshold	V_{HV} decreasing	$V_{BO(stop)}$	93	98	102	V
Brownout Hysteresis	V_{HV} increasing	$V_{BO(HYS)}$	9	14	–	V
Brownout Detection Blanking Time	V_{HV} decreasing	$t_{BO(stop)}$	40	70	100	ms
System Start-Up Threshold Filter		$t_{delay(BO\_start)}$	50	100	150	μs

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(V_{CCL} = 12 V, V_{CCH} = V_{CCL}, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCCL} = 100 nF, C_{VCCH} = 100 nF, C_{xDRV} = 100 pF, for typical values T_J = 25 °C, for min/max values, T_J is –40 °C to 125 °C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
BROWNOUT DETECTION						
Brownout Detection Blanking Time Filter		$t_{delay(BO\_stop)}$	200	300	400	μs
LINE RANGE DETECTION						
Low Line to High Line Transition Threshold	V_{HV} increasing	$V_{HL(th)}$	221	236	251	V
High Line to Low Line Transition Threshold	V_{HV} decreasing	$V_{LL(th)}$	209	222	237	V
Line Range Hysteresis	V_{HV} decreasing	$V_{LINE(HYS)}$	10	14	–	V
Line range detector blanking time	V_{HV} decreasing	$t_{HL(blank)}$	20	25	30	ms
Line Range Detection Watchdog	V_{HV} increasing	$T_{WDG,HL}$	430	500	560	ms
QR GATE DRIVE						
Rise Time FA, LA Version FA, LA Version	V_{QDRV} from 10% to 90% C_{QDRV} = 100 pF C_{QDRV} = 1 nF V_{QFB} = 0.8 V, C_{QDRV} = 100 pF V_{QFB} = 0.8 V, C_{QDRV} = 1 nF	$t_{QDRV(rise)}$	– – – –	20 50 200 500	40 90 – –	ns
Fall Time	V_{QDRV} from 90% to 10% C_{QDRV} = 1 nF	$t_{QDRV(fall)}$	–	20	60	ns
Source Current Capability FA, LA Version	V_{QFB} = 2 V V_{QFB} = 0.8 V	$I_{QDRV(SRC)}$	– –	500 50	– –	mA
Sink Current Capability		$I_{QDRV(SNK)}$	–	800	–	mA
Adaptive Gate Drive Activation Valley		$n_{DRV(valley)}$	–	5	–	
Drive Clamp Voltage NCP1945AA, FA, LA NCP1945BA	V_{CCL} = 30 V, R_{QDRV} = 10 kΩ	$V_{QDRV(clamp)}$	10 6.1	12 6.5	14 6.9	V
High State Voltage NCP1945AA, FA, LA NCP1945BA	V_{CCL} = $V_{CC(off)}$ + 0.2 V, R_{QDRV} = 10 kΩ	$V_{QDRV(high)}$	8 6.1	– –	– –	V
Low Stage Voltage	V_{Fault} = 0 V	$V_{QDRV(low)}$	–	–	0.25	V
QR FEEDBACK						
Open Pin Voltage		$V_{QFB(open)}$	4.8	5.0	5.2	V
V_{QFB} to Internal Current Setpoint Division Ratio NCP1945LA NCP1945AA, BA, FA		K_{QFB}	3.6 2.7	4.00 3.00	4.4 3.3	
Internal Pull-Up Resistor	V_{QFB} = 0.4 V	R_{QFB}	17.0	20.0	25.0	kΩ
Valley Thresholds (NCP1945AA, BA, FA) Transition from 1st to 2nd valley Transition from 2nd to 3rd valley Transition from 3rd to 4th valley Transition from 4th to 5th valley Transition from 5th to 6th valley Transition from 6th to 5th valley Transition from 5th to 4th valley Transition from 4th to 3rd valley Transition from 3rd to 2nd valley Transition from 2nd to 1st valley	 V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing	 V_{1to2} V_{2to3} V_{3to4} V_{4to5} V_{5to6} V_{6to5} V_{5to4} V_{4to3} V_{3to2} V_{2to1}	 0.987 0.846 0.776 0.705 0.635 1.199 1.269 1.340 1.410 1.551	 1.050 0.900 0.825 0.750 0.675 1.275 1.350 1.425 1.500 1.650	 1.113 0.954 0.874 0.795 0.715 1.352 1.431 1.511 1.590 1.749	V

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(V_{CCL} = 12 V, V_{CCH} = V_{CCL}, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCCL} = 100 nF, C_{VCCH} = 100 nF, C_{xDRV} = 100 pF, for typical values T_J = 25 °C, for min/max values, T_J is –40 °C to 125 °C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
QR FEEDBACK						
Valley Thresholds (NCP1945LA) Transition from 1st to 2nd valley Transition from 2nd to 3rd valley Transition from 3rd to 4th valley Transition from 4th to 5th valley Transition from 5th to 6th valley Transition from 6th to 5th valley Transition from 5th to 4th valley Transition from 4th to 3rd valley Transition from 3rd to 2nd valley Transition from 2nd to 1st valley	 V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} decreasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing V_{QFB} increasing	 V_{1to2} V_{2to3} V_{3to4} V_{4to5} V_{5to6} V_{6to5} V_{5to4} V_{4to3} V_{3to2} V_{2to1}	 1.316 1.128 1.034 0.940 0.846 1.410 1.504 1.598 1.692 1.880	 1.400 1.200 1.100 1.000 0.900 1.500 1.600 1.700 1.800 2.000	 1.484 1.272 1.166 1.060 0.954 1.590 1.696 1.802 1.908 2.120	V
Maximum On Time		$t_{on(MAX)}$	26	32	38	μs
QR DEMAGNETIZATION INPUT						
QZCD Threshold Voltage	V_{QZCD} decreasing	$V_{QZCD(trig)}$	30	60	90	mV
QZCD Hysteresis	V_{QZCD} increasing	$V_{QZCD(HYS)}$	10	25	55	mV
QZCD Demagnetization Propagation Delay	V_{QZCD} step from 2.1 V to 0 V	t_{demag}	–	80	150	ns
QZCD Clamp Voltage Negative Clamp	Not including R_{vout} I_{QZCD} = –2.0 mA	$V_{QZCD(MIN)}$	–0.9	–0.7	0	V
QZCD Blanking Delay After Turn-Off NCP1945AA, BA, FA NCP1945LA		$t_{QZCD(blank)}$	 1 2.25	 1.2 3.00	 1.4 3.75	μs
Timeout After Last Demagnetization Detection	While in soft-start After soft-start complete	$t_{(tout1)}$ $t_{(tout2)}$	80 5.1	100 6	120 6.9	μs
QZCD Pull-Down Resistor		R_{Vout}	0.95	1.00	1.04	kΩ
QZCD Pull-Up Current		I_{QZCD}	0.8	1	1.2	μA
QR CURRENT SENSE						
Soft-Start Period	Measured from 1st DRV pulse to V_{QCS} = V_{QILIM1}	t_{SSTART}	2.8	4.0	5.0	ms
Current Limit Threshold Voltage NCP1945LA NCP1945AA, BA, FA	V_{QCS} increasing	V_{QILIM1}	 0.765 0.96	 0.8 1	 0.835 1.04	V
Leading Edge Blanking Duration	DRV minimum width minus $t_{delay(QILIM1)}$	t_{QLEB1}	220	275	330	ns
Current Limit Threshold Propagation Delay	Step V_{QCS} 25 mV below V_{QILIM1} to 75 mV above V_{QILIM1},V_{OPP} = 0, V_{QFB} = 4 V	$t_{delay(QILIM1)}$	–	–	80	ns
Overpower Protection Delay	Step V_{QCS} 25 mV below V_{QILIM1} – V_{OPP} to 75 mV above V_{QILIM1} – V_{OPP}, V_{QFB} = 4 V	$t_{OPP(delay)}$	–	–	90	ns
PWM Comparator Propagation Delay	Step V_{QCS} 25 mV below V_{QFB}/k_{FB} to 75 mV above V_{QFB}/k_{FB}	$t_{delay(PWM)}$	–	–	110	ns
Minimum Peak Current	V_{OPP} = 0 $V_{QZCD(hi)}$ = 10.5 V $V_{QZCD(hi)}$ = 1.25 V	$V_{QCS(MIN)}$	 180 63	 200 80	 240 97	mV
Minimum Peak Current with OPP	$V_{QZCD(hi)}$ = 1.25 V	$V_{CS(MIN\_clamp)}$	–	40	–	mV
QCSmin Comparator Propagation Delay	Step V_{QCS} 25 mV below $V_{QCS(MIN)}$ to 75 mV above $V_{QCS(MIN)}$	$t_{delay(QCSMIN)}$	–	–	140	ns
RFF Entry Threshold (Disabled in NCP1945LA)	V_{QFB} Decreasing	$V_{RFF(entry)}$	550	600	650	mV
RFF Peak Current Shift (Disabled in NCP1945LA)	V_{QFB} = $V_{RFF(entry)}$	$V_{RFF(delta)}$	340	400	460	mV

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(V_{CCL} = 12 V, V_{CCH} = V_{CCL}, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCCL} = 100 nF, C_{VCCH} = 100 nF, C_{xDRV} = 100 pF, for typical values T_J = 25 °C, for min/max values, T_J is –40 °C to 125 °C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
QR CURRENT SENSE						
RFF Exit Threshold (Disabled in NCP1945LA)	V_{QFB} Increasing	$V_{RFF(exit)}$	520	550	580	mV
RFF Transition Timer (Disabled in NCP1945LA)		t_{RFF}	0.80	1.00	1.1	ms
Abnormal Overcurrent Fault Threshold LA AA, BA, FA	V_{QCS} increasing, V_{QFB} = 5.0 V	V_{QILIM2}	 1.125 1.4	 1.20 1.5	 1.27 1.6	V
Abnormal Overcurrent Fault Blanking Duration	QDRV minimum width minus $t_{delay(QILIM2)}$	t_{QLEB2}	55	80	105	ns
Abnormal Overcurrent Fault Propagation Delay	Step V_{QCS} 25 mV below V_{QILIM2} to 75 mV above V_{QLIM2}, V_{QFB} = 5 V	$t_{delay(QILIM2)}$	–	–	90	ns
Number of Consecutive Abnormal Overcurrent Faults to Enter Latch Mode		n_{QILIM2}	–	4	–	
Pull-Up Current Source	V_{QCS} = 1.5 V	I_{QCS}	0.7	1.0	1.5	A
POWER EXCURSION MODE (AA, BA, FA only)						
PEM QCS Activation Threshold	V_{QCS} increasing	V_{PEM}	0.760	0.800	0.840	V
Maximum QFB Voltage for Off-Time Scaling	Guaranteed By Design, V_{QFB} increasing	$V_{QFB(MAX)}$	3.5	–	–	V
Maximum Off-Time Reduction During PEM	V_{QFB} = 3.6 V	$1/K_{scale(MAX)}$	2.5	–	–	
PEM QZCD Arming Threshold	V_{QZCD} increasing	$V_{PEM(arm)}$	0.65	0.8	1.0	V
Maximum Switching Frequency in PEM	V_{QFB} = 3.6 V	$F_{MAX(PEM)}$	–	140	–	kHz
OVERPOWER PTOTECTION (OPP)						
OPP Programming Current on QZCD	Startup Only	I_{OPP}	18.8	20	21.2	μA
QZCD Programming Resistor for Maximum OPP		$R_{QZCD(MAX)}$	–	150	–	kΩ
Maximum OPP Applied to QCS		$V_{OPP(MAX)}$	80	100	120	mV
QZCD Programming Resistor for No OPP		$R_{QZCD(MIN)}$	–	7.5	–	kΩ
OPP at High Line w/ PFC Enabled	R_{QZCD} = 150 kΩ, V_{PFB} = 2.5 V	$V_{OPP(HL1)}$	–	100	–	mV
OPP at Low Line w/ PFC Enabled	R_{QZCD} = 150 kΩ, V_{PFB} = 1.6 V	$V_{OPP(LL1)}$	–	70	–	mV
OUTPUT CURRENT LIMIT (DISABLED FOR NCP1945LA)						
QR CCLIM Reference Programming Current	V_{CCLIM} = 0	I_{CCLIM}	9	10	11	μA
Programming Resistor for Maximum Constant Current Limitation	1% Resistor	$R_{CCLIM(MAX)}$	–	84.5	–	kΩ
Programming Resistor for Minimum Constant Current Limitation	1% Resistor	$R_{CCLIM(MIN)}$	–	15	–	kΩ
Feedback Voltage Overload Threshold PEM enabled	Apply 100 kHz Square Wave to QZCD Pin +6.9 V / 0 V, and Inverse Square Wave to CS Pin 0.9 V/0 V 60% Duty Cycle, V_{CCLIM} = 310 mV 95% Duty Cycle, V_{CCLIM} = 310 mV 60% Duty Cycle, V_{CCLIM} = 450 mV 95% Duty Cycle, V_{CCLIM} = 450 mV	$V_{QFB(OVLD)}$	 1.475 0.85 2.280 1.340	 1.75 0.99 2.680 1.575	 2.025 1.15 3.080 1.810	V
QR FREQUENCY JITTERING						
Jitter Frequency	Measured on QCS	f_{jitter}	2.73	3.90	5.07	kHz
Peak-to-Peak Jitter Voltage	Measured on QCS	V_{jitter}	85	100	115	mV

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(V_{CCL} = 12 V, V_{CCH} = V_{CCL}, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{VCCL} = 100 nF, C_{VCCH} = 100 nF, C_{xDRV} = 100 pF, for typical values T_J = 25 °C, for min/max values, T_J is –40 °C to 125 °C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
FAULT PROTECTION						
Flyback Overload Fault Timer	V_{QCS} = V_{QILIM1} + 0.2 V	t_{OVLD}	120	160	200	ms
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	VFault(OVP)	2.99	3.2	3.41	V
Overvoltage Protection (OVP) Delay	V_{Fault} increasing	$t_{delay(OVP)}$	22.5	30.0	37.5	µs
Output OVP Threshold Measured on QZCD		$V_{out(OVP)}$	11.4	12	12.4	V
Number of Consecutive OVP Detections to Trigger Fault		$n_{out(OVP)}$	–	3	–	
Overtemperature Protection (OTP) Threshold	V_{Fault} decreasing	$V_{Fault(OTP\_in)}$	0.385	0.40	0.415	V
Overtemperature Protection (OTP) Exiting Threshold	V_{Fault} increasing	$V_{Fault(OTP\_out)}$	0.880	0.920	0.960	V
OTP Detection Delay	V_{Fault} decreasing	$t_{delay(OTP)}$	22.5	30.0	37.5	µs
OTP Pull-Up Current Source	V_{Fault} = $V_{Fault(OTP\_in)}$ + 0.2 V	I_{OTP}	43.6	45.0	46.35	µA
Fault Input Clamp Voltage	V_{FLT} = Open	$V_{Fault(clamp)}$	1.15	1.7	2.25	V
Fault Input Clamp Series Resistor		$R_{Fault(clamp)}$	1.52	1.75	1.98	kΩ
Autorecovery Timer		$t_{restart}$	1.8	2	2.2	s
QR LIGHT LOAD MANAGEMENT						
Minimum Frequency Clamp		Qf_{MIN}	21	24.5	28	kHz
Dead-Time Added During Frequency Foldback NCP1945LA NCP1945AA, BA, FA	 V_{QFB} = 400 mV V_{QFB} = 300 mV	$t_{DT(MAX)}$	 32 32	 – –	 – –	µs
Skip Entry Threshold NCP1945LA NCP1945AA, BA, FA	V_{QFB} decreasing	V_{QSKIP}	 304 284	 320 300	 336 316	mV
Skip Exit Threshold NCP1945LA NCP1945AA, BA, FA	V_{QFB} increasing	V_{QSKIP_EXIT}	 350 330	 370 350	 390 370	mV
Skip Hysteresis	V_{QFB} increasing	$V_{QSKIP(HYS)}$	–	50	–	mV
THERMAL PROTECTION						
Thermal Shutdown	Temperature increasing	T_{SHDN}	–	140	–	°C
Thermal Shutdown Hysteresis	Temperature decreasing	$T_{SHDN(HYS)}$	–	40	–	°C
Thermal Shutdown Delay		$t_{delay(TSHDN)}$	–	30	–	µs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

* NTC with R_{110} = 8.8 k. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Table 6. PFC SPECIFICATIONS

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
PFC GATE DRIVE						
Rise Time	V_{PDRV} from 10% to 90% C_{PDRV} = 100 pF C_{PDRV} = 1 nF	$t_{PDRV(rise)}$	– 	 20 50	 40 90	ns
Fall Time Source Current Capability	V_{PDRV} from 90% to 10% C_{PDRV} = 1 nF	$t_{PDRV(fall)}$	–	20	60	ns
		$I_{PDRV(SRC)}$	–	500	–	mA
Sink Current Capability		$I_{PDRV(SNK)}$	–	800	–	mA
Drive Clamp Voltage NCP1945AA, FA, LA NCP1945BA	V_{CCL} = 30 V R_{PDRV} = 10 kΩ	$V_{PDRV(clamp)}$	 10 6.1	 12 6.5	 14 6.9	V
High State Voltage NCP1945AA, FA, LA NCP1945BA	$V_{CCL} = V_{CC(off)} + 0.2$ V R_{PDRV} = 10 kΩ	$V_{PDRV(high)}$	 8 6.1	 – –	 – –	V
Low Stage Voltage	V_{Fault} = 0 V	$V_{PDRV(low)}$	–	–	0.25	V
FREQUENCY FOLD-BACK DEAD TIME						
Dead-Time, V_{PCTRL} = 0.63 V	V_{PCTRL} = 0.63 V	$t_{DT1,E}$	10.29	14.7	19.11	μs
Dead-Time, V_{PCTRL} = 0.75 V	V_{PCTRL} = 0.75 V	$t_{DT2,E}$	4.83	6.9	8.97	μs
V_{PCTRL} threshold CrM to DCM mode	V_{PCTRL} decreasing	$V_{PCTRL(FF)}$	1.39	1.55	1.71	V
V_{PCTRL} DCM to CrM Hysteresis	V_{PCTRL} increasing	$V_{PCTRL(FF)hys}$	75	100	–	mV
Minimum Frequency Timer Period (valley synchronized)		T_{fmin}	30	–	40	μs
Minimum Switching Frequency (valley synchronized).	pfcOK high	F_{min}	24	–	–	kHz
V_{PCTRL} pin SKIP Level, PFC Skip Exit Threshold	V_{PCTRL} rising	$V_{PSKIP-EXIT}$	0.55	0.62	0.68	V
V_{PCTRL} pin SKIP Level, PFC Skip Entry Threshold	V_{PCTRL} falling	$V_{PSKIP-EN}$	0.50	0.56	0.62	V
V_{PCTRL} pin SKIP Hysteresis, PFC Skip Threshold Hysteresis		$V_{PSKIP(hys)}$	40	70	100	mV
REGULATION BLOCK						
Feedback Voltage Reference	High Line	V_{PREFHL}	2.44	2.50	2.56	V
Feedback Voltage Reference NCP1945AA, BA NCP1945FA NCP1945LA	Low Line	V_{PREFLL}	 1.55 1.75 2.44	 1.6 1.8 2.5	 1.65 1.85 2.56	V
Error Amplifier Current Capability		I_{EA}	–	±20	–	μA
PCTRL Startup Source Current		$I_{VCTRL(START)}$	90	120	150	μA
Error Amplifier Gain		G_{EA}	110	200	290	μS
PCTRL Dynamic Voltage Range: – @ V_{PFB} = 2 V (OTA is sourcing 20 μA) – @ V_{PFB} = 3 V (OTA is sinking 20 μA)		 $V_{PCTRL(MAX)}$ $V_{PCTRL(MIN)}$	 – –	 4.5 0.5	 – –	V
Gain from V_{PCTRL} to internal V_{regul}		K_{PCTRL}	–	0.75	–	
DRE Enable Threshold Below Reference Voltage: $\Delta V_{DRE\_EN} = V_{PFB(DRE\_EN)} - V_{PREFxL}$	V_{PFB} decreasing	ΔV_{DRE_EN}	−133	–	−89	mV
DRE Disable Threshold Below Reference Voltage: $\Delta V_{DRE\_DIS} = V_{PFB(DRE\_DIS)} - V_{PREFxL}$	V_{PFB} increasing	ΔV_{DRE_DIS}	−79	–	−35	mV
DRE Disable Hysteresis Ratio	V_{PFB} increasing	$K_{PFC(DRE\_HYS)}$	1.0	2.0	3.0	%
PCTRL DRE Source Current		I_{DRE}	180	220	250	μA

Table 6. PFC SPECIFICATIONS (continued)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
REGULATION BLOCK						
PCTRL Soft Stop Discharge Current		$I_{VCTRL(BO)}$	20	30	40	μA
CURRENT SENSE						
PCS Over-Current Protection Threshold		$V_{PCS(TH)}$	450	500	550	mV
Over-Current Protection Leading Edge Blanking Time		$t_{PLEB(OCP)}$	320	400	460	ns
PCS Overstress Protection Threshold		$V_{PCS,OVS(th)}$	675	750	825	mV
Number of Consecutive Overstress Faults to Enter Latch Mode		n_{OVS}	–	15	–	
"Overstress" Leading edge Blanking Time		$t_{PLEB(OVS)}$	100	250	400	ns
Over-Current Protection Delay	V_{PCS} rising 10 V/μs	t_{POCP}	–	40	200	ns
Overstress Protection Delay	V_{PCS} rising 10 V/μs	t_{POVS}	–	40	200	ns
Pull-up Current Source for Open Pin Detection	V_{PCS} = 1 V	$I_{PCS(Vcc)}$	100	200	300	nA
ZERO CURRENT DETECTION						
Zero Current Detection, V_{PZCD} Rising		$V_{PZCD(th)H}$	5	40	75	mV
Zero Current Detection, V_{PZCD} Falling		$V_{PZCD(th)L}$	−75	−40	−5	mV
Hysteresis of the Zero Current Detection Comparator		$V_{PZCD(hyst)}$	50	80	110	mV
PZCD Detection Leading Edge Blanking		$t_{PZCD(blank)}$	250	350	450	ns
PZCD Positive Clamp @ I_{PZCD} = 5 mA		$V_{CL(pos)}$	8	9.5	11.5	V
Minimum PZCD to DRV high delay		t_{PZCD0}	–	60	200	ns
Minimum PZCD Pulse Width		t_{SYNC}	–	110	200	ns
Watch Dog Timer		t_{WDG}	80	200	320	μs
Watch Dog Timer in "OverStress" Situation		$t_{WDG(OS)}$	700	800	900	μs
STATIC OVP						
Duty Cycle, V_{PFB} = 3 V (When Low Clamp of P_{CTRL} is Reached)		D_{MIN}	–	–	0	%
ON-TIME CONTROL						
Maximum On Time at Low Line	$V_{PFB} = V_{PREFLL} - 0.5$ V	$t_{onpwm(max),LL}$	10.8	12.5	14.2	μs
Maximum On Time at High Line	$V_{PFB} = V_{PREFHL} - 0.5$ V	$t_{onpwm(max),HL}$	4.2	5.0	5.8	μs
Line Feedforward: Ratio of t_{ONPWM} @LL over t_{ONPWM} @HL		$K_{tonpwmLL-HL}$	–	2.5	–	
Minimum On Time at Low Line		$t_{on,LL,min}$	100	180	250	ns
Minimum On Time at High Line		$t_{on,HL,min}$	50	100	150	ns
FEEDBACK OVER AND UNDER VOLTAGE PROTECTIONS (POVP AND PUVP)						
Soft OVP Enable Threshold Above Reference Voltage at High Line: $V_{softOVP\_HL} - V_{PREFHL}$	V_{PFB} rising	$\Delta V_{softOVP\_HL}$	114	125	150	mV
Soft OVP Enable Threshold Above Reference Voltage at Low Line: $V_{softOVP\_LL} - V_{PREFLL}$; NCP1945AA, BA, FA NCP1945LA	V_{PFB} rising	$\Delta V_{softOVP\_LL}$	 233 –	 250 125	 270 –	mV
Soft OVP Disable Hysteresis	V_{PFB} falling	$\Delta V_{softOVP\_HYS}$	20	50	80	mV
Fast OVP Enable Threshold Above Reference Voltage at High Line: $V_{fastOVP\_HL} - V_{PREFHL}$	V_{PFB} rising	$\Delta V_{fastOVP\_HL}$	159	175	200	mV

Table 6. PFC SPECIFICATIONS (continued)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
FEEDBACK OVER AND UNDER VOLTAGE PROTECTIONS (POVP AND PUVP)						
Fast OVP Enable Threshold Above Reference Voltage at Low Line: $V_{fastOVP\_LL} - V_{PREFLL}$ NCP1945AA, BA, FA NCP1945LA	V_{PFB} rising	$\Delta V_{fastOVP\_LL}$	 326 –	 350 175	 372 –	mV
Fast OVP Disable Hysteresis	V_{PFB} falling	$\Delta V_{fastOVP\_HYS}$	20	50	80	mV
PUVP Exit Threshold	V_{PFB} rising	V_{UVPH}	470	530	590	mV
PUVP Entry Threshold	V_{PFB} falling	V_{UVPL}	240	300	360	mV
PUVP Entry & Exit Filter Time	V_{PFB} rising or falling	t_{UVP}	–	5	–	ms
PFB Pin Bias Current @ $V_{FB} = V_{OVP}$ and $V_{FB} = V_{UVP}$	$V_{PFB} = V_{UVPL}$	I_{PFB0}	50	200	450	nA
PONOFF						
PONOFF Threshold to Enable PFC	V_{Ponoff} rising	$V_{PONOFF(TH)}$	2.95	3	3.05	V
PFC Enable Blanking Filter	$V_{Ponoff} > V_{PONOFF(TH)}$	$T_{PON(blank)}$	640	780	960	μs
PFC Enable Bypass Timer When QR in PEM	$V_{QCS} > V_{PEM}$ $V_{Ponoff} < V_{PONOFF(TH)}$	T_{PEM}	–	6	–	ms
PONOFF Threshold to Disable PFC	V_{Ponoff} falling	$V_{POFF(TH)}$	–	2.55	–	V
Hysteresis Between Enable and Disable	V_{Ponoff} falling	$V_{POFF(HYS)}$	12	15	18	%
PFC Disable Blanking Filter	$V_{Ponoff} < V_{POFF(TH)}$	$T_{POFF(blank)}$	20	25	30	ms
PONOFF Operating Mode Voltage	Apply 100 kHz Square Wave to QZCD 6 V/ 0 V, and Inverse Square Wave to QCS 0.9 V/0 V, 50% Duty Cycle V_{QFB} = 2 V, V_{PFB} = 2.5 V, R_{QZCD} = 150k, R_{PONOFF} = 140 k	$V_{PONOFF1}$	 –	 3	 –	V
THD ENHANCER PIN – NCP1945LA ONLY						
THD Enhancer Programming Current	V_{THD} = 1.5 V	I_{THD}	9	10	11	uA
On Time Adjustment Gain Factor	V_{THD} = 1.5 V, $V_{PZCD(avg)}$ = 1 V,	K_{ADJ}	0.42	0.47	0.52	μs
PFC On Time Adjustment: $\Delta T_{ADJ,THD} = K_{ADJ} \times V_{THD} / V_{PZCD(avg)}$	V_{THD} = 1.5 V, $V_{PZCD(avg)}$ = 1 V	$\Delta T_{ADJ,THD}$	–	705	–	ns
Maximum On Time Adjustment	$V_{PZCD(avg)}$ = 0 V	$T_{ADJ(MAX)}$	3.6	4	4.8	μs

BRIEF DESCRIPTION

INTRODUCTION

The NCP1945 is a highly integrated combination quasi-resonant (QR) flyback and critical conduction mode (CrM) power factor correction (PFC) controller optimized for off-line USB-PD and LED lighting applications requiring wide output voltage range, high power density, and low standby power. It contains an comprehensive feature set necessary for high density, performance optimization and robust protection. Key features are described below:

- **High Voltage (HV) Startup Circuit**

The NCP1945 features a high voltage startup circuit enabling the device to charge the VCC capacitor during power up of the application. Once the application begins switching, an auxiliary winding should supply VCC and the high voltage startup circuit transitions to a high impedance state, minimizing the power consumed from the HV input. This enables the application to achieve very low standby and no-load power consumption, satisfying regulatory energy conservation standards.

The HV startup circuit also performs line voltage sensing for the application, providing internal brownin / brown-out (BIBO) protection, low line (US Mains) vs high line (EU & Asia Mains) detection, and line removal detection. BIBO protection functions as input under-voltage protection, ensuring that the application only operates when the input mains voltage is above a specified value. The device inhibits switching when the detected mains voltage is below the brown-out threshold, preventing the application from attempting to regulate when the input voltage is too low.

Low line / high line detection adjusts certain operating parameters of the NCP1945 to optimize operation for the different line voltages. The PFC incorporates line voltage feedforward which adjusts the loop gain of the on-time modulator circuit to offset the increased loop gain at higher line voltages. This allows the PFC to have a more consistent and stable compensation design across line voltages. Line detection is also used to implement the two-level boost follower function.

Line removal detection is utilized to incorporate the input X2 capacitor discharge feature. The NCP1945 includes an active discharge circuit to ensure that the X2 capacitors, connected across L – N at the AC input, are discharged to a safe level within the time required from regulatory standards such as IEC 60950 and IEC 62368. The active discharge circuit enables when AC line removal has been detected, and is otherwise in a high impedance state to minimize power consumption from the HV input. This improves the application light load and no load performance compared to bleeder resistors that are sometimes used for safety discharge of the X2 capacitors.

- **Dual VCC Management**

USB-PD and many LED driver applications are required to function across a wide range of output voltages, presenting a challenge for controllers that are self-biased from an auxiliary winding off of the flyback transformer. As the auxiliary winding voltage will typically scale proportionally with the output voltage, it is difficult to remain within the VCC operating range of the controller across the entire output voltage operating range. The NCP1945 addresses this issue by incorporating two VCC pins, VCCL and VCCH, capable of accepting up to 30 V and 150 V, respectively. The dual VCC pins, which include a linear regulator between VCCH and VCCL, enable the NCP1945 to be biased with stacked auxiliary windings to meet the wide output operating range of the design.

- **Flyabck Quasi-Resonant and Valley Lockout Operation**

Quasi-Resonant (QR) mode is a highly efficient mode of operation where the power switch turn-on is synchronized to when the drain-source is at the lowest voltage, or valley of the resonance, minimizing the turn-on losses. QR mode operates with variable switching frequency, which increases as the load decreases. To counteract this and contain the maximum switching frequency, the NCP1945 incorporates a valley transition scheme that pushes the turn-on transition into subsequent valleys as the load decreases. The device also incorporates a valley lockout technique to prevent the device from hopping between different valleys unless there is a substantial change in load. QR with valley lockout operation is maintained for up to 6 valleys, at heavy to medium operating loads.

- **Rapid Frequency Foldback (RFF)**

As the operating load in the application decreases, it becomes less effective to continue valley switching due to damping of the resonance. Below a certain load, the NCP1945 begins adding dead time after the 6$_{th}$ valley, and new drive pulses are initiated after the dead time expires. The added dead time reduces the switching frequency which is beneficial for meeting regulatory light load and no load power dissipation standards.

The added dead time and switching frequency reduction is accelerated by the RFF scheme which forces an increase in the minimum peak current required for drive pulse termination. The forced increase in peak current drives the application control loop to naturally reduce the error voltage delivered to the QFB pin, which then increases the amount of dead time added after the 6$_{th}$ valley. During this mode, dead time continues to be added until skip mode is reached, or the switching frequency reaches its minimum level of 25 kHz.

- **Minimum Peak Current Modulation (MPCM)**

MPCM is the technique utilized by the RFF algorithm to accelerate the switching frequency reduction. During RFF, the minimum peak current is tapered as the switching frequency reduces to ensure that the RFF does not proceed too rapidly, and keeps the application from entering skip mode at too high of a load. Additionally, the MPCM utilizes estimated output voltage information from the QR ZCD pin (QZCD) to limit the absolute minimum peak current setpoint. Lower output voltages will have a lower minimum peak current setpoint, which ensures a consistent skip mode entry load level across the output voltage range.

- **Power Excursion Mode (PEM)**

The NCP1945 includes a power excursion mode, where the QR flyback can operate in off-time controlled continuous conduction mode (CCM) for short time durations, enabling the application to ride through transient peak power loads. PEM operation eliminates the need for a larger transformer to handle peak power requirements and also helps reduce the size of the PFC output bulk capacitance, allowing for higher power density.

- **Programmable Constant Current Overload Protection**

The NCP1945 incorporates a novel current limit technique that utilizes the demagnetization timing measured at QZCD to produce an internal voltage proportional to the application load current. The internal voltage representative of the load current is then compared against a threshold, programmed by the QCCLIM pin. The device enables the overload timer whenever the threshold is exceeded. This technique produces an overload current limit independent of the application's output voltage, and overcoming the inaccuracy of using primary-side cycle-by-cycle peak current limit for enabling overload protection.

- **Over Power Protection (OPP)**

The NCP1945 Over Power Protection compensates for line-dependent overshoot due to propagation delays in the PWM comparator and the QILIM comparator. The gain of the compensation circuit is programmable at application power up via the QZCD pin. The OPP feature utilizes the PFB pin to sense the input voltage to the QR flyback, and applies a voltage offset at the input of the comparators to mitigate the effects of propagation delay. This makes the QFB voltage a precise representation of the peak transformer current enabling more accurate constant current overload protection, PFC on/off detection, and cycle-by-cycle current limit.

- **Frequency Jittering**:

To reduce the application EMI signature, a low frequency triangular voltage is added to the CS signal input of the QR flyback PWM comparator. The voltage that is superimposed on the CS signal modulates the cycle-by-cycle energy transfer in the flyback, which mitigates energy peaking from being concentrated within a narrow frequency band.

- **PFC ON/OFF Detection**

The PONOFF function is utilized to enable the PFC circuit as a function of the QR flyback output power. The feature utilizes a proprietary control circuit that takes the sensed voltage from the QZCD pin and the measured load current from the constant current protection to estimate the output power from the QR flyback. The estimated power signal is output from the PONOFF pin, where a programming resistor can be used to select the power level when the PFC would be enabled.

- **Valley-Synchronized Frequency Foldback**

The NCP1945 PFC classically operates in critical conduction mode (CrM) until the power drops below a threshold level where the PFC stage enters the discontinuous conduction mode (DCM) with a dead time prolonged as the load further decays (frequency foldback). This novel technique also provides stable valley turn-on in both CrM and DCM for a maximized efficiency. In addition, the minimum frequency clamp (33 kHz typically) prevents audible frequencies and the on-time is modulated to ensure near-unity power factor in both CrM and DCM operations.

- **Boost Follower Operation**

The PFC error amplifier can be programmed with a line-dependent reference voltage that increases when the application is operating at high line. This allows the PFC to operate as a two-level boost follower, enabling higher average efficiency across line voltage.

- **Total Harmonic Distortion (THD) Performance Enhancer**

The PTHD pin, available on some device options, is used for programming an on-time extension for the PFC switch that is inversevly proportional to the instantaneous line voltage. The extended on-time is enacted near the AC zero crossings, reducing zero crossing distortion.

DETAILED OPERATING DESCRIPTION

HIGH VOLTAGE (HV) STARTUP CIRCUIT

The NCP1945 contains a multi-functional high voltage (HV) pin embedded with a high voltage startup regulator, line range detector, brownout detection, and line removal detection. To perform these functions correctly, the HV pin must be connected directly to the ac line through a diode "OR" configuration from the line and neutral. The connection diagram interfacing the AC mains to the HV pin is shown in Figure 4. The diodes prevent the pin voltage from going below ground. A resistor in series with the pin should be used to protect the pin during EMC or surge testing. A low value resistor should be used (<5 kΩ) to reduce the voltage offset during start-up.

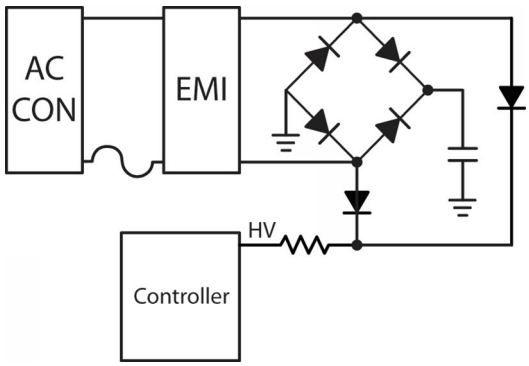


Figure 4. AC Mains Connection to NCP1945 HV Pin

STARTUP AND V_{CC} MANAGEMENT

The NCP1945 integrates a high voltage startup regulator powered through the HV pin. The startup regulator consists of a constant current source that supplies current from the AC input line to the energy storage capacitor on the V_{CCL} pin. During start-up, the current source turns on and charges the V_{CCL} capacitor with I_{start2} (typically 3.75 mA). When V_{CCL} reaches $V_{CC(on)}$ (typically 17.0 V), the current source turns off. If the input voltage is not high enough to ensure a proper start-up (i.e. V_{HV} has not reached $V_{BO(start)}$), the controller will not start. V_{CCL} then begins to fall with the energy storage capacitor being discharged by the device's I_{CC} consumption. When V_{CCL} falls to $V_{CC(off)}$ (typically 9 V), the current source turns back on and charges V_{CCL}. This cycle repeats indefinitely until V_{HV} reaches $V_{BO(start)}$. Once this occurs, I_{start2} immediately turns on and charges V_{CCL} back up to $V_{CC(on)}$, at which point the controller can initiate drive pulses. The startup circuit current (I_{start2}) is typically 3.75 mA provided that V_{CCL} is greater than the $V_{CC(inhibit)}$ threshold, typically 0.7 V. When V_{CCL} is below the inhibit threshold, the startup regulator reduces the current to I_{start1}, typically 0.5 mA. This is done to protect the NCP1945 from thermal failure if there is a short to ground at V_{CCL}. The startup sequence is illustrated in Figure 5.

Once the NCP1945 is enabled, the controller bias current increases and the QR drive pulses are enabled, increasing the total I_{CC} consumption due to the gate charge of the external switching MOSFET. The increase in I_{CC} due to the MOSFET is calculated using Equation 1 where ΔI_{CC} is the increase in milliamps (mA), fsw is the switching frequency in kilohertz (kHz) and Q_G is the gate charge of the external MOSFET in nanocoulombs (nC). The energy storage capacitor on V_{CCL} must be sized such that a V_{CCL} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage increases during start-up. If C_{VCC} is too small, V_{CCL} will fall below $V_{CC(off)}$ and the controller will turn off before the auxiliary winding supplies the IC. The total I_{CC} current after the controller is enabled (I_{CC3} plus ΔI_{CC}) must be considered to correctly size the V_{CCL} energy storage capacitor.

$$\Delta I_{CC} = f_{sw} \cdot Q_G \qquad \text{(eq. 1)}$$

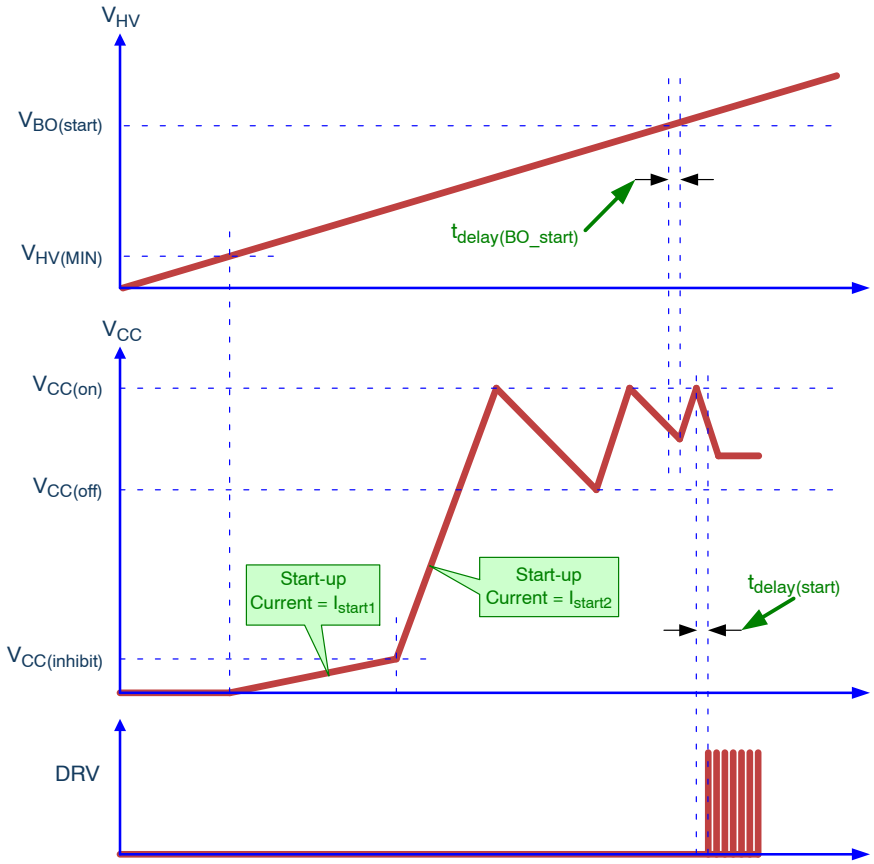


Figure 5. NCP1945 Startup Sequence

DUAL-RANGE V_{CC} MANAGEMENT

For typical USB-PD 3.0 adapter designs, the output voltage ranges from as low as 3.3 V up to 28 V. This wide variation of output voltage places a burden on the application design primary controller to support a wide range of V_{CC} bias voltages. The NCP1945 incorporates a dual range V_{CC} architecture consisting of two V_{CC} pins, V_{CCL} and V_{CCH}, rated at 30 V and 150 V, respectively. The V_{CCH} pin is designed to connect directly to a second aux winding, typically in a stacked winding configuration, and providing a recommended bias voltage that is at least 3 or 4x the output voltage. A simplified diagram of the stacked winding configuration and internal V_{CC} architecture is shown in Figure 6.

When the application output is at lower voltages such as 3.3 or 5 V, the voltage generated across the lower auxiliary winding should be too low to bias the NCP1945. The upper auxiliary winding, stacked on top of the lower winding, will bias the controller through the V_{CCH} pin. When the output is 5 V, the V_{CCH} winding should be designed to supply ~ 15 – 20 V. Internally, the NCP1945 V_{CC} architecture consists of a crude linear regulator which takes the V_{CCH} voltage and regulates it down to the V_{REG} voltage of ~ 10 V at V_{CCL}. The device is then biased from V_{CCL}. The internal linear regulator is designed with a typical dropout voltage, V_{DO}, of 0.6 V, and is therefore able to keep the device operational even if V_{CCH} drops to about 10 V. At higher output voltages, the lower auxiliary winding in the stack will take over biasing of the NCP1945 once it exceeds the V_{REG} voltage. The recommendation for designing the lower auxiliary winding is to bias V_{CCL} at about 20 V at the highest output voltage. This should provide sufficient headroom against the absolute maximum voltage rating of the V_{CCL} pin.

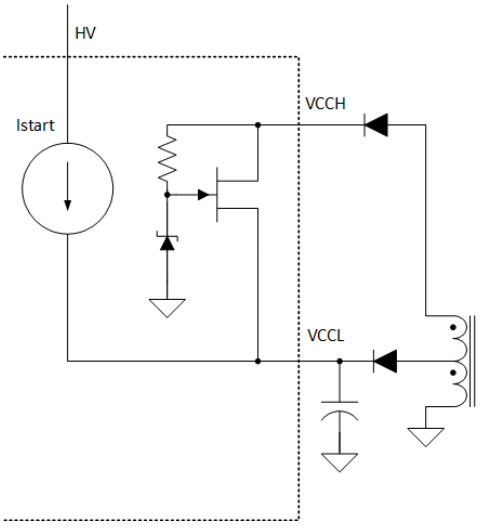


Figure 6. Simplified V_{CC} Architecture and Stacked Auxiliary Windings

LINE VOLTAGE RANGE DETECTOR

The input voltage range is detected based on the peak voltage measured at the HV pin. Discrete values are selected for the PFC stage gain (feedforward) and the PFC reference voltage depending on the input voltage range. The controller determines the line level by comparing the voltage at the HV pin, V_{HV}, to internal line selection thresholds.

The default power-up mode of the controller is high line. In “high line” mode the line range detector blanking timer, $t_{HL(blank)}$, (typically 25 ms) is enabled once V_{HV} falls below $V_{LL(th)}$ (typically 222 V), and the controller switches to low line mode if the $t_{HL(blank)}$ timer expires. Once in low line mode, the controller does not allow transition back to high line mode for a lockout or watchdog period, $T_{WDG,HL}$, typically 500 ms.

After the watchdog timer expires, the controller can switch back to high line mode if the peak HV voltage exceeds the internal high line transition threshold, $V_{HV(HL)}$, typically 236 V. A small internal filter prevents noise coupling or voltage spikes on the line detection from prematurely triggering a high line transition.

In high line mode the PFC maximum on time is reduced by a factor of 2.5, resulting in maximum power capability of the PFC that is largely independent of input voltage. For versions of the device where the boost follower is enabled, the reference voltage for PFC regulation, V_{PREFxL}, also changes depending on whether the device is in low line or high line mode.

The watchdog timer coupled with the line transition threshold hysteresis, $V_{LINE(HYS)}$, typically 14 V, helps to ensure that the device does not oscillate between the two line ranges if the HV pin voltage is near one of the transition thresholds. Figure 7 illustrates the line transition operation.

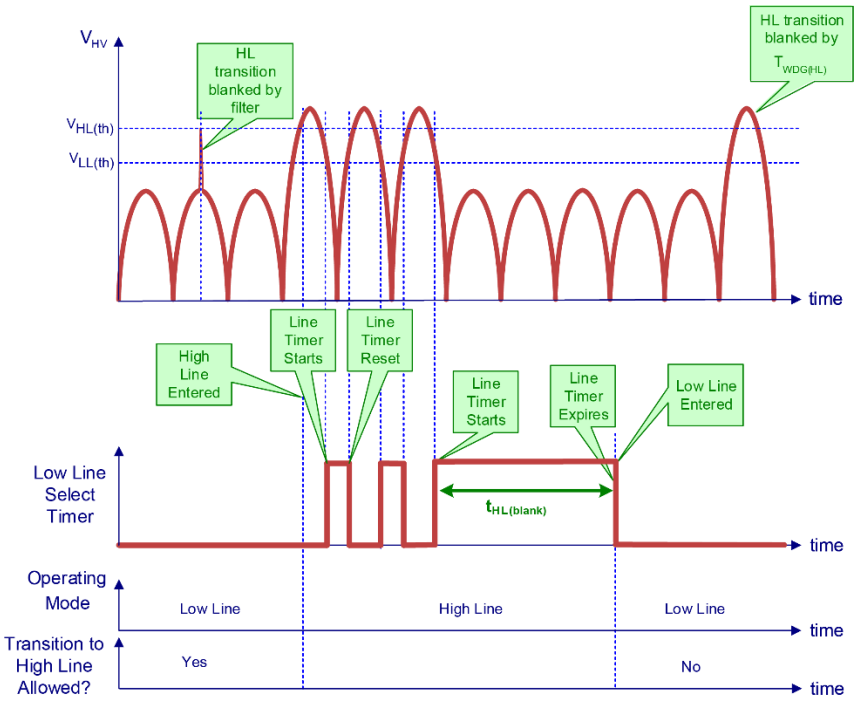


Figure 7. Line Range Detection Operating Waveform

BROWN-IN/OUT (BIBO) DETECTOR

The HV pin voltage is used to provide brown-in/out (BIBO) detection for the NCP1945 controller. The BIBO detector functions as an input under-voltage lockout (UVLO) to prevent the application from operating when the input voltage is below a predetermined threshold.

BIBO protection works similar to the line range detection in that the peak HV pin voltage is compared against internal thresholds to enable and disable the device. For enabling of the NCP1945, V_{HV} must exceed the start threshold, $V_{BO(start)}$, typically 112 V. A small filter, $t_{delay(BO\_start)}$, ensures that the V_{HV} voltage exceeds the threshold for a duration greater than 100 μs before allowing the device to enable. This prevents noise glitches or line voltage spikes from prematurely enabling the device.

Once V_{HV} exceeds the $V_{BO(start)}$ threshold, the NCP1945 will enable drive pulses for the QR flyback when the V_{CCL} voltage reaches the $V_{CC(ON)}$ threshold. To facilitate a faster startup, the HV startup regulator will immediately enable when V_{HV} exceeds the BO start threshold. This begins immediate charging of the V_{CCL} capacitor.

Once the NCP1945 has been enabled, the BIBO detector continuously monitors V_{HV} and enables a 70 ms timer, $t_{BO(stop)}$, whenever V_{HV} falls below the $V_{BO(stop)}$ threshold, which is typically 98 V. If the $t_{BO(stop)}$ timer expires, the device will declare a brown-out fault and disable drive

pulses. Note that the drive pulses may not be immediately disabled, as the NCP1945 does have a soft stop algorithm for powering down if the PFC is enabled. The soft stop feature allows the PFC circuit to shut down slowly, discharging stored energy in the EMI chokes and input wiring cables. This mitigates inductive voltage spikes that may occur due to residual energy along the input line inductances. Figure 8 shows the basic operation of the BIBO feature.

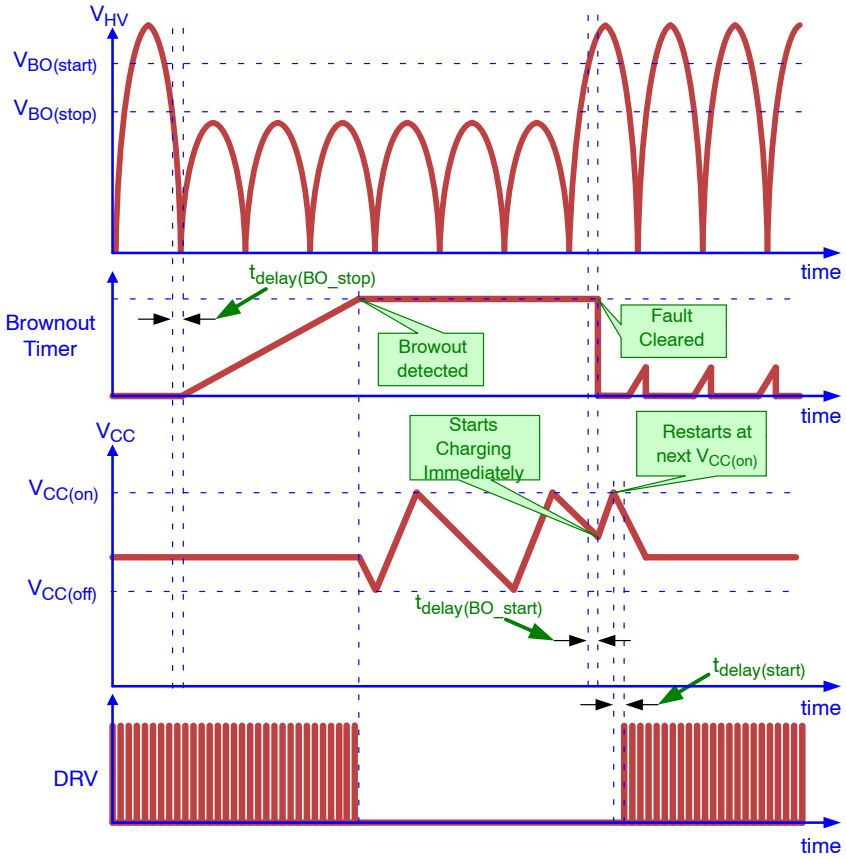


Figure 8. BIBO Operating Waveform

INPUT FILTER CAPACITOR DISCHARGE

Another feature of the NCP1945 is the capability to detect the presence of an AC input voltage, and to discharge the EMI line filter capacitors if the device determines that the AC input has been disconnected. Discharging of the line filter capacitors is a regulatory requirement to ensure safe handling of off-line plug-in applications. This requirement is not necessary for all AC-DC applications and the discharge feature can be disabled if it is not required.

To accomplish the line filter capacitor discharge, the NCP1945 incorporates a slope detection circuit to detect the removal of AC input, and an active discharge circuit, both through the HV pin. The slope detection circuit works by digitally sampling the voltage present at the HV pin and monitoring the magnitude of the slope on successive samples. A timer, $t_{line(removal)}$ (typically 100 ms), starts running when the slope magnitude of the input signal is below a minimum level. The timer is reset by the upslope detection reset timer $t_{HV(up)}$ (typically 1 ms) or the downslope detection reset timer $t_{HV(down)}$ (typically 14 ms). Line removal operation is illustrated in Figure 9.

Once the timer expires, a line removal condition is acknowledged, disabling the controller and initiating an HV discharge cycle. The discharge cycle begins by ensuring V_{CCL} is below the $V_{CC(on)}$ threshold. $I_{CC(disch)}$, typically 18 mA, brings the V_{CCL} voltage to the necessary level to execute the input capacitor discharge phase. During the discharge phase, the HV discharge current source $I_{HV(disch)}$ (typically 2 mA) is activated. The current source $I_{HV(disch)}$ remains active and constant until V_{HV} drops to $V_{HVdisch(MIN)}$ (typically 40 V). At this point, it begins to pinch off until the discharge phase completes when V_{HV} drops to $V_{HVdisch(end)}$ (typically 30 V). Once the discharge phase completes, a new start-up cycle commences as normal. In the event that line voltage is reapplied during a discharge phase, the circuit will simply continue to discharge until the line zero crossing occurs, at which point V_{HV} will drop to $V_{HVdisch(end)}$ and a new start-up cycle will commence. An illustration of the capacitor discharge operation is shown in Figure 10. *It is important to note that the HV pin cannot be connected to a DC voltage if the line discharge feature is enabled in the device option.*

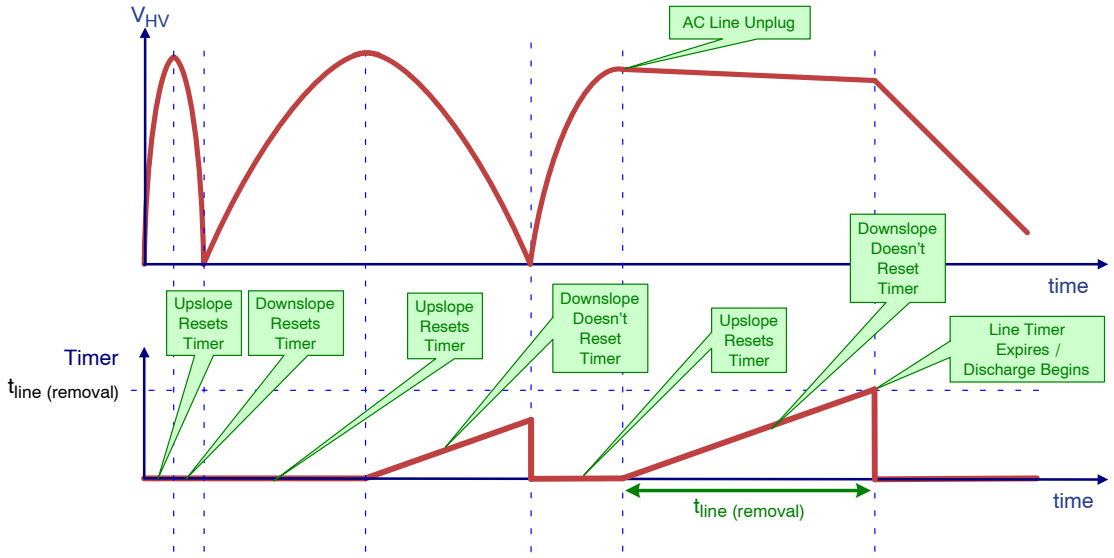


Figure 9. AC Line Removal Detection

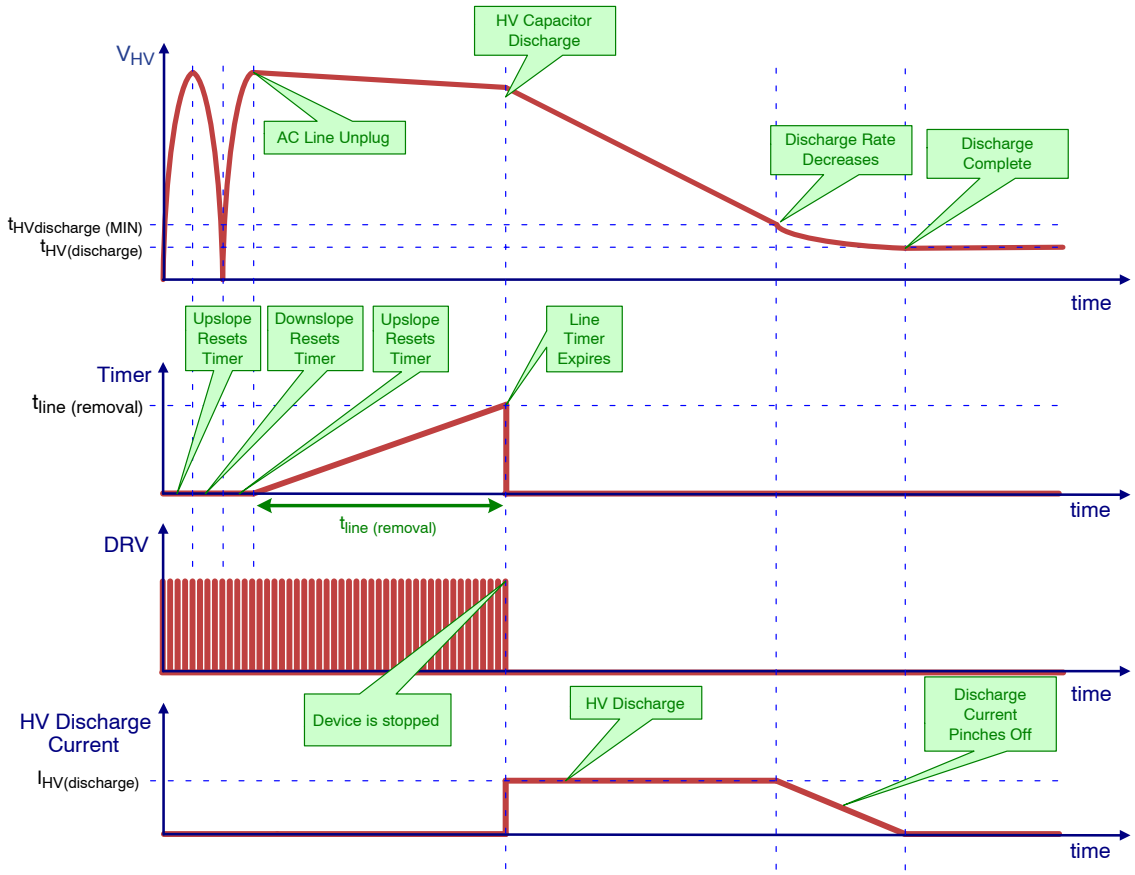


Figure 10. Input Filter Capacitor Discharge Operation

QR FLYBACK OPERATION AND FUNCTIONS

Feedback Interface

The NCP1945 QR feedback interface features a resistor pullup network as shown in Figure 11. In this architecture the QFB pin is supplied by a 5 V rail through a 20 kΩ pullup resistor, R_{QFB}. The QFB pin open circuit voltage, $V_{QFB(open)}$, is specified as a typical value of 5 V.

Internally the voltage at the QFB pin is divided down by a factor of K_{QFB}, typically 3 or 4, depending on the version of the device. The voltage directly at the QFB pin is fed into the skip and valley selection comparators while the divided down signal is fed into the PWM comparator for on time modulation.

The resistor pullup is a conventional voltage-controlled architecture which translates the error signal communicated through the optocoupler into an error voltage that controls the duty cycle of the SMPS. A capacitor to GND can be placed in parallel to the collector of the optocoupler to control the location of the optocoupler pole. Due to the resistance of R_{QFB}, the optocoupler pole will typically be in the range of 2 kHz to 4 kHz which limits the closed loop bandwidth of the SMPS in the range of 1–2 kHz. The capacitor placed in parallel to the collector of the optocoupler will typically be in the range of 470 pF to 4.7 nF with 1 nF being a fairly common value.

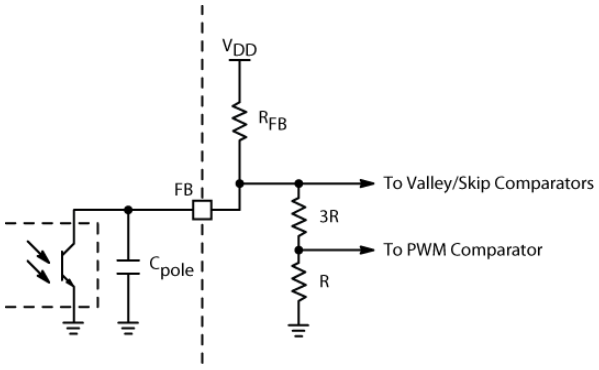


Figure 11. Pull-up Resistor FB Interface

ON TIME CONTROL

Peak Current Control

The NCP1945 uses peak current-mode control on the QR flyback stage, which means that the QFB voltage sets the peak current flowing in the transformer and the MOSFET. This is achieved by sensing the MOSFET current across a resistor and applying the resulting voltage ramp to the non-inverting input of the PWM comparator through the QCS pin. The current limit threshold is set by applying the QFB voltage divided by K_{QFB}, typically 3 in PEM enabled OPNs, to the inverting input of the PWM comparator. When the current sense voltage ramp exceeds this threshold, the output driver is turned off. Additionally, the peak current is affected by several functions, as shown in Figure 12.

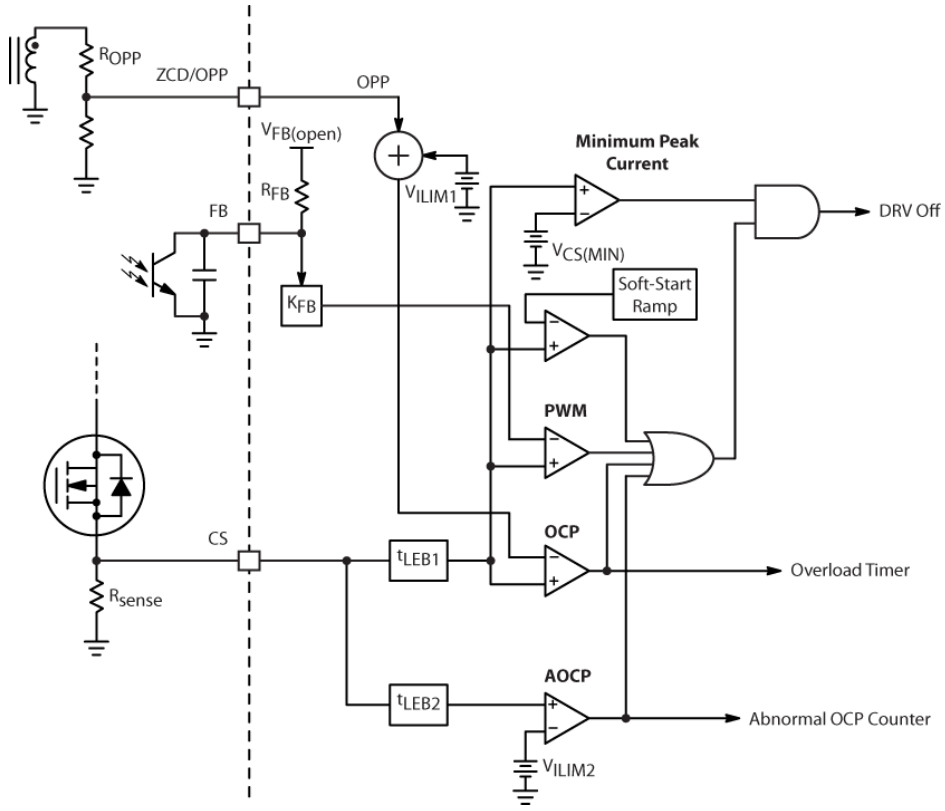


Figure 12. Peak Current Setpoint of the QR Flyback Stage

The peak current level is clamped during the soft-start phase. The setpoint is actually limited by a clamp level ramping from 0 to 1 V within 4 ms.

In addition to the PWM comparator, a dedicated comparator monitors the current sense voltage, and if it reaches the maximum value, V_{QILIM1} (typically 1 V), the gate driver is turned off and the overload timer is enabled. This occurs even if the limit imposed by the feedback voltage is higher than V_{QILIM1}.

Due to the parasitic capacitances of the MOSFET, a large voltage spike often appears on the QCS Pin at turn-on. To prevent this spike from falsely triggering the current sense circuit, the current sense signal is blanked by a leading edge blanking (LEB) circuit, t_{QLEB1}, typically 275 ns. The NCP1945 also sets a minimum peak level, $V_{QCS(MIN)}$, that must be exceeded every switching cycle. This results in higher efficiency at light loads by increasing the minimum energy delivered per switching cycle, while reducing the overall number of switching cycles during light load.

Soft-Start

Soft-start is achieved by ramping up an internal reference and comparing it to the current sense signal. The internal reference ramps up from 0 V once the controller initially powers up. The peak current setpoint is then limited by the generated reference voltage ramp resulting in a gradual increase of the switch current during startup. The soft-start duration, t_{SSTART}, is nominally 4 ms. During startup, demagnetization phases are long and difficult to detect since the auxiliary winding voltage is very small. In this condition, the 6 µs steady-state timeout is generally shorter than the inductor demagnetization period. If it is used to restart a switching cycle, it can cause operation in CCM for several cycles until the voltage on the QZCD pin is high enough to prevent the timer from running. Therefore, a longer timeout period of 100 µs, $t_{(tout1)}$, is used during soft-start to prevent CCM operation.

Frequency Jittering

In order to help meet stringent EMI requirements, the NCP1945 features frequency jittering to average the energy peaks over the EMI frequency range. The function consists of summing a 0 to 100 mV, 3.9 kHz triangular wave V_{jitter} with the QCS signal immediately before the PWM comparator. This current acts to modulate the on time and hence the operation frequency.

Since the jittering function modulates the peak current level, the QFB signal will attempt to compensate for this effect in order to limit the output voltage ripple. Therefore, the bandwidth of the feedback loop must be well below the jitter frequency, or the jitter function will be filtered by the loop. Due to the frozen peak current, the effect of the jittering circuit may not be seen during frequency foldback mode.

OFF TIME CONTROL

Zero Current Detection

In a quasi-resonant flyback, the power switch turn-off is determined by the peak current set by the feedback loop, the switch turn-on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized has the benefit of reduced switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the lump capacitance of the drain of the FET, eventually settling at the input voltage. A QR flyback controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce switching losses and electromagnetic interference (EMI). A valley is detected once the QZCD pin voltage falls below the demagnetization threshold, $V_{QZCD(trig)}$, typically 60 mV. The controller will either switch once the valley is detected or increment the valley counter, depending on the QFB voltage.

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be used to limit the operating frequency. However, when used by itself, such an approach often causes instabilities since when this clamp is active, the controller tends to jump (or hesitate) between two valleys, thus generating audible noise. Instead, the NCP1945 incorporates a patented valley lockout (VLO) circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. This technique extends the QR mode operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency. The operating valley (1st, 2nd, 3rd, 4th, 5th or 6th) is determined by the QFB voltage. An internal counter increments each time a valley is detected by the QZCD pin. Figure 13 shows a typical frequency characteristic obtainable at low line in a 100 W application without PEM.

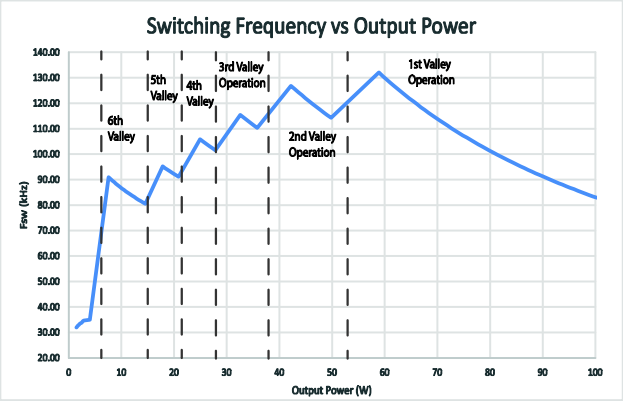


Figure 13. Valley Lockout Frequency vs. Output Power for 100 W Application

Once a valley is asserted by the valley selection circuitry, the controller is locked in this valley until the QFB voltage rises or falls enough for the next valley to be selected. For example, if a NCP1945AA sees 1.2 V on QFB, and is operating in the 2nd valley, it will remain in that valley until it hits 1.65 V on QFB, and moves to first valley operation, or until it hits 0.9 V on QFB, in which case it moves to third valley operation. Tables 7 and 8 show the thresholds for each valley for both PEM and non-PEM OPNs. The regulation loop adjusts the peak current to deliver the necessary output power. Each valley selection comparator features a 600 mV hysteresis that helps stabilize operation despite the QFB voltage swing produced by the regulation loop.

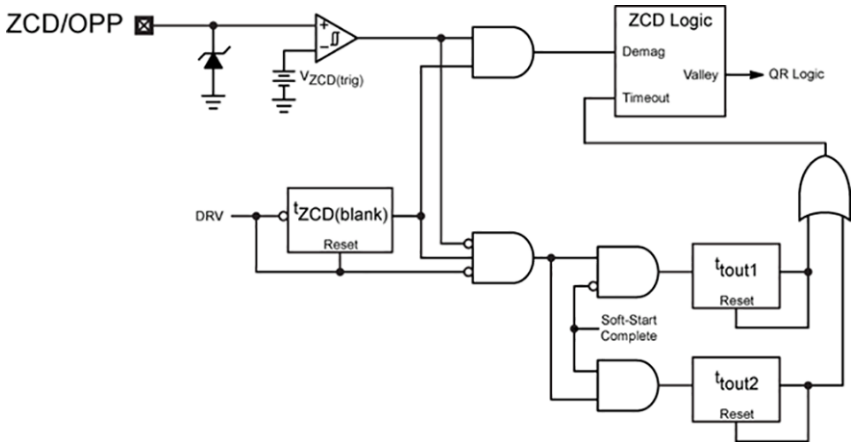


Figure 14. Valley Timeout Circuitry

Valley Timeout

In case of extremely damped oscillations, the QZCD comparator may not be able to detect the valleys. In this condition, drive pulses may stop while the controller waits for the next valley or ZCD event. The NCP1945 ensures continued operation by incorporating a maximum timeout period after the last demagnetization detection. The timeout signal acts as a substitute for the QZCD signal to the valley counter. Figure 14 shows the valley timeout circuit schematic. The steady state timeout period, $t_{(tout2)}$, is set at 6 μs to limit the frequency step.

During startup, the reflected voltage at the QZCD pin may not be high enough for the QZCD comparator to accurately detect valleys. In this condition, the steady state timeout period may be shorter than the inductor demagnetization period causing CCM operation. CCM operation lasts for a few cycles until the voltage on the QZCD pin is high enough to detect the valleys. A longer timeout period, $t_{(tout1)}$, of 100 μs is set during soft-start to limit CCM operation.

In VLO operation, the number of timeout periods are counted instead of valleys when the drain-source voltage oscillations are too damped to be detected. For example, if the QFB voltage sets VLO mode to turn on at the fifth valley, and the QZCD ringing is damped such that the QZCD circuit is only able to detect:

- Valleys 1 to 4: the circuit generates a DRV pulse 6 μs (steady-state timeout delay) after the 4th valley detection.
- Valleys 1 to 3: the timeout delay must run twice, and the circuit generates a DRV pulse 12 μs after the 3rd valley detection.

LIGHT LOAD MANAGEMENT

Frequency Foldback with Rapid Frequency Foldback (RFF)

As the output load decreases (QFB voltage decreases), the valleys are incremented from 1 to 6. When the sixth valley is reached and the QFB voltage further decreases to 0.6 V, the minimum peak current setpoint is increased by $V_{RFF(delta)}$ (0.4 V typically), and the controller enters frequency foldback mode (FF). The increase in peak current serves to force the switching frequency to a much lower value, thus improving efficiency at light loads. During this mode, the controller regulates the power delivery by modulating the switching frequency.

Once in frequency foldback mode, the controller reduces the switching frequency by adding dead time after the 6th valley is detected. This dead time increases as the QFB voltage decreases.

The dead time circuit is designed to add zero dead-time when V_{QFB} = 0.6 V and linearly increases the total dead time to $t_{DT(MAX)}$ (32 μs minimum) as QFB falls to 0.3 V. The minimum frequency clamp prevents the switching frequency from dropping below 25 kHz to eliminate the risk of audible noise. Note that the dead time is not added until the device is in RFF to ensure valley switching and prevent reduction of the RFF entry load threshold.

In addition to dead time, the peak current setpoint is linearly reduced as QFB falls to 0.3 V. This ensures that the peak current is not too high during the lightest loads and has the effect of reducing the skip entry power level.

To reduce the hysteresis between entering and exiting RFF, the exit threshold is actually slightly below the entry threshold (0.55 V). A 1 ms timer, t_{RFF}, is engaged every time RFF is entered or exited to prevent oscillations during the operating point transition. If at any time QFB falls to skip mode, or rises to 5th valley, RFF will be immediately exited regardless of the state of the lockout timer. Figure 15 summarizes the VLO to foldback operation with respect to the QFB voltage.

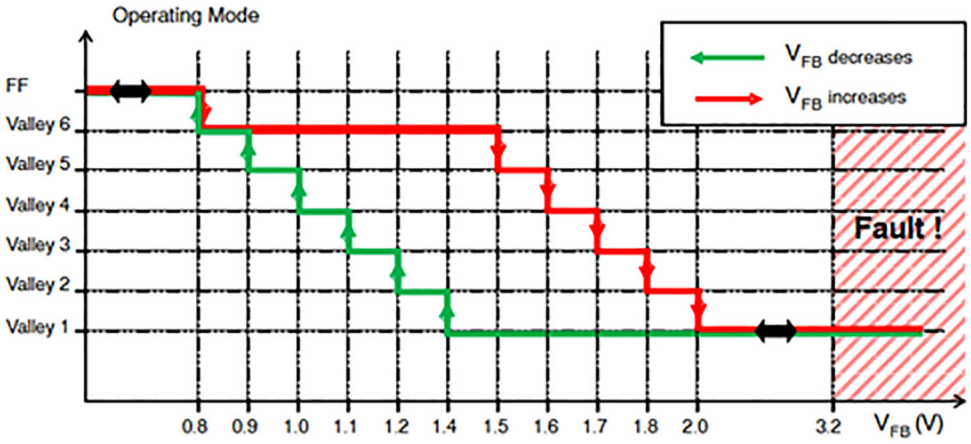


Figure 15. Valley Lockout Thresholds

Table 7. NCP1945 VALLEY FB THRESHOLDS NOMINAL VALUES FOR OPN LA

FB Falling		FB Rising	
1st to 2nd valley	1.400 V	2nd to 1st valley	2.000 V
2nd to 3rd valley	1.200 V	3rd to 2nd valley	1.800 V
3rd to 4th valley	1.100 V	4th to 3rd valley	1.700 V
4th to 5th valley	1.000 V	5th to 4th valley	1.600 V
5th to 6th valley	0.900 V	6th to 5th valley	1.500 V

Table 8. NCP1945 VALLEY FB THRESHOLDS NOMINAL VALUES FOR OPNs AA, BA, FA

FB Falling		FB Rising	
1st to 2nd valley	1.050 V	2nd to 1st valley	1.650 V
2nd to 3rd valley	0.900 V	3rd to 2nd valley	1.500 V
3rd to 4th valley	0.825 V	4th to 3rd valley	1.425 V
4th to 5th valley	0.750 V	5th to 4th valley	1.350 V
5th to 6th valley	0.675 V	6th to 5th valley	1.275 V

Minimum Frequency Clamp and Skip Mode

As mentioned previously, the circuit prevents the switching frequency from dropping below Qf_{MIN} (25 kHz typical). When the switching cycle would be longer than 40 μs, the circuit forces a new switching cycle. However, the f_{MIN} clamp cannot generate a QDRV pulse until the demagnetization is completed. In other words, it will not cause operation in CCM. Since the NCP1945 forces a minimum peak current and a minimum frequency, the power delivery cannot be continuously controlled down to zero. Instead, the circuit starts skipping pulses when the QFB voltage drops below the skip level, V_{QSKIP}, and recovers operation when QFB exceeds V_{QSKIP_EXIT}. This skip mode method provides an efficient method of control during light loads.

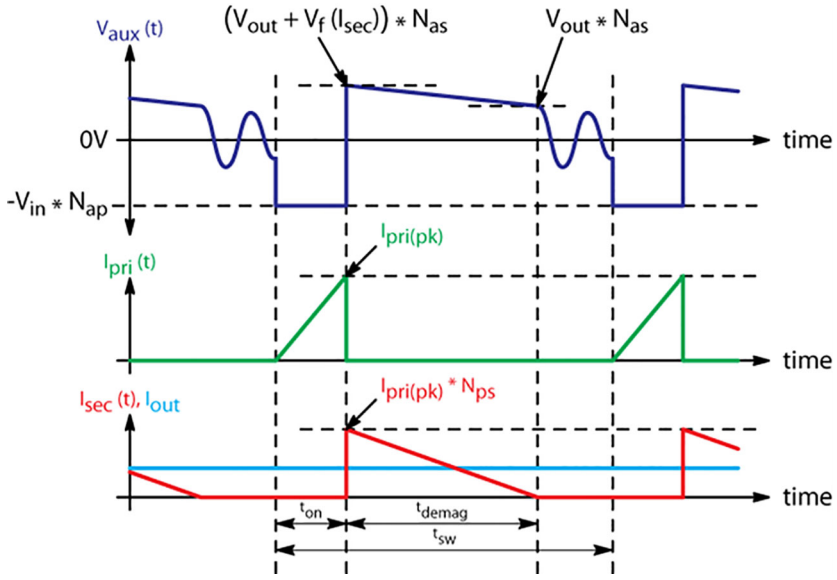


Figure 16. Output Voltage Sensing Waveforms

Overpower Protection

The peak value of the AC line input voltage is sensed by the HV Pin, and internally scaled down to a smaller level for OPP. The OPP signal is then added to each of the comparators – QILIM1, QCS(MIN), and Iout(limit). The QZCD pin has three functions. The primary function is to detect the demagnetization of the transformer. The second function is to set the OPP gain via external resistor Ropp. During startup, a 20 μA current is sourced from the ZCD pin to generate a voltage across the Ropp resistor. The voltage across the Ropp resistor determines the maximum possible OPP amount that will be added. The typical values of OPP vs. R OPP for given input voltages are shown in Figure 17.

The third function is to sense the output voltage during the drive off-time, and route it to the CS(MIN) comparator. During operation, an internal 1k resistor is connected in parallel with the Ropp resistor to create a 2:1 ratio for output voltage sensing. A current source provides error correction over the output voltage range.

Figure 17. OPP Voltage vs. R_{OPP} for Different Input Voltages

Table 9. NCP1945 Vcs BINNING

Vout	$V_{QZCD(hi)}$	BIN#	To	Vs Threshold			VQCSMIN (mV)		
				MIN	TYP	MAX	MIN	TYP	MAX
≥20	9.75	17					180	200	220
			16to17	9	9.5	10			
19	9.25	16					175	195	215
			15to16	8.5	9	9.5			
18	8.75	15					170	190	210
			14to15	8	8.5	9			
17	8.25	14					165	185	205
			13to14	7.5	8	8.5			
16	7.75	13					160	180	200
			12to13	7	7.5	8			
15	7.25	12					155	175	195
			11to12	6.5	7	7.5			
14	6.75	11					145	165	185
			10to11	6	6.5	7			
13	6.25	10					141	160	179
			9to10	5.5	6	6.5			
12	5.75	9					136	155	174
			8to9	5	5.5	6			
11	5.25	8					131	150	169
			7to8	4.5	5	5.5			
10	4.75	7					121	140	159
			6to7	4	4.5	5			
9	4.25	6					116	135	154
			5to6	3.5	4	4.5			
8	3.75	5					106	125	144
			4to5	3	3.5	4			
7	3.25	4					102	120	138
			3to4	2.5	3	3.5			
6	2.75	3					92	110	128
			2to3	2	2.5	3			
5	2.25	2					82	100	118
			1to2	1.5	2	2.5			
4	1.75	1					72	90	108
			0to1	1.075	1.575	2.075			
≤3.3	1.4	0					63	80	97

Gate Drive

Weak Gate Drive

Due to the loss of valley switching during frequency foldback, the output rectifier can be subjected to large voltage spikes during the primary switch turn-on. The NCP1945 includes special circuitry to reduce the driver turn-on strength during frequency foldback and thus reduce the severity of the secondary voltage spike. The sourcing current for the QDRV is reduced from 500 mA to 50 mA. The circuitry is only active while in 5th, 6th valley, and frequency foldback. This feature is only available in versions FA and LA.

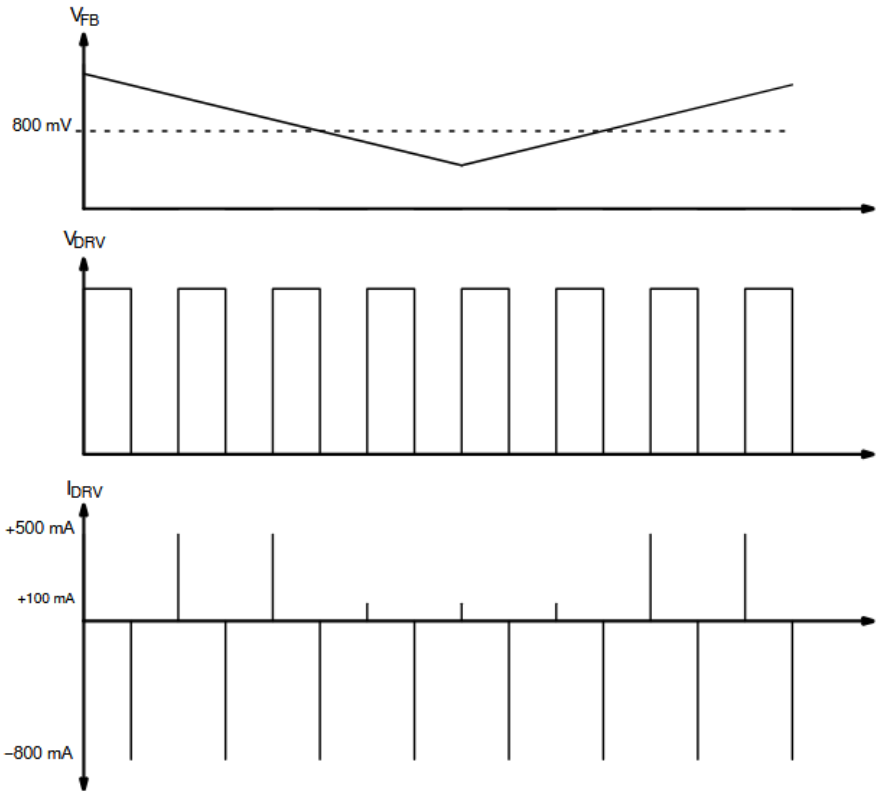


Figure 18. Adaptive Gate Drive Current

Low Drive

The device integrates a dedicated low voltage gate driver optimized for direct interface with Gallium Nitride (GaN) transistors. Unlike traditional silicon MOSFETs, which typically require 10–12 V of gate drive, GaN devices typically have a 6V gate voltage.

To ensure safe operation, the controller provides a regulated 6.5 V output to both the PFC and the QR drive pins. To ensure fast switching and minimize ringing, drive circuitry typically features an inline diode to separate the turn on and turn off paths of the drive current. The 6.5 V drive clamp voltage compensates for the voltage drop across this diode. The lower drive voltage allows the NCP1945 to directly drive GaN devices without the need for external level shifting or voltage clamping components. This can reduce costs and can improve efficiency in higher frequency designs. Version BA is designed for USB-PD applications with GaN FETs.

Power Excursion Mode (PEM)

When the power demand exceeds the maximum power limit, the NCP1945 linearly increases the switching frequency, forcing the QR stage into CCM. The switching frequency can be increased up to 2.5x, thus eliminating the need for a larger transformer. In addition to the frequency scaling, the peak current threshold is increased by 50%, which makes it such that 2x the typical max power can be delivered. This makes it possible to have a significantly smaller transformer than a converter that remained in QR mode.

The NCP1945 contains a register to store the off time during QR mode. During each switching period, the off time is measured and the register is updated. As long as the PEM comparator is not tripped, this operation will continue indefinitely. When the PEM comparator is tripped (due to an increase in power demand), the NCP1945 will enter PEM on the following cycle. During PEM, the stored value in the

off-time register becomes a maximum off-time clamp, and when that clamp is reached, the next drive cycle will commence. Since the demagnetization time of a QR flyback is directly proportional to the load, as the load increases, the system will naturally enter CCM with a fixed off time. The switching frequency is then determined by the on time (which increases with load) and the fixed off time. This operation alone provides a 1.5x power increase.

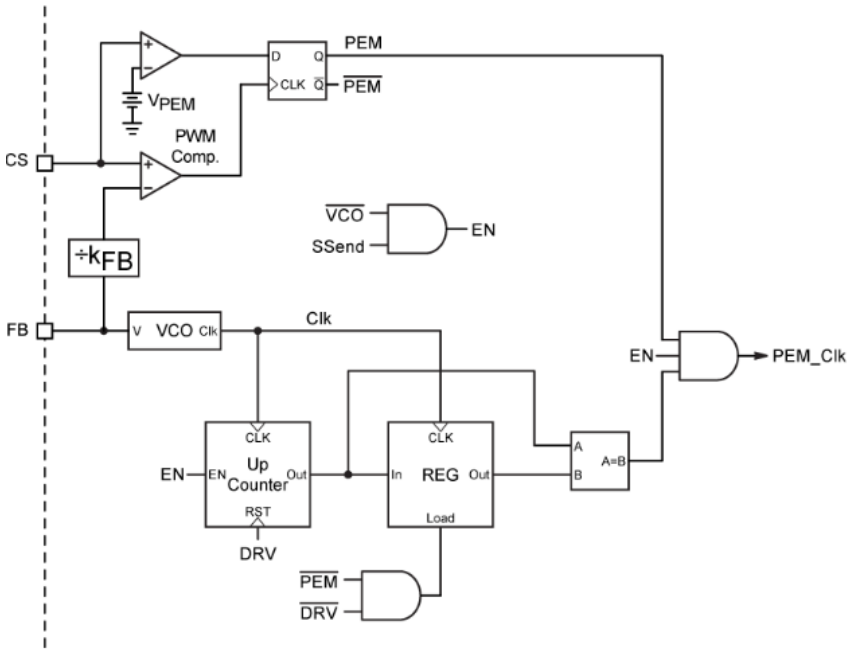


Figure 19. PEM Block Diagram

In order to achieve 2x power, the off-time clamp is decreased linearly as the FB voltages increases. This has the effect of increasing the switching frequency to boost the output power. The frequency continues to be scaled until the maximum switching frequency or the maximum feedback voltage, $V_{QFB(MAX)}$ (3.5 V typical), is reached. This operation continues as long as the controller remains in PEM, and the PEM comparator is tripped before each drive turnoff. Once a drive turnoff occurs without first tripping the PEM comparator, PEM is exited immediately (in the same cycle), and the controller immediately defaults back to QR mode with the next switching cycle starting at the ZCD transition. Since CCM operation is maintained via off-time modulation instead of fixed-frequency duty cycle modulation, the system is naturally immune to subharmonic oscillations and slope compensation is not required.

In addition to operation in CCM, the NCP1945 contains a maximum QCS setpoint, V_{QILIM1} (typically 1.0 V), to allow a 25% increase in peak current. When this comparator triggers, the drive pulse is terminated. This corresponds to a QFB voltage of 3 V (typical). The VILIM1 comparator shares the same LEB as the VPEM comparator. While QFB voltages higher than 3 V will not cause any additional increase in peak current, the switching frequency continues to increase until the QFB pin reaches $V_{QFB(MAX)}$. At this point, the switching frequency will be scaled by a maximum value of $K_{scale(MAX)}$, provided $F_{MAX(PEM)}$ has not been reached. Figure 19 shows the block diagram for the PEM circuit.

Whenever the drive is low and the PEM flag is not set, the PEM counter value is continuously updated in the PEM register. When the drive is high, the PEM counter is held reset. The V_{PEM} comparator monitors the QCS signal and outputs to a D flip-flop that is clocked by the PWM comparator. If the QCS signal reaches V_{PEM} (800 mV typical) prior to the DRV going low (the PEM comparator is tripped) the PEM flag is set high. When the PEM flag is set, the PEM register no longer updates the value from the PEM counter. It is instead stored as the maximum off-time and the next drive pulse will not start until the PEM counter reaches the maximum off-time stored in the PEM register, or a QZCD transition is detected. This has the effect of setting a minimum frequency clamp. As the power demand increases, so does the QFB voltage. As the QFB voltage increases, the counter speed increases linearly. This causes the maximum off-time to decrease and consequently the minimum frequency clamp to increase. This continues until the maximum switching frequency or the maximum feedback voltage, $V_{FB(MAX)}$ (3.5 V typical), is reached. This operation continues as long as the PEM flag is set. The PEM flag is cleared immediately once the drive transitions low without first tripping the PEM comparator. Once the PEM flag is cleared, PEM is exited, and the PEM timer output is disabled. The controller immediately defaults back to QR

mode with the next switching cycle starting at the QZCD transition.

PEM is disabled during soft-start and cannot be enabled until the PEM comparator is not tripped for one cycle. Figure 20 shows the timing diagram for PEM operation with frequency scaling and increased peak current limit.

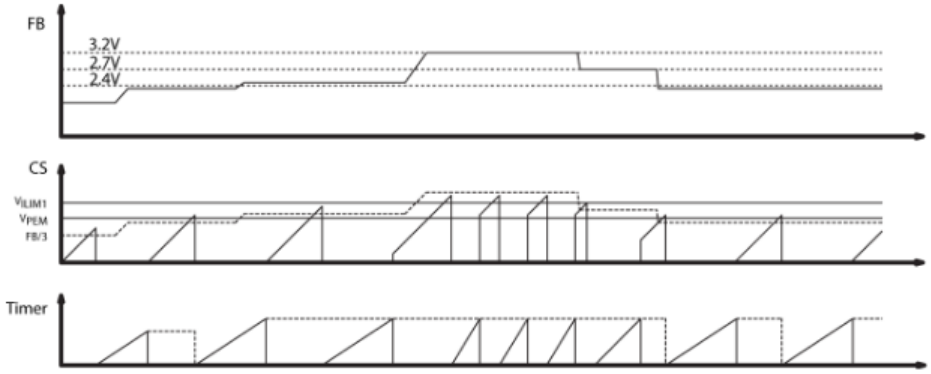


Figure 20. Timing Diagram of PEM Operation with Frequency Scaling

Constant Current Overload

Some regulations such as that for a Limited Power Source (LPS) require the output current and power to be limited during all conditions. In particular, LPS requires that the output power must be limited to 100 W, and the output current to 8 A after 5 seconds at all times, including during a single fault condition.

In order to maintain a constant output current limit across multiple output voltages, the NCP1945 incorporates a special auto-tuning output current limit circuit. This function monitors the feedback voltage, transformer demagnetization time, and the user-programmed current-limit setting on the CCOVLD pin to generate an internal reference feedback voltage. This internal reference, $V_{QFB(OVLD)}$ represents the maximum allowable operating point for the converter. If the QFB pin voltage exceeds $V_{QFB(OVLD)}$, an overload condition is detected and the t_{OVLD} timer begins. If the overload condition continues for 160 ms, the device turns off both drives and enters auto-recovery mode. To limit thermal stress on the components, the controller remains off for 2 seconds ($T_{RESTART}$) before attempting to auto-recover.

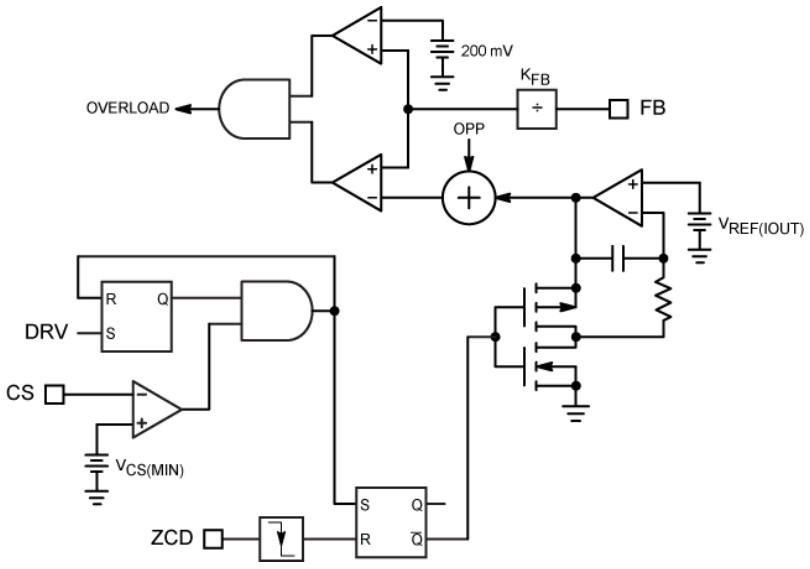


Figure 21. Output Current Limit Schematic

PFC OPERATION AND FUNCTIONS

Frequency Control

Valley Synchronized Frequency Foldback (VSFF)

The NCP1945 implements the Valley Synchronized Frequency Foldback (VSFF) which consists of operating the PFC stage in critical conduction mode (CrM) until the power drops below the frequency foldback threshold. As the power is further reduced the PFC stage enters discontinuous conduction mode (DCM) with an added dead time which gets longer. The output of the regulation error amplifier V_{PCTRL} is used to select the operation mode and to adjust the dead-time duration. The circuit enters DCM when V_{PCTRL} drops below the frequency foldback enter threshold, $V_{PCTRL(FF)}$. The device will remain in this mode until V_{PCTRL} increases past the frequency foldback exit threshold. The frequency foldback exit threshold is $V_{PCTRL(FF)} + V_{PCTRL(FF)hys}$. The 100 mV of hysteresis between the enter and exit threshold is there to prevent an unstable condition where rapidly switching between DCM and CRM occurs. Figure 22 demonstrates the addition of dead time as V_{PCTRL} decreases.

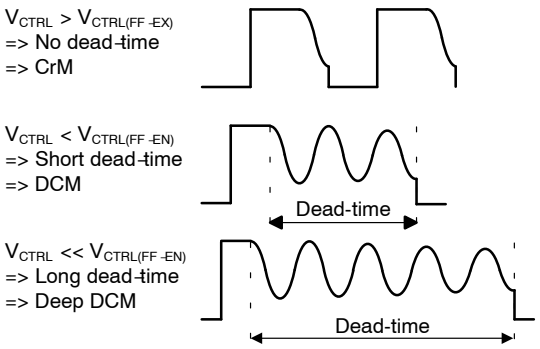


Figure 22. Drain Voltage in VSFF

In addition to the operation mode, V_{PCTRL} also determines the turn-on time, t_{on}, in voltage mode control. The on time will be proportional to $V_{PCTRL} - V_{CPTRL(min)}$. This relationship can be used to determine the input power of the PFC, as shown below.

$$P_{IN} = \frac{V^2_{IN.RMS}}{2L} \times \frac{t_{on(max)} \times \left(V_{PCTRL} - V_{PCTRL(min)}\right)}{\left(V_{PCTRL(max)} - V_{PCTRL(min)}\right)} \quad \text{(eq. 2)}$$

Typically, the frequency foldback threshold is 1.55 V, meaning the device will enter DCM when input power is:

$$P_{IN} = \frac{V^2_{IN.RMS}}{2L} \times 0.2625\ V \quad \text{(eq. 3)}$$

To further improve efficiency, the MOSFET turn on is delayed until the drain-source voltage is at its next valley. Practically, this means that after the dead time determined by V_{PCTRL} expires, the circuit will hold off drive run on until the next valley is detected. The NCP1945's on time modulation will adjust the drive turn on times to compensate for the added dead times in DCM such that the device always has near unity power factor.

Minimum Switching Frequency

Frequency foldback reduces the switching frequency as the load decreases to optimize the efficiency across a wide range of load conditions. However, an internal minimum frequency logic limits the switching frequency above the audible frequency.

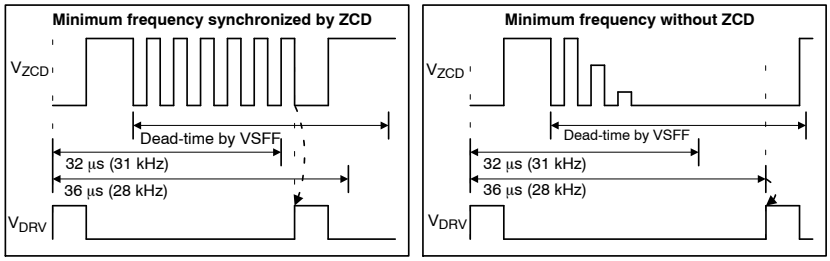


Figure 23. Minimum Switching Frequency

The operation of the minimum switching frequency clamp is shown in Figure 23. At drive turn on, a 32 µs timer is started. After 32 µs, the device will begin to look for the next valley to turn on the next pulse. If no valleys are detected, then PDRV is forced high at 36 µs regardless of the drain-souce voltage. This ensures that the minimum frequency is between 31 kHz (32 µs switching period) if a valley is immediately detected and 28 kHz (36 µs switching period) if no valley can be detected. However, if the circuit cannot detect any PZCD signal at all during drive turn-off time, the circuit will not generate any PDRV pulses until the 200 µs PZCD watchdog time has elapsed.

ON-TIME MODULATION

When the FET is on, the inductor current of a CrM/DCM PFC boost stage starts from zero and ramps up. The slope of the ramp is defined by V_{IN}/L where L is the boost inductance. At the end of the on time (t_1), the inductor starts to demagnetize. t_2 is defined as the time it takes for the inductor current to ramp to zero. At that point if the circuit is in CRM, a new switching cycle starts. When in DCM, the dead time t_3 is generated. This operation is demonstrated in Figure 24.

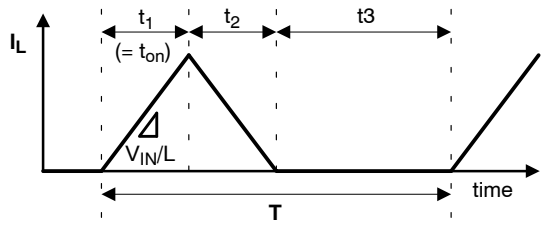


Figure 24. Inductor Current in DCM

It can be shown that the input current is defined by the following equation:

$$I_{in} = V_{in} \times \frac{t_1 \times (t_1 + t_2)}{2 \times L \times T} = V_{in} \times \frac{t_{on} \times (t_1 + t_2)}{2 \times L \times T} \quad \text{(eq. 4)}$$

Where $T = t_1 + t_2 + t_3$, is the switching period. From this equation it can be determined that V_{in} is proportional to I_{in} when $t_{on} \times (t_1 + t_2)/T$ is a constant. In voltage mode control, without on time modulation, the on time is determined by:

$$t_{on} = t_{on(max)} \times \frac{\left(V_{PCTRL} - V_{PCTRL(min)}\right)}{\left(V_{PCTRL(max)} - V_{PCTRL(min)}\right)} \quad \text{(eq. 5)}$$

It should be noted that the NCP1945 features a level line feed forward. The $t_{on(max)}$ at low line is 2.5x longer than at high line.

To keep $t_{on} \times (t_1 + t_2)/T$ constant, the on time for each cycle is modulated by the factor $T/(t1 + t2)$ determined from previous switching cycle. After t_{on} modulation, the on time is determined by the following equation:

$$t_{on} = t_{on(max)} \times \frac{\left(V_{PCTRL} - V_{PCTRL(min)}\right)}{\left(V_{PCTRL(max)} - V_{PCTRL(min)}\right)} \times \frac{T}{t_1 + t_2} \quad \text{(eq. 6)}$$

Combining Equation 4 and Equation 6, the final equation for the input current can be solved for:

$$I_{in} = \frac{V_{in} t_{on(max)}}{2 \times L} \times \frac{\left(V_{PCTRL} - V_{PCTRL(min)}\right)}{\left(V_{PCTRL(max)} - V_{PCTRL(min)}\right)} \quad \text{(eq. 7)}$$

This allows the NCP1945 to operate in both DCM and CRM without any power factor degradation, and no discontinuity in the power delivery.

Feedback Regulation

OTA and VPCTRL Function

The NCP1945 features a transconductance error amplifier (OTA) with the inverting input on the PFB pin and the output is connected to PCTRL as shown in Figure 25. It features a reference voltage for output regulation, a typical transconductance gain of 200 μS and a maximum capability of about ±20 μA OTA output current. The output of the error amplifier for external loop compensation. Typically, a type-2 network is applied between the PCTRL pin and ground to set the regulation bandwidth below about 20 Hz. P_{CTRL} controls turn-on time, dead time in VSFF, skip mode and Static OVP. The following are some points to note about PCTRL:

- Turn on time is proportional to $V_{PCTRL} - V_{PCTRL(min)}$ as described in the On Time Modulation section.
- Added dead time is lengthened as V_{PCTRL} is lowered from $V_{PCTRL(FF)}$.
- V_{PCTRL} is pulled down by a 30 μA current source $I_{PCTRL(BO)}$ when exiting normal operation. This current source is a soft stop discharge current. If V_{PCTRL} is lower than $V_{PCTRL(min)}$ while $I_{PCTRL(BO)}$ is enabled, Static OVP is triggered and NCP1945 shuts off.

Boost Follower Operation

At low line, a boost follower reduces the PFC bulk voltage to optimize the PFC stage efficiency and shrink its size and cost. In particular, the boost inductance and the MOSFET losses can be dramatically reduced. Since the output voltage must remain higher than the line voltage, the output voltage is lowered only in low line, while it remains regulated to the default nominal level generally set to 400 V in high-line conditions. Practically, the IC controls this 2-level follower boost operation through the reference voltage on the error amplifier. For versions AA and BA, V_{pref} at low line is 1.6 V. For FA, it is 1.8 V, and for LA, boost follower is disabled, so V_{PREF} is 2.5 V at all line voltages.

Feedback Transient Control

The NCP1945 features multiple protection and enhancement features for improved performance and robustness of the application. The soft and fast OVP, UVP and DRE comparators monitor the sampled PFB pin voltage.

Soft-start

At startup, $I_{PCTRL(START)}$ provides the current to build up voltage in an external compensation capacitor in a controller manner. As the PFB voltage reaches V_{PREF}, the sourcing current of the OTA is reduced to zero. Then the PFCOK internal signal is set high and $I_{PCTRL(START)}$ is turned off.

Dynamic Response Enhancer (DRE)

The transient response of PFCs are inherently slow because the voltage loop must operate below line frequency to preserve line current shape. But that makes PFCs susceptible to output voltage dropouts at abrupt increases of load current. To deal with this issue, the NCP1945 features a Dynamic Response Enhancer (DRE). An internal comparator monitors the PFB pin and when the voltage drops 112 mV below V_{PREF}, $I_{PCTRL(DRE)}$, a 200 μA current source, is turned on to speed up the charge of the compensation network. This is shown in Figure 25 below. Effectively, this appears as a 10x increase in the loop gain. DRE is disabled during the start-up sequence until the PFC stage has stabilized and PFCOK is high.

Soft / Fast Over Voltage Protection (SOVP, FOVP)

In certain cases of high load to low load transition or line level change, the bulk voltage can go above the regulation level, triggering over voltage protection. In such cases of overshoot, soft OVP is first triggered by comparing the PFB voltage and the soft OVP threshold as shown in Figure 25. Once soft OVP is triggered, the turn-on time is gradually decreased in 4 to 5 switching periods to smoothly reduce powering. If bulk voltage rises faster and reaches the fast OVP threshold, then switching is immediately disabled. The Fast OVP comparator trips when the feedback voltage exceeds V_{PREF} by $\Delta V_{FastOVP}$. For both fast and soft OVP, there is a 50 mV hysteresis that determines the threshold at which OVP is exited. At low-line condition with boost follower enabled, soft and fast OVP thresholds, $V_{softOVP\_LL}$ and $V_{fastOVP\_LL}$, are increased. The NCP1945 triggers DRE, soft OVP and fast OVP at the thresholds below levels:

- DRE:
  - $\Delta V_{DRE\_EN}/\Delta V_{DRE\_DIS} = V_{ref} - 112$ mV/63 mV
- Soft OVP:
  - $\Delta V_{softOVP\_HL} = V_{ref} + 125$ mV
  - $\Delta V_{softOVP\_LL} = V_{ref} + 250$ mV
- Fast OVP:
  - $\Delta V_{FastOVP\_HL} = V_{ref} + 175$ mV
  - $\Delta V_{FastOVP\_HL} = V_{ref} + 350$ mV

Where $V_{SoftOVP\_LL}$ and $V_{FastOVP\_LL}$ are set at low line when Boost Follower is enabled.

Under Voltage Protection (UVP)

If the PFB pin is open, V_{PFB} is pulled down lower than an UVP threshold voltage V_{UVPL} and DRV switching stops. The output voltage of the PFC stage is scaled down by a resistor divider and monitored by the OTA inverting input (PFB pin voltage). PFB sink current, I_{PFB0} for UVP, is minimized less than 450 nA to allow the use of a high impedance feedback resistor network.

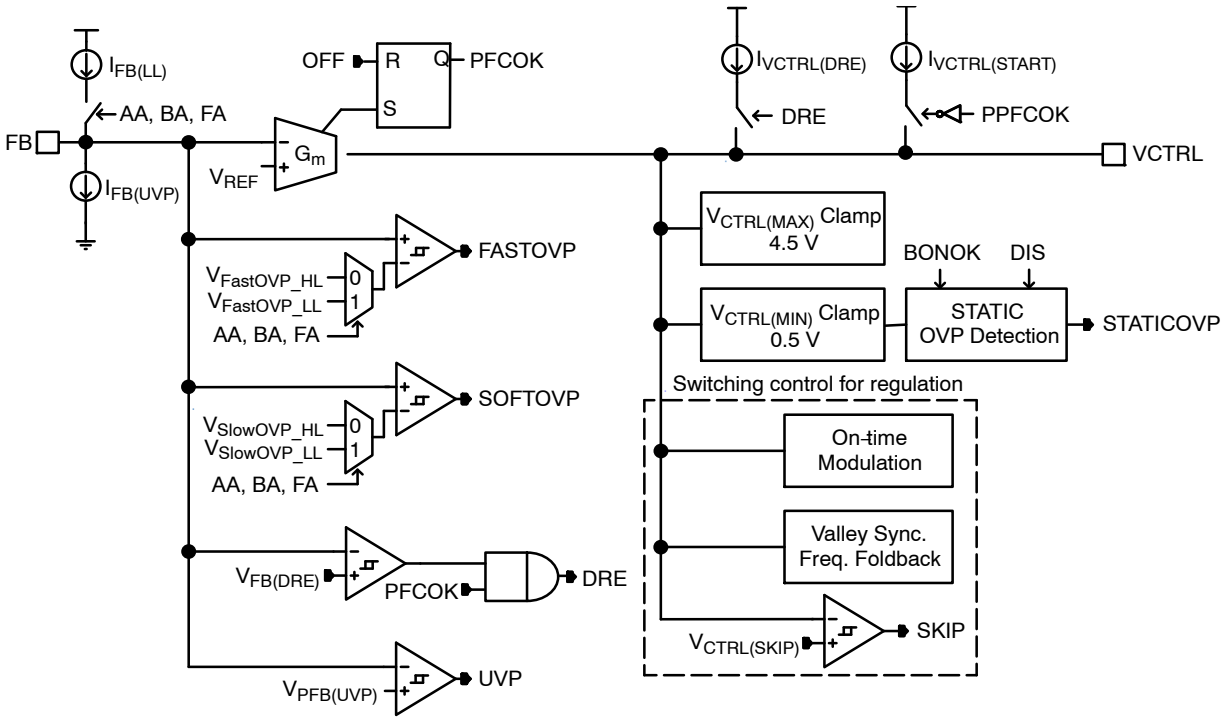


Figure 25. Feedback Regulation and Transient Control

Current Sense and Zero Cross Detection

Excessive Current Protection (OCP and OVS)

The NCP1945 is designed to monitor the current flowing through the PFC switch. Practically, a current sense resistor, R_{sense}, should be inserted between the MOSFET source and ground to generate a positive voltage proportional to the MOSFET current, V_{PCS}. The controller turns off the FET when V_{PCS} reaches the over-current threshold $V_{PCS(TH)}$ of

500 mV. There is a 400 ns blanking time measured from DRV turn on, $t_{PLEB(OCP)}$ to prevent switching noise from falsely triggering the OCP. A second threshold is set 150% higher ($V_{PCS,OVS(th)}$ of 750 mV typically) to detect overstress situations. Such a situation can occur when the current slope is steep enough to trigger this second level comparator despite the overcurrent limitation, like for instance, if the boost diode is shorted or if the inductor saturates. When an overstress situation is detected, the circuit stops generating DRV pulses for 800 µs. This long delay leads to a low duty-ratio operation in order to limit risks of application overheating.

Zero Current Detection (ZCD)

The PZCD pin receives a voltage representative of the MOSFET drain-source voltage, V_{DS}. Typically an auxiliary winding coupled from the boost inductor generates an image of the drain−source voltage, and is fed into the PZCD pin through a capacitively coupled, resistor divider network.

The PZCD pin provides the input signal for zero current and valley detection. The NCP1945 does not turn on until it detects that the inductor current has dropped to zero. In addition, when the circuit operates in discontinuous mode, it ensures that the MOSFET turns on at the valley of the drain-source voltage for minimized losses and noise. More practically, the demagnetization phase is detected when V_{PZCD} exceeds (V_{ZCD0} + $V_{ZCD(th)H}$), where $V_{ZCD(th)H}$ is 40 mV typically and detects the zero crossing or the valley when V_{ZCD} goes below (V_{ZCD0} + $V_{ZCD(th)L}$), where $V_{ZCD(th)L}$ is about −40 mV.

If the PZCD pin is unable to detect any signal that triggers the ZCD comparator during the off-time, an internal 200-µs watchdog timer initiates the next drive pulse.

Ponoff

The Ponoff pin of NCP1945 allows users to program the PFC enable/disable threshold to a given QR output power. A resistor from pin to ground pin sets the output power level at which the PFC should be activated. At a high level, the QFB voltage and demagnetization time information is used to calculate the value of output current, similar to how the output current is determined for CC overload. Combined with output voltage information, a power reference is calculated.

Internally, this function is implemented in two stages: I_{OUT} reference generation and P_{OUT} reference generation. In the first stage, the controller forms an I_{OUT} reference by summing the QR feedback voltage with the OPP voltage and converting the result into a current through a V-I converter. This current is then scaled according to the demagnetization duty cycle and applied across an internal resistor to produce the $I_{OUT(REF)}$ voltage. In the second stage, the device generates a P_{OUT} reference by modulating the $I_{OUT(REF)}$ signal with a PWM waveform proportional to the output voltage. The PWM signal is created by comparing the sensed output voltage to an internal ramp, producing a duty cycle proportional representation of V_{OUT}. The $I_{OUT(REF)}$ signal is multiplied by this PWM duty cycle and then converted into a voltage across an internal resistor. This resulting voltage is compared to a 3 V threshold to assert the Ponoff decision.

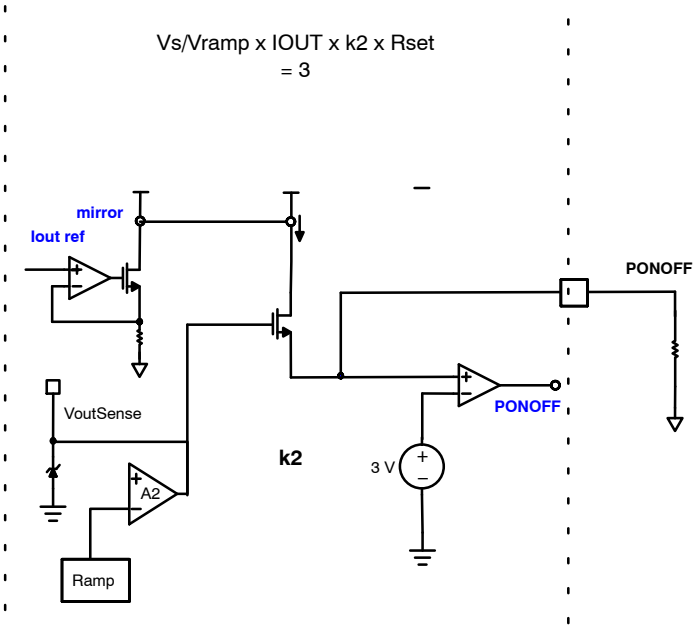


Figure 26. P_{ONOFF} Complete Schematic

This power-based method for determining the PFC entry point is valid only when the QR flyback operates in CRM. If PEM mode is enabled and the system transitions into PEM, the PEM timer determines when the PFC should be activated. If the device remains in PEM for longer than the 6 ms T_{PEM} timer, the controller turns on the PFC.

The PFC disable threshold is set such that there is approximately 15% hysteresis relative to the output power. As a result, the PFC turns off at a lower power than it enables. This hysteretic margin ensures that there is no condition in normal operation where the PFC will get into an on/off oscillatory state. Figure 26 shows a schematic of the Ponoff calculation.

THD Enhancer

NCP1945 includes an innovative function which is used to improve the Total Harmonic Distortion (THD) of the system. At DRV turn-on, inductor current is negative due to resonant current. Therefore, at AC zero cross, the input current can get distorted and lose its sinusoidal shape if the PFC drive on time is simply constant in voltage-mode. This feature is available on version LA.

The THD Enhancer of the NCP1945 increases on time of the PFC FET to compensate for the negative current. This extra time, T_{ADJ} is added at the end of the on time and its duration depends upon the input voltage.

The NCP1945 uses the HV pin to perform the line voltage sensing for brown-in/brownout (BIBO) protection, highline vs lowline detection, and line removal detection. The limitation of diode rectified line sensing is that it does not provide accurate information about line voltage near AC zero cross. Therefore, another scheme of line sensing is used for the THD enhancer, where precision voltage sensing of the line is required near the AC zero-cross. The NCP1945 generates an image of the input voltage using the PZD pin. The voltage is low pass filtered, and the generated signal is called V_{SNS}. The purpose of this signal is to provide line voltage signal information to the THD Enhancer.

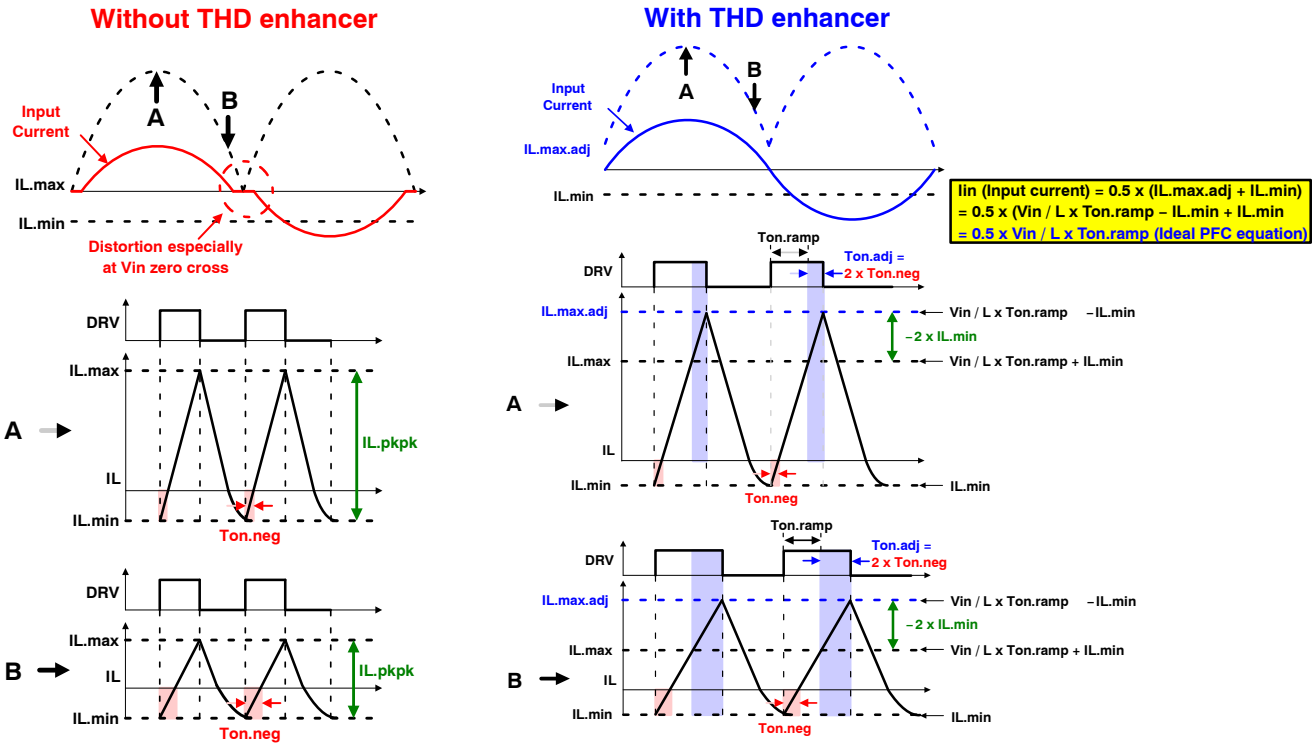


Figure 27. THD Enhancer Added on Time Across the Line

The figure above shows the added extra time to t_{on} at different regions of line cycle. At the peak of line cycle, T_{ADJ} time added to t_{on} is lowest, while it is highest near the zero crossing. The added time is inversely proportional to the line cycle.

To get precise information about the line voltage near zero cross, the THD enhancer uses the P_{ZCD} votlage to generate an image of the input voltage called V_{SNS}. The V_{SNS} signal is then converted to a current through a V-I converter. This current is used to charge a capacitor, C_{ADJ}, and the voltage on C_{ADJ}, is compared against a reference voltage, V_{ADJ}. On the PTHD pin, there is an internal current source of 10 μA, which uses the external set resistor R_{THD} to set the V_{ADJ}.

FAULT MANAGEMENT

The NCP1945 contains multiple fault detection and protection features to enable a robust application design. The fault protections with detection logic and recovery logic are summarized in the fault matrix in Table 10. Generally, the faults are divided into either latching or recoverable (i.e. non-latching) faults, where the latching faults disable the controller and do not allow the application to restart unless the latch has been cleared by a device reset. These faults usually indicate a significant issue in the application.

When the NCP1945 detects a latching fault, the driver outputs are immediately disabled and the V_{CCL} voltage discharges to the $V_{CC(off)}$ level. The HV startup circuit turns on to charge V_{CCL} up to the $V_{CC(on)}$ threshold, but the controller does not re-enable drive pulses and the device will continue to operate indefinitely in this V_{CCL} cycling mode. In order to clear the latch and restart the application, the device must go through a system reset which occurs if V_{CCL} falls below the $V_{CC(reset)}$ threshold of 6.5 V, or a line removal event has been detected. Generic device operation during a latched fault is shown in Figure 28.

There are 4 fault detections in the device that are latching faults: The OVP fault on the dedicated fault pin, the output OVP fault detected through the QZCD pin for 3 consecutive QR drive pulses, the PFC overstress fault and the QR abnormal over current fault, which are detected if the respective current sense pin exceeds a threshold for 4 consecutive drive pulses. Additionally, the OTP fault on the dedicated fault pin, and the QR overload (OVLD) can be configured as latching faults though they are by default recoverable.

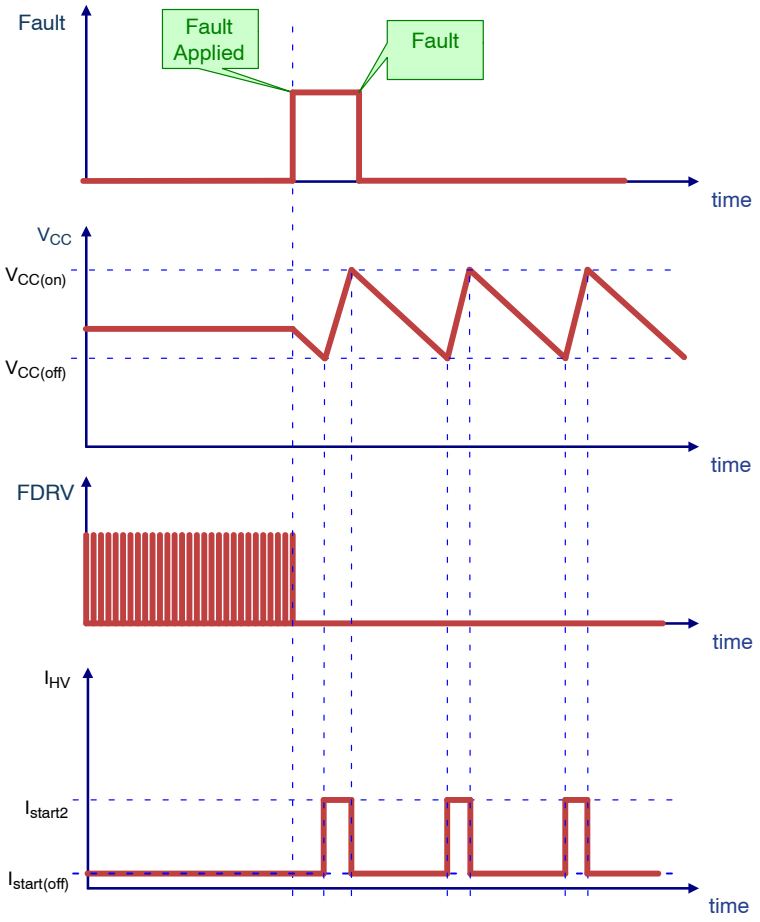


Figure 28. Operation During Latching Fault

Table 10. FAULT HANDLING MATRIX

Fault	Set	Reset	Controller Action
BO Fault	$(V_{HV} < V_{BO(STOP)}) + t_{BO(STOP)}$ expires	$V_{HV} > V_{BO(START)} + t_{delay(BO\_start)}$	• Device begins soft stop function • Soft stop complete on StaticOVP • QDRV & PDRV disabled when soft stop complete • Device restarts next $V_{CC(ON)}$ after fault is reset
V_{CC} UVLO	$V_{CCL} < V_{CC(OFF)}$	$V_{CCL} > V_{CC(ON)}$	• QDRV & PDRV disabled immediately • HV Startups Enabled • Device restarts next $V_{CC(ON)}$
Fault OTP	t_{SSTART} complete + $V_{Fault} < (V_{Fault(OTP\_in)} + t_{delay(OTP)})$	$t_{RESTART}$ expires + $V_{Fault} > V_{fault(OTP\_out)}$	• QDRV & PDRV disabled immediately • Auto-recovery timer runs • Device restarts next $V_{CC(ON)}$ after fault is reset
Fault OVP	$V_{Fault} > (V_{Fault(OVP)} + t_{delay(OVP)})$	Master System Reset	• QDRV & PDRV disabled immediately • Latching fault, system reset needed to restart
TSD	$T_J > T_{SHDN} + t_{delay(SHDN)}$	$T_J < (T_{SHDN} - T_{SHDN(HYS)})$	• QDRV & PDRV disabled immediately • Device restarts when fault clears
V_{out} OVP / $n_{out(OVP)}$	$V_{QZCD} > V_{OUT(OVP)}$ for 3 consecutive QDRVs	Master System Reset	• $n_{OUT(OVP)}$ counter increments on OVP event • QDRV & PDRV disabled after 3 events • Latching fault, system reset needed to restart
PFC UVP	$V_{PFB} < V_{UVPL} + t_{UVP}$	$V_{PFB} > V_{UVPH} + t_{UVP}$	• QDRV & PDRV disabled immediately • Device restarts next $V_{CC(ON)}$ after fault is reset
PFC Soft OVP	$V_{PFB} > V_{softOVP\_xL}$	$V_{PFB} < V_{SoftOVP\_xL} - V_{Soft-OVP\_HYS}$	• Start PDRV pulse width reduction sequence • PDRV disables after soft OVP sequence • PDRV restarts when hysteresis cleared
PFC Fast OVP	$V_{PFB} > V_{fastOVP\_xL}$	$V_{PFB} < V_{fastOVP\_xL} - V_{fastOVP\_HYS}$	• PDRV disabled immediately • PDRV restarts when hysteresis cleared
PFC Over-Current (OCP)	$V_{PCS} > V_{PCS(TH)}$	Cycle-by-Cycle, No Reset Required	• PDRV pulse terminates immediately • New PDRV pulse on next PZCD – Normal Operation
PFC Over-Stress (OVS)	$V_{PCS} > V_{PCS,OVS(th)}$	Cycle-by-Cycle, No Reset Required	• PDRV pulse terminates immediately • Controller forces $t_{WDG(OS)}$ • New PDRV pulse after $t_{WDG(OS)}$
n_{OVS}	$V_{PCS} > V_{PCS,OVS(th)}$ for 15 consecutive PDRVs	Master System Reset	• QDRV & PDRV disabled immediately • Latching fault, system reset needed to restart
QR Over-Current (OCP)	$V_{QCS} > V_{QILIM1}$	Cycle-by-Cycle, No Reset Required	• QDRV pulse terminates immediately • Start overload timer (t_{OVLD}) • New QDRV pulse on next QZCD – Normal Operation
QR Constant Current Limit (CCILIM)	$V_{QFB} > V_{FB(OVLD)}$	Cycle-by-Cycle, No Reset Required	• Start overload timer (t_{OVLD}) • New QDRV pulse on next QZCD – Normal Operation
QR Over-load (OVLD)	t_{OVLD} Expires	$t_{RESTART}$ expires	• QDRV & PDRV disabled immediately • Device restarts next $V_{CC(ON)}$ after fault is reset
QR Abnormal Overcurrent (AOCP)	$V_{QCS} > V_{QILIM2}$	Cycle-by-Cycle, No Reset Required	• QDRV pulse terminates immediately • New QDRV pulse on next QZCD – Normal Operation
N_{QILIM2}	$V_{QCS} > V_{QILIM2}$ 4 consecutive PDRVs	Master System Reset	• QDRV & PDRV disabled immediately • Latching fault, system reset needed to restart

Recoverable or non-latching faults can be cycle-by-cycle protections that may occur occasionally during normal operation and should not cause a significant disruption to the application. In some cases, cycle-by-cycle protections may eventually cause the device to shut down if they persist, and recovery from the shutdown is then a combination of timer or event based. Timer-based autorecovery such as the QR overload fault requires that the 2 second restart period ($t_{RESTART}$) expire, and then the device waits for the next $V_{CC(ON)}$ event to enable drive pulses. This is illustrated in Figure 29.

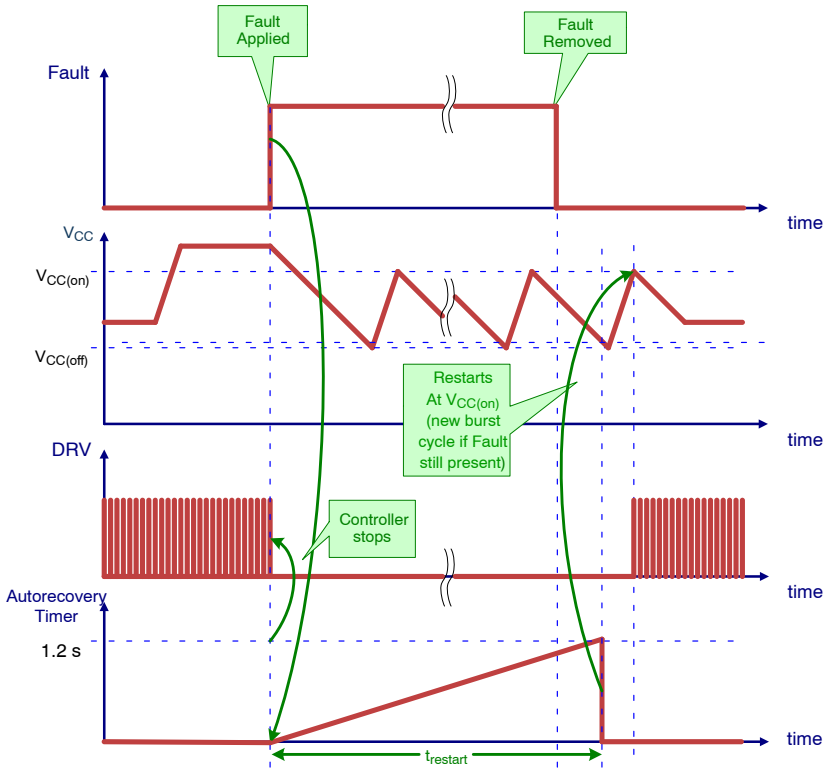


Figure 29. Timer-Based Auto-Recovery Operation

DEDICATED FAULT PIN

The NCP1945 includes a dedicated fault circuit accessible via the Fault pin. The controller can be latched off by pulling the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.2 V. The controller is also disabled if the Fault pin voltage is pulled below the lower fault threshold, $V_{Fault(OTP\_in)}$, typically 0.4 V. The lower threshold is typically used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 30 shows the architecture of the Fault input.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Both the upper and lower fault detector blanking delays, $t_{delay(OVP)}$ and $t_{delay(OTP)}$,are typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.

As shown in Figure 28, the fault pin input includes an internal clamp that prevents the pin from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull-up current has to be higher than the pull-down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$), i.e., approximately 1 mA. The upper fault threshold is intended to be used for an overvoltage fault using a zener diode and a resistor in series from the auxiliary winding voltage. Typically, this would be configured for detecting an over-voltage on the V_{CCL} supply pin. The controller is latched once V_{Fault} exceeds $V_{Fault(OVP)}$.

Once the controller is latched, it follows the behavior of a latching fault and is only reset if V_{CC} is reduced to $V_{CC(reset)}$, or X2 discharge is activated. In the typical application these conditions occur only if the ac voltage is removed from the system.

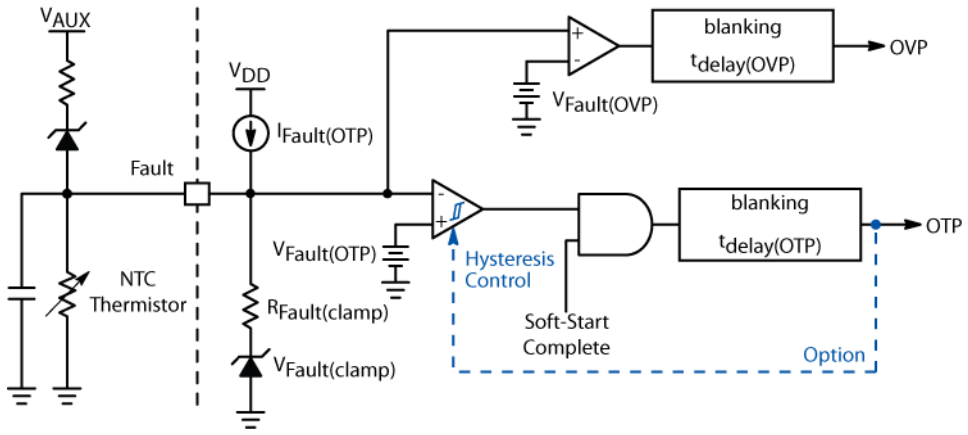


Figure 30. Fault Pin Internal Schematic

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source, I_{OTP} (typically 45 μA), generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP\_in)}$.

The OTP fault is disabled during device startup including the soft-start period. I_{OTP} is disabled prior to V_{CCL} reaching $V_{CC(ON)}$, this is done to reduce the controller I_{CC} consumption while the HV startup regulators are attempting to charge up the V_{CCL} capacitor. The current source is enabled once V_{CCL} reaches $V_{CC(on)}$, but immediately enabling the OTP fault detection would result in the controller immediately declaring a fault while the OTP current was charging the external filter capacitor that is typically connected between the Fault and GND pins. Therefore, the lower fault comparator (i.e. over-temperature detection) is ignored during soft-start.

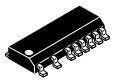
The QR overload fault is a timer-based auto recovery fault requiring the device to complete a 2 second restart period ($t_{RESTART}$) before the application is re-enabled the next time that V_{CCL} is charged above the $V_{CC(on)}$ threshold. The QR overload fault is triggered by the overload timer which is set into operation by either the cycle-by-cycle current peak limit or the constant current limit. The overload timer, t_{OVLD}, is typically 160 ms, and is also an integrating timer, meaning that the timer will increment when the fault is detected and decrement if the fault is not detected.

REVISION HISTORY

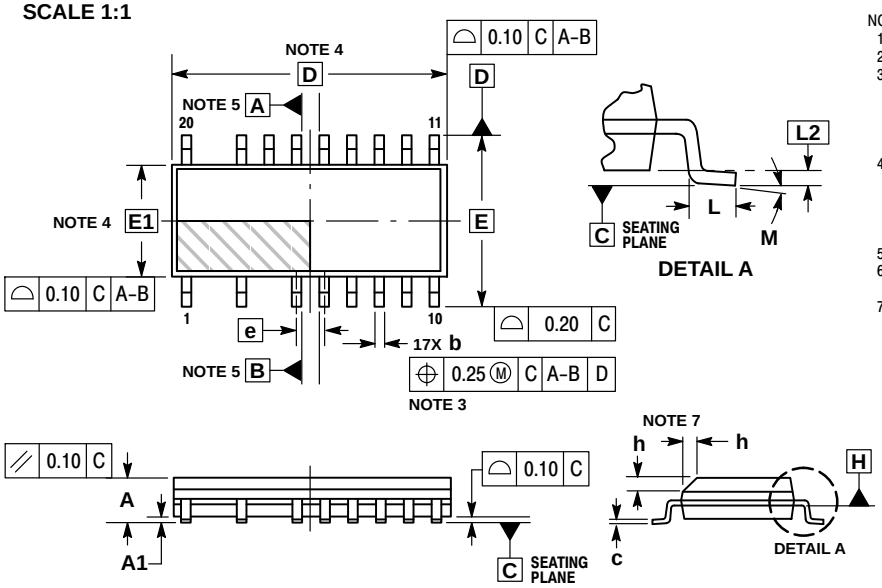
Revision	Description of Changes	Date
0	Initial document release.	4/2/2026

SOIC20 NB LESS PINS 2, 4 & 19
CASE 751BS
ISSUE O

DATE 28 APR 2011



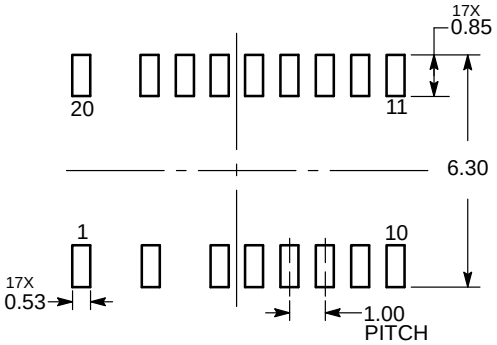
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 TOTAL IN EXCESS OF THE b DIMENSION. DIMENSION b APPLIES TO THE FLAT PORTION OF THE LEAD AND SHALL BE MEASURED BETWEEN 0.13 AND 0.25 FROM THE TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS BUT DO INCLUDE MOLD MISMATCH. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. CHAMFER FEATURE IS OPTIONAL. IF NOT PRESENT, THEN A PIN ONE IDENTIFIER MUST BE LOCATED IN THIS AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.20
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.00 BSC	
h	0.25	0.50
L	0.40	0.85
L2	0.25 BSC	
M	0°	8°

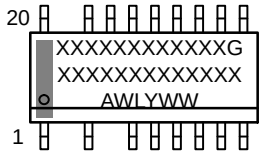
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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