NCP3985

Micropower, 150 mA Low-Noise, High PSRR, Ultra-Low Dropout BiCMOS Voltage Regulator

The NCP3985 is 150 mA LDO that provides the engineer with a very stable, accurate voltage with low noise and high Power Supply Rejection Ratio (PSRR) suitable for sensitive applications. In order to optimize performance for battery operated portable applications, the NCP3985 employs an advanced BiCMOS process to combine the benefits of low noise and superior dynamic performance of bipolar elements with very low ground current consumption at full loads offered by CMOS.

The NCP3985 is stable with small, low value capacitors and is available in TSOP−5 package.

Features

- Output Voltage Options:
  - 1.8 V, 2.5 V, 2.75 V, 2.8 V, 3.0 V, 3.3 V
  - Contact Factory for Other Voltage Options
- Output Current Limit 200 mA
- Low Noise (typ 20 μV_{rms})
- High PSRR (typ 70 dB)
- Stable with Ceramic Output Capacitors as low as 1 μF
- Low Sleep Mode Current (max 1 μA)
- Active Discharge Circuit
- Current Limit Protection
- Thermal Shutdown Protection
- Direct Replacement for LP3985
- These are Pb−Free Devices

Typical Applications

- Cellular Telephones
- Noise Sensitive Applications (Video, Audio)
- Analog Power Supplies
- PDAs / Palmtops / Organizers / GPS
- Battery Supplied Devices

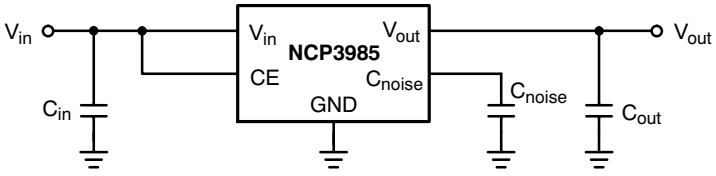


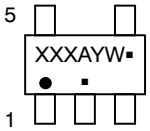
Figure 1. Typical Application Schematic

ON Semiconductor®

http://onsemi.com

TSOP−5
SN SUFFIX
CASE 483

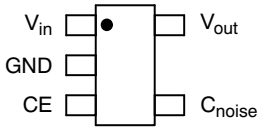
MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

© Semiconductor Components Industries, LLC, 2008

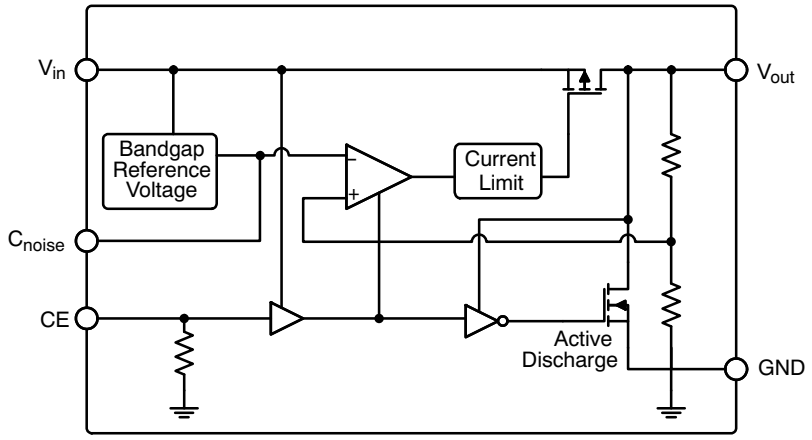


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{in}	Power Supply Input Voltage
2	GND	Power Supply Ground
3	CE	Chip Enable: This pin allows on/off control of the regulator. To disable the device, connect to GND. If this function is not in use, connect to V_{in}. Internal 5 MΩ Pull Down resistor is connected between CE and GND.
4	C_{noise}	Noise reduction pin. (Connect 100 nF or 10 nF capacitor to GND)
5	V_{out}	Regulated Output Voltage

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{in}	−0.3 V to 6 V	V
Chip Enable Voltage	V_{CE}	−0.3 V to V_{in} +0.3 V	V
Noise Reduction Voltage	V_{Cnoise}	−0.3 V to V_{in} +0.3 V	V
Output Voltage	V_{out}	−0.3 V to V_{in} +0.3 V	V
Maximum Junction Temperature (Note 1)	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL−STD−883, Method 3015
Machine Model Method 200 V

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Package Thermal Resistance: (Note 1) Junction−to−Lead (pin 5) Junction−to−Ambient	$R_{\theta JA}$	 109 220	°C/W

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area

ELECTRICAL CHARACTERISTICS

(V_{in} = V_{out} + 0.5 V, V_{CE} = 1.2 V, C_{in} = 0.1 μF, C_{out} = 1 μF, C_{noise} = 10 nF, T_A = −40°C to 85°C, unless otherwise specified (Note 2))

Characteristic		Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT							
Input Voltage			V_{in}	2.5	–	5.5	V
Output Voltage (Note 3)	1.8 V	V_{in} = (V_{out} + 0.5 V) to 5.5 V	V_{out}	1.764	–	1.836	V
	2.5 V	I_{out} = 1 mA		2.450	–	2.550	
	2.75 V			2.695	–	2.805	
	2.8 V			2.744	–	2.856	
	3.0 V			2.940	–	3.060	
	3.3 V			3.234 (−2%)	–	3.366 (+2%)	
Output Voltage (Note 3)	1.8 V	V_{in} = (V_{out} + 0.5 V) to 5.5 V	V_{out}	1.746	–	1.854	V
	2.5 V	I_{out} = 1 mA to 150 mA		2.425	–	2.575	
	2.75 V			2.6675	–	2.8325	
	2.8 V			2.716	–	2.884	
	3.0 V			2.910	–	3.090	
	3.3 V			3.201 (−3%)	–	3.399 (+3%)	
Power Supply Ripple Rejection		V_{in} = V_{out} + 0.5 V + 0.5 V_{p-p}	PSRR				dB
		I_{out} = 1 mA to 150 mA f = 120 Hz		–	70	–	
		C_{noise} = 100nF f = 1 kHz		–	70	–	
		f = 10 kHz		–	55	–	
Line Regulation		V_{in} = (V_{out} + 0.5 V) to 5.5 V, I_{out} = 1 mA	Reg_{line}	−0.2	–	0.2	%/V
Load Regulation		I_{out} = 1 mA to 150 mA	Reg_{load}	–	12	25	mV
Output Noise Voltage		f = 10 Hz to 100 kHz	V_n				μV_{rms}
		I_{out} = 1 mA to 150 mA C_{noise} = 100 nF		–	20	–	
		C_{noise} = 10 nF		–	25	–	
Output Current Limit		V_{out} = $V_{out(nom)}$ − 0.1 V	I_{LIM}	200	310	470	mA
Output Short Circuit Current		V_{out} = 0 V	I_{SC}	210	320	490	mA
Dropout Voltage (Note 4)	2.5 V	I_{out} = 150 mA	V_{DO}	–	105	155	mV
	2.75 V			–	105	155	
	2.8 V			–	105	155	
	3.0 V			–	100	150	
	3.3 V			–	100	150	
GENERAL							
Ground Current		I_{out} = 1 mA	I_{GND}	–	70	90	μA
		I_{out} = 150 mA		–	110	220	
Disable Current		V_{CE} = 0 V	I_{DIS}	–	0.1	1	μA
Thermal Shutdown Threshold (Note 5)			T_{SD}	–	150	–	°C
Thermal Shutdown Hysteresis (Note 5)			T_{SH}	–	20	–	°C
CHIP ENABLE							
Input Threshold	Low		$V_{th(CE)}$	–	–	0.4	V
	High			1.2	–	–	
Internal Pull−Down Resistance (Note 6)			$R_{PD(CE)}$	2.5	5	10	MΩ
TIMING							
Turn−on Time		I_{out} = 150 mA C_{noise} = 10 nF	t_{on}	–	0.4	–	ms
		C_{noise} = 100 nF		–	4	–	
Turn−off Time		C_{noise} = 10 nF/100 nF I_{out} = 1 mA	t_{off}	–	800	–	μs
		I_{out} = 10 mA		–	200	–	

2. Performance guaranteed over the indicated operating temperature range by design and/or characterization, production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
3. Contact factory for other voltage options.
4. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = V_{out} + 0.5 V if V_{out} < 2.5 V, then V_{DO} = V_{in} − V_{out} at V_{in} = 2.5 V.
5. Guaranteed by design and characterization.
6. Expected to disable device when CE pin is floating.

TYPICAL CHARACTERISTICS

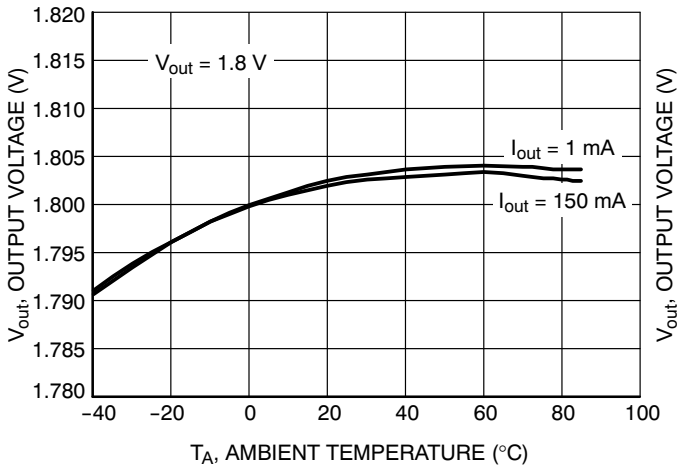


Figure 3. Output Voltage vs. Temperature (V_{out} = 1.8 V)

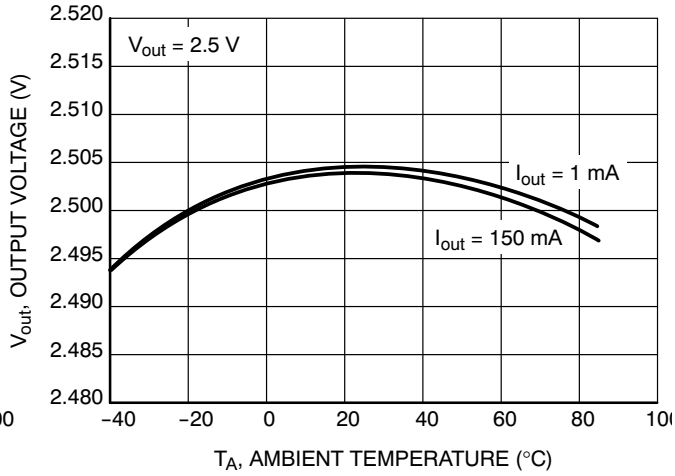


Figure 4. Output Voltage vs. Temperature (V_{out} = 2.5 V)

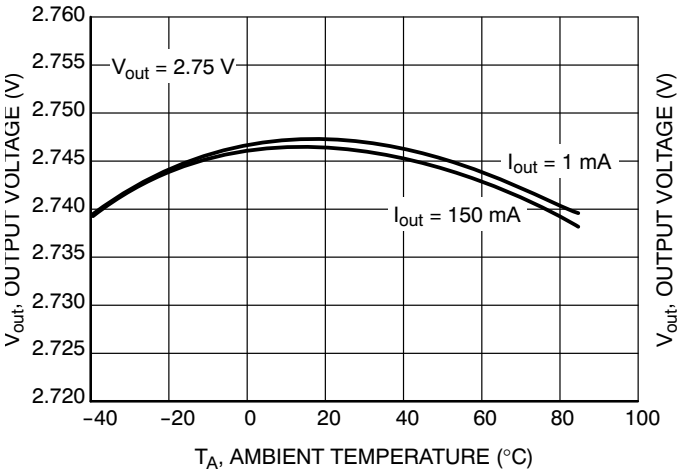


Figure 5. Output Voltage vs. Temperature (V_{out} = 2.75 V)

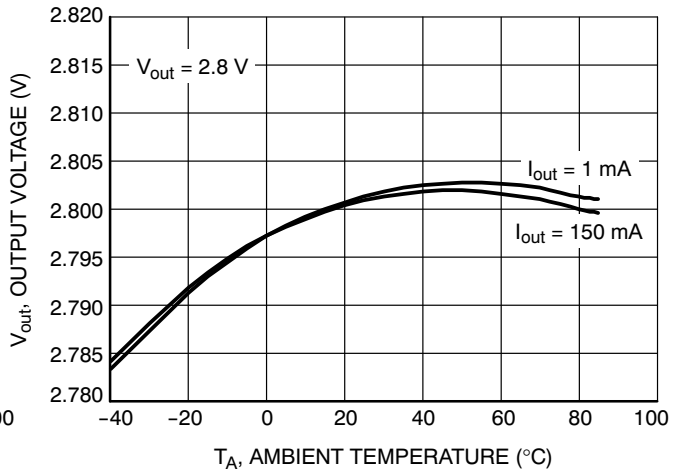


Figure 6. Output Voltage vs. Temperature (V_{out} = 2.8 V)

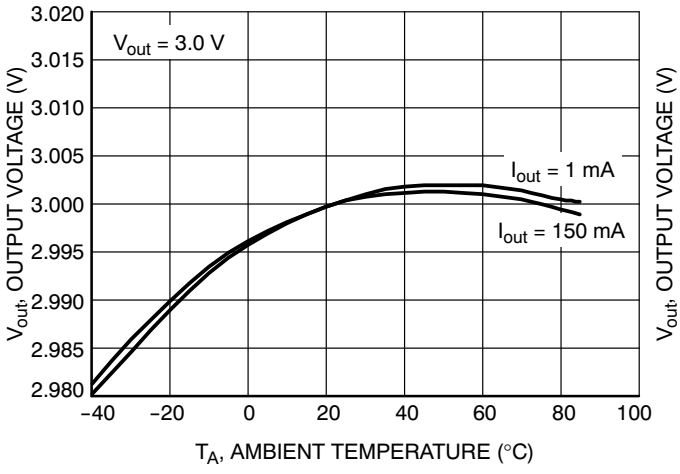


Figure 7. Output Voltage vs. Temperature (V_{out} = 3.0 V)

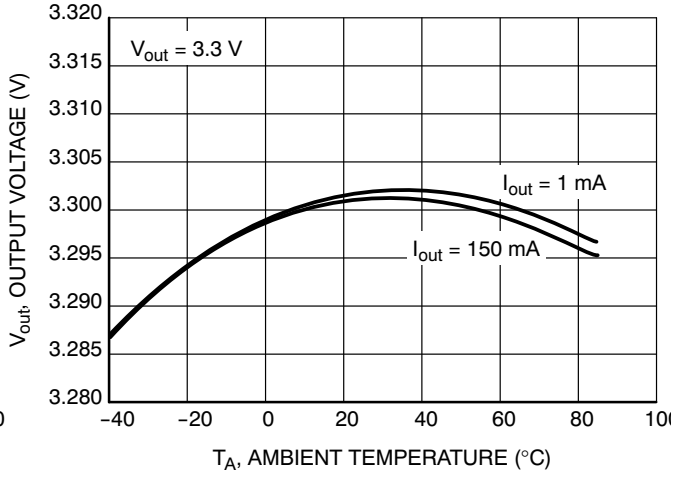


Figure 8. Output Voltage vs. Temperature (V_{out} = 3.3 V)

TYPICAL CHARACTERISTICS

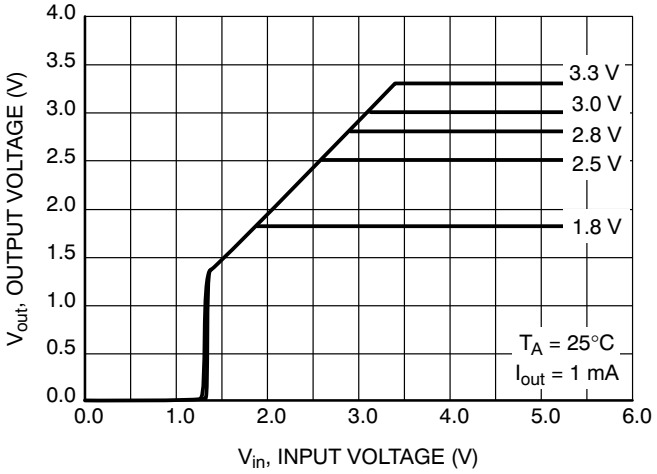


Figure 9. Output Voltage vs. Input Voltage

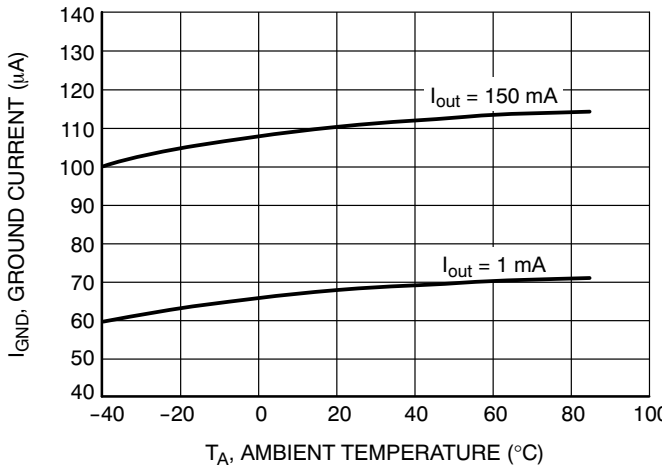


Figure 10. Ground Current vs. Temperature

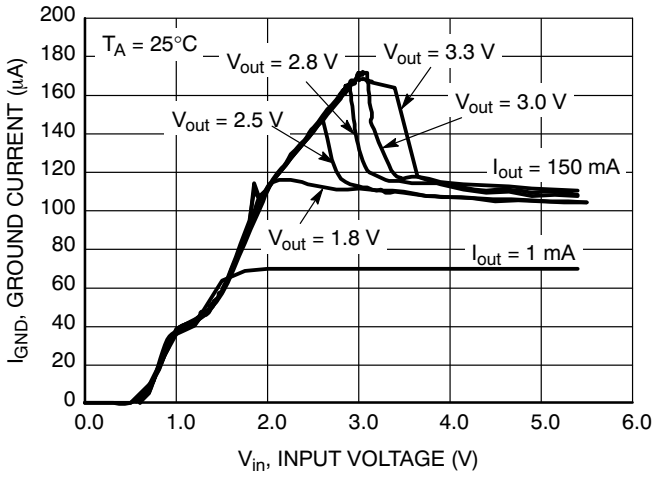


Figure 11. Ground Current vs. Input Voltage

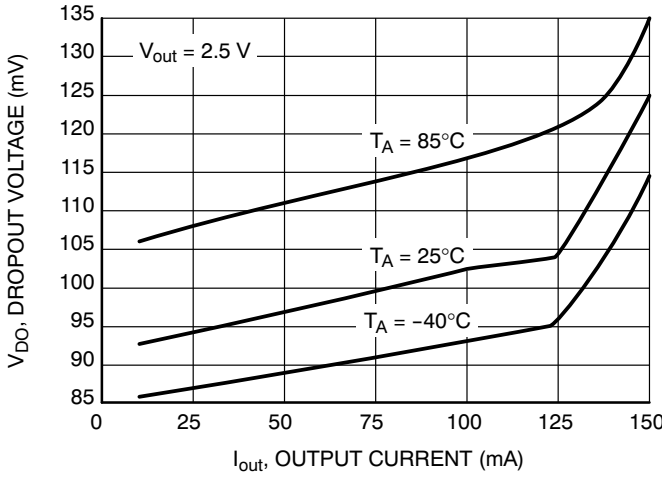


Figure 12. Dropout Voltage vs. Output Current

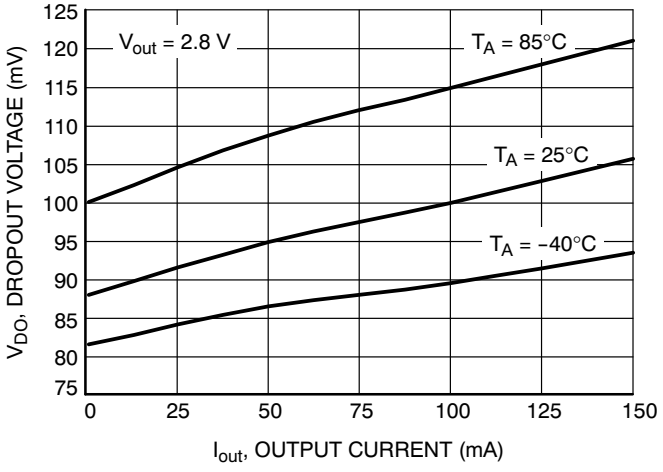


Figure 13. Dropout Voltage vs. Output Current

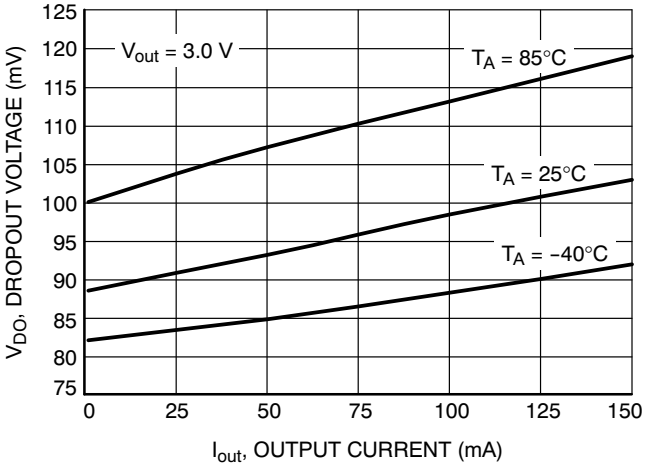


Figure 14. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

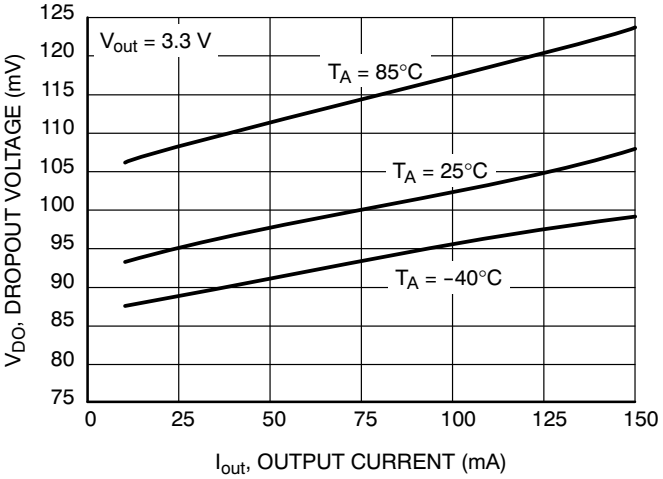


Figure 15. Dropout Voltage vs. Output Current

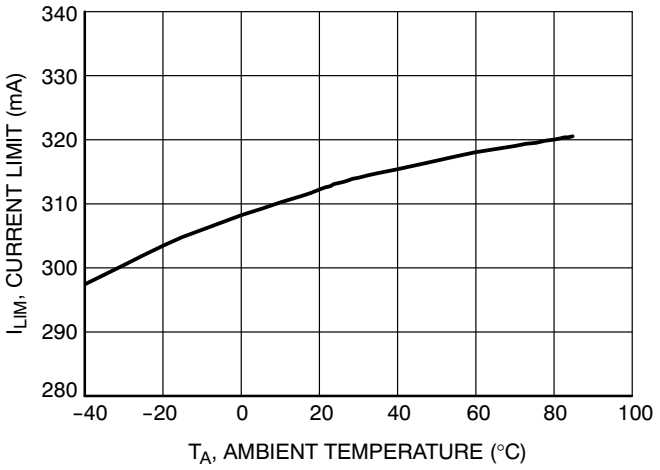


Figure 16. Current Limit vs. Temperature

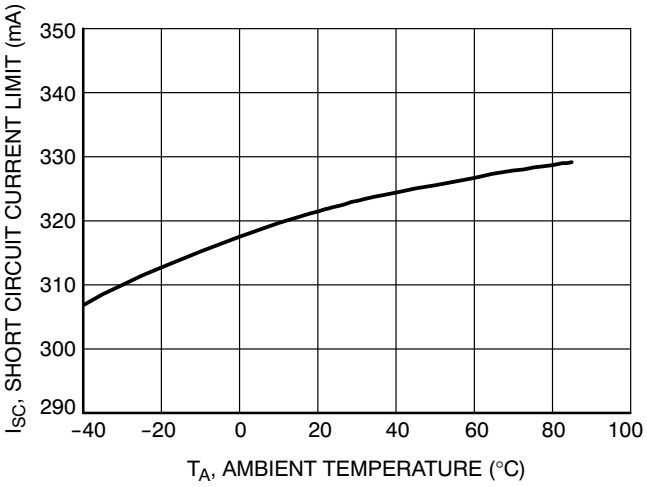


Figure 17. Short Circuit Current vs. Temperature

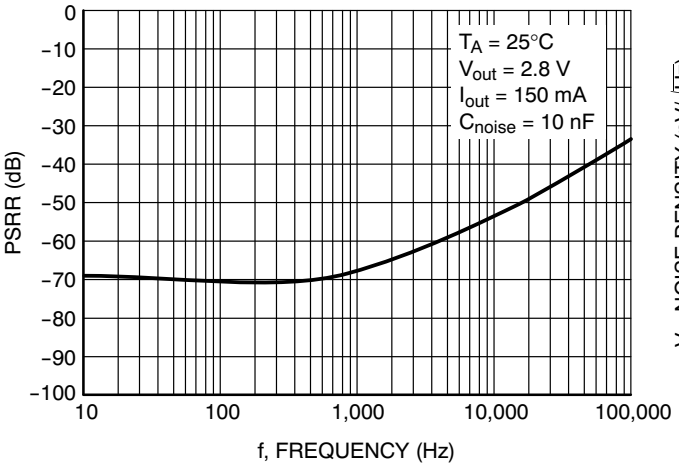


Figure 18. PSRR vs. Frequency

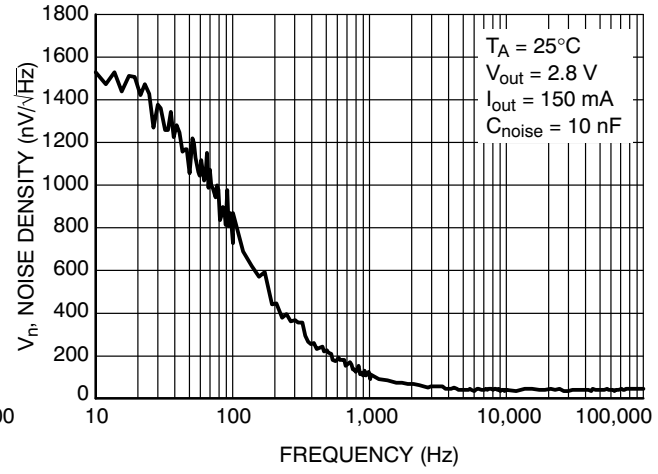


Figure 19. Noise Density vs. Frequency

TYPICAL CHARACTERISTICS

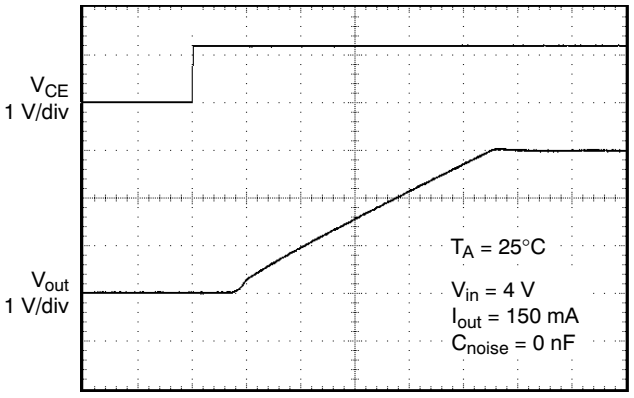


Figure 20. Enable Voltage and Output Voltage vs. Time (Start−Up)

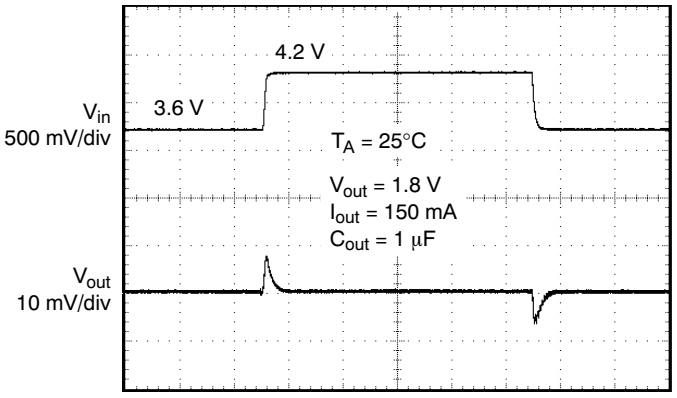


Figure 21. Line Transient

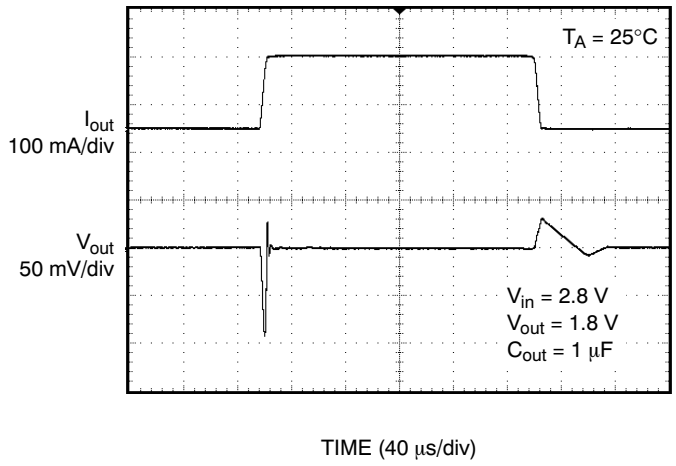


Figure 22. Load Transient

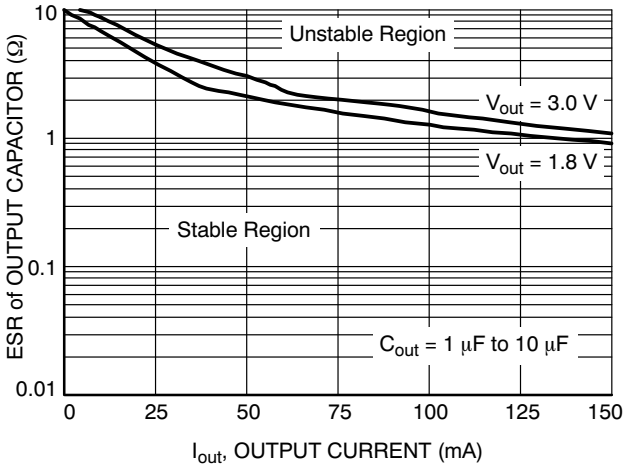


Figure 23. Output Capacitor ESR vs. Output Current

NOTE: Typical characteristics were measured with the same conditions as electrical characteristics, unless otherwise noted.

APPLICATION INFORMATION

General

The NCP3985 is a 200 mA (current limited) linear regulator with a logic input for on/off control for the high speed turn−off output voltage.

Access to the major contributor of noise within the integrated circuit is provided as the focus for noise reduction within the linear regulator system.

Power Up/Down

During power up, the NCP3985 maintains a high impedance output (V_{out}) until sufficient voltage is present on V_{in} to power the internal bandgap reference voltage. When sufficient voltage is supplied (approx 1.2 V), V_{out} will start to turn on (assume CE shorted to V_{in}), linearly increasing until the output regulation voltage has been reached.

Active discharge circuitry has been implemented to insure a fast turn off time. Then CE goes low, the active discharge transistor turns on creating a fast discharge of the output voltage. Power to drive this circuitry is drawn from the output node. This is to maintain the lowest quiescent current when in the sleep mode (V_{CE} = 0.4 V). This circuitry subsequently turns off when the output voltage discharges.

CE (chip enable)

The enable function is controller by the logic pin CE. The voltage threshold of this pin is set between 0.4 V and 1.2 V. A voltage lower than 0.4 V guarantees the device is off. A voltage higher than 1.2 V guarantees the device is on. The NCP3985 enters a sleep mode when in the off state drawing less than 1 μA of quiescent current.

The device can be used as a simple regulator without use of the chip enable feature by tying the CE pin to the V_{in} pin.

Current Limit

Output Current is internally limited within the IC to a minimum of 200 mA. The design is set to a higher value to allow for variation in processing and the temperature coefficient of the parameter. The NCP3985 will source this amount of current measured with a voltage 100 mV lower than the typical operating output voltage.

The specification for short circuit current limit (@ V_{out} = 0 V) is specified at 320 mA (typ). There is no additional circuitry to lower the current limit at low output voltages. This number is provided for informational purposes only.

Output Capacitor

The NCP3985 has been designed to work with low ESR ceramic capacitors. There is no ESR lower limit for stability for the recommended 1 μF output capacitor. Stable region for Output capacitor ESR vs Output Current is shown in Figure 23.

Typical characteristics were measured with Murata ceramic capacitors. GRM219R71E105K (1 μF, 25 V, X7R, 0805) and GRM21BR71A106K (10 μF, 10 V, X7R, 0805).

Output Noise

The main contributor for noise present on the output pin V_{out} is the reference voltage node. This is because any noise which is generated at this node will be subsequently amplified through the error amplifier and the PMOS pass device. Access to the reference voltage node is supplied directly through the C_{noise} pin. Noise can be reduced from a typical value of 25 μV_{rms} by using 10 nF to 20 μV_{rms} by using a 100 nF from the C_{noise} pin to ground.

A bypass capacitor is recommended for good noise performance and better load transient response.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold, a Thermal Shutdown (TSD) event is detected and the output (V_{out}) is turned off. There is no effect from the active discharge circuitry. The IC will remain in this state until the die temperature moves below the shutdown threshold (150°C typical) minus the hysteresis factor (20°C typical).

This feature provides protection from a catastrophic device failure due to accidental overheating. It is not intended to be used as a substitute for proper heat sinking. The maximum device power dissipation can be calculated by:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

Thermal resistance value versus copper area and package is shown in Figure 24.

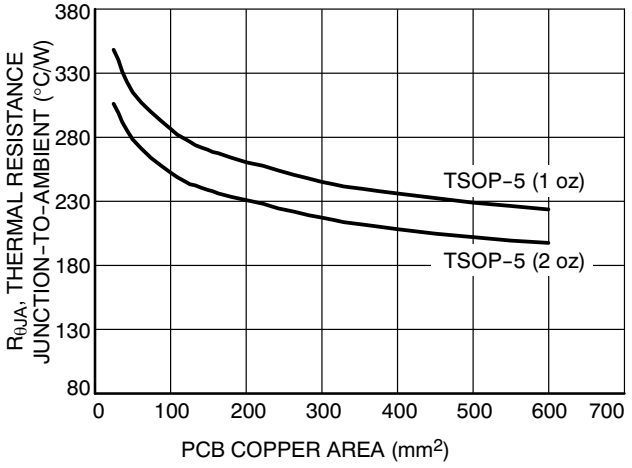


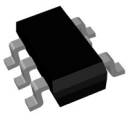
Figure 24. $R_{\theta JA}$ vs. PCB Copper Area

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP3985SN18T1G	1.8 V	LKA	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP3985SN25T1G	2.5 V	LKD		
NCP3985SN275T1G	2.75 V	LKE		
NCP3985SN28T1G	2.8 V	LKB		
NCP3985SN30T1G	3.0 V	LKC		
NCP3985SN33T1G	3.3 V	LKF		

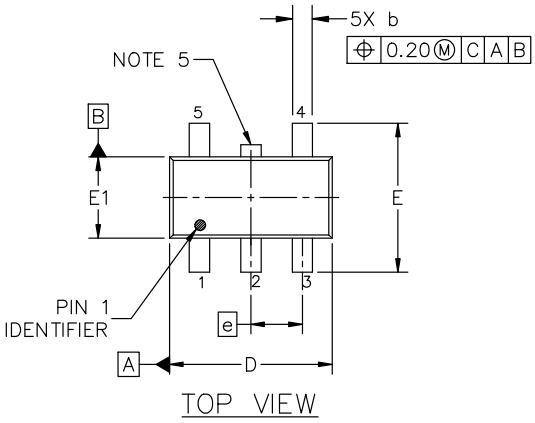
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The products described herein (NCP3985), may be covered by one or more U.S. patents.

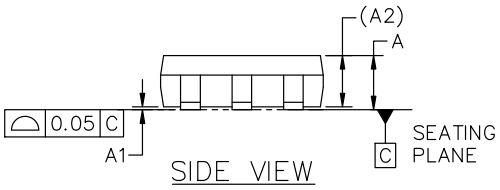


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

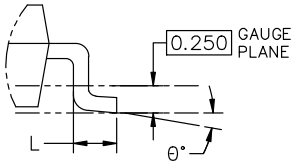
DATE 01 APR 2024



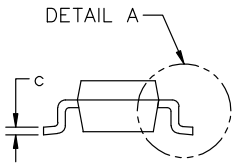
TOP VIEW



SIDE VIEW



DETAIL "A"
SCALE 2:1



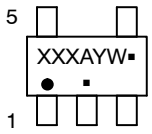
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

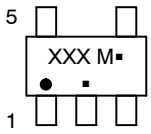
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

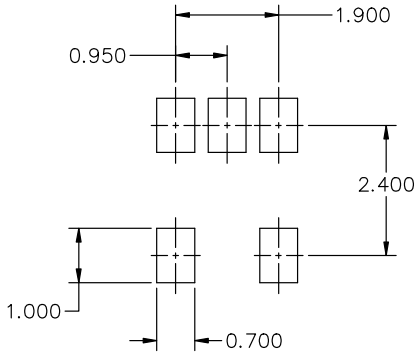


Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales