# ecoSWITCH™
# Advanced Load Management
## Controlled Load Switch with Low $R_{ON}$

# NCP45541

The NCP45541 load switch provides a component and area-reducing solution for efficient power domain switching with inrush current limit via soft−start. In addition to integrated control functionality with ultra low on−resistance, this device offers system monitoring via power good signaling. This cost effective solution is ideal for power management and hot-swap applications requiring low power consumption in a small footprint.

### Features

- Advanced Controller with Charge Pump
- Integrated N-Channel MOSFET with Low $R_{ON}$
- Input Voltage Range 0.5 V to 13.5 V
- Soft-Start via Controlled Slew Rate
- Adjustable Slew Rate Control
- Power Good Signal
- Extremely Low Standby Current
- Load Bleed (Quick Discharge)
- This is a Pb−Free Device

### Typical Applications

- Portable Electronics and Systems
- Notebook and Tablet Computers
- Telecom, Networking, Medical, and Industrial Equipment
- Set−Top Boxes, Servers, and Gateways
- Hot−Swap Devices and Peripheral Ports

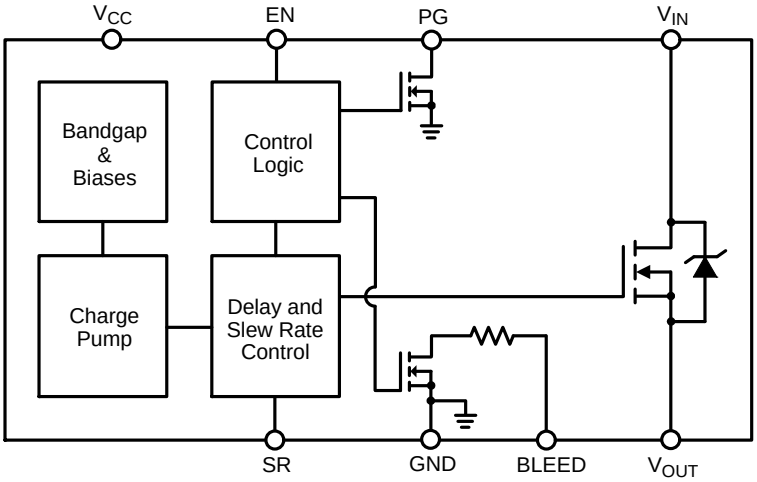


**Figure 1. Block Diagram**

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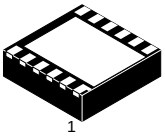
| $R_{ON}$ TYP | $V_{CC}$ | $V_{IN}$ | $I_{MAX_DC}$* |
|---|---|---|---|
| 7.7 mΩ | 3.3 V | 1.8 V | 14 A |
| 8.0 mΩ | 3.3 V | 5.0 V | |
| 9.2 mΩ | 3.3 V | 12 V | |

*$I_{MAX_DC}$ is defined as the maximum steady state current the load switch can pass at room ambient temperature without entering thermal lockout.

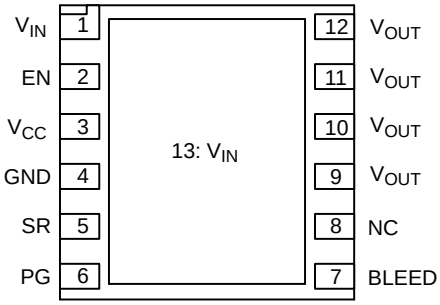



**DFN12, 3x3**
**CASE 506CD**

### MARKING DIAGRAM

x = H for NCP45541−H
= L for NCP45541−L
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### PIN CONFIGURATION




(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

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**Table 1. PIN DESCRIPTION**

| Pin | Name | Function |
|---|---|---|
| 1, 13 | $V_{IN}$ | Drain of MOSFET (0.5 V – 13.5 V), Pin 1 must be connected to Pin 13 |
| 2 | EN | NCP45541−H − Active−high digital input used to turn on the MOSFET, pin has an internal pull down resistor to GND |
| | | NCP45541−L − Active−low digital input used to turn on the MOSFET, pin has an internal pull up resistor to $V_{CC}$ |
| 3 | $V_{CC}$ | Supply voltage to controller (3.0 V − 5.5 V) |
| 4 | GND | Controller ground |
| 5 | SR | Slew rate adjustment; float if not used |
| 6 | PG | Active−high, open−drain output that indicates when the gate of the MOSFET is fully driven, external pull up resistor ≥ 1 kΩ to an external voltage source required; tie to GND if not used. |
| 7 | BLEED | Load bleed connection, must be tied to $V_{OUT}$ either directly or through a resistor ≤ 100 MΩ |
| 8 | NC | No connect, internally floating but pin may be tied to $V_{OUT}$ |
| 9−12 | $V_{OUT}$ | Source of MOSFET connected to load |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | −0.3 to 6 | V |
| Input Voltage Range | $V_{IN}$ | −0.3 to 18 | V |
| Output Voltage Range | $V_{OUT}$ | −0.3 to 18 | V |
| EN Digital Input Range | $V_{EN}$ | −0.3 to ($V_{CC}$ + 0.3) | V |
| PG Output Voltage Range (Note 1) | $V_{PG}$ | −0.3 to 6 | V |
| Thermal Resistance, Junction−to−Ambient, Steady State (Note 2) | $R_{\theta JA}$ | 30.9 | °C/W |
| Thermal Resistance, Junction−to−Ambient, Steady State (Note 3) | $R_{\theta JA}$ | 51.3 | °C/W |
| Thermal Resistance, Junction−to−Case ($V_{IN}$ Paddle) | $R_{\theta JC}$ | 3.5 | °C/W |
| Continuous MOSFET Current @ $T_A$ = 25°C (Note 2) | $I_{MAX}$ | 14 | A |
| Continuous MOSFET Current @ $T_A$ = 25°C (Note 3) | $I_{MAX}$ | 15.5 | A |
| Transient MOSFET Current (for up to 500 μs) | $I_{MAX_TRANS}$ | 24 | A |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2)<br>Derate above $T_A$ = 25°C | $P_D$ | 3.24<br>32.4 | W<br>mW/°C |
| Total Power Dissipation @ $T_A$ = 25°C (Note 3)<br>Derate above $T_A$ = 25°C | $P_D$ | 1.95<br>19.5 | W<br>mW/°C |
| Storage Temperature Range | $T_{STG}$ | −40 to 150 | °C |
| Lead Temperature, Soldering (10 sec.) | $T_{SLD}$ | 260 | °C |
| ESD Capability, Human Body Model (Notes 4 and 5) | $ESD_{HBM}$ | 3.0 | kV |
| ESD Capability, Charged Device Model (Note 4) | $ESD_{CDM}$ | 1.0 | kV |
| Latch−up Current Immunity (Notes 4 and 5) | LU | 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. PG is an open−drain output that requires an external pull up resistor ≥ 1 kΩ to an external voltage source.
2. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
3. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
4. Tested by the following methods @ $T_A$ = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78
5. Rating is for all pins except for $V_{IN}$ and $V_{OUT}$ which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for $V_{IN}$ and $V_{OUT}$ should be expected and these devices should be treated as ESD sensitive.

**Table 3. RECOMMENDED OPERATING RANGES**

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3 | 5.5 | V |
| Input Voltage | $V_{IN}$ | 0.5 | 13.5 | V |
| Ground | GND | | 0 | V |
| Ambient Temperature | $T_A$ | −40 | 85 | °C |
| Junction Temperature | $T_J$ | −40 | 125 | °C |
| OFF to ON Transition Energy Dissipation Limit (See application section) | $E_{TRANS}$ | 0 | 130 | mJ |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Conditions (Note 6) | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **MOSFET** | | | | | | |
| On−Resistance | $V_{CC}$ = 3.3 V; $V_{IN}$ = 1.8 V | $R_{ON}$ | | 7.7 | 8.9 | mΩ |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 5 V | | | 8.0 | 9.3 | |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 12 V | | | 9.2 | 12.1 | |
| Leakage Current (Note 7) | $V_{EN}$ = 0 V; $V_{IN}$ = 13.5 V | $I_{LEAK}$ | | 0.1 | 1.0 | μA |
| **CONTROLLER** | | | | | | |
| Supply Standby Current (Note 8) | $V_{EN}$ = 0 V; $V_{CC}$ = 3 V | $I_{STBY}$ | | 0.65 | 2.0 | μA |
| | $V_{EN}$ = 0 V; $V_{CC}$ = 5.5 V | | | 3.2 | 4.5 | |
| Supply Dynamic Current (Note 9) | $V_{EN}$ = $V_{CC}$ = 3 V; $V_{IN}$ = 12 V | $I_{DYN}$ | | 180 | 300 | μA |
| | $V_{EN}$ = $V_{CC}$ = 5.5 V; $V_{IN}$ = 1.8 V | | | 475 | 680 | |
| Bleed Resistance | $V_{EN}$ = 0 V; $V_{CC}$ = 3 V | $R_{BLEED}$ | 86 | 115 | 144 | Ω |
| | $V_{EN}$ = 0 V; $V_{CC}$ = 5.5 V | | 72 | 97 | 121 | |
| EN Input High Voltage | $V_{CC}$ = 3 V − 5.5 V | $V_{IH}$ | 2.0 | | | V |
| EN Input Low Voltage | $V_{CC}$ = 3 V − 5.5 V | $V_{IL}$ | | | 0.8 | V |
| EN Input Leakage Current | NCP45541−H; $V_{EN}$ = 0 V | $I_{IL}$ | | 90 | 500 | nA |
| | NCP45541−L; $V_{EN}$ = $V_{CC}$ | $I_{IH}$ | | 90 | 500 | |
| EN Pull Down Resistance | NCP45541−H | $R_{PD}$ | 76 | 100 | 124 | kΩ |
| EN Pull Up Resistance | NCP45541−L | $R_{PU}$ | 76 | 100 | 124 | kΩ |
| PG Output Low Voltage (Note 10) | $V_{CC}$ = 3 V; $I_{SINK}$ = 5 mA | $V_{OL}$ | | | 0.2 | V |
| PG Output Leakage Current (Note 11) | $V_{CC}$ = 3 V; $V_{TERM}$ = 3.3 V | $I_{OH}$ | | 5.0 | 100 | nA |
| Slew Rate Control Constant (Note 12) | $V_{CC}$ = 3 V | $K_{SR}$ | 26 | 33 | 40 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. $V_{EN}$ shown only for NCP45541−H, (EN Active−High) unless otherwise specified.
7. Average current from $V_{IN}$ to $V_{OUT}$ with MOSFET turned off.
8. Average current from $V_{CC}$ to GND with MOSFET turned off.
9. Average current from $V_{CC}$ to GND after charge up time of MOSFET.
10. PG is an open-drain output that is pulled low when the MOSFET is disabled.
11. PG is an open-drain output that is not driven when the gate of the MOSFET is fully charged, requires an external pull up resistor ≥ 1 kΩ to an external voltage source, $V_{TERM}$.
12. See Applications Information section for details on how to adjust the slew rate.

**Table 5. SWITCHING CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified) (Notes 13 and 14)

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Slew Rate | $V_{CC}$ = 3.3 V; $V_{IN}$ = 1.8 V | SR | | 11.8 | | kV/s |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 1.8 V | | | 12.0 | | |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 12 V | | | 13.3 | | |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 12 V | | | 13.5 | | |
| Output Turn−on Delay | $V_{CC}$ = 3.3 V; $V_{IN}$ = 1.8 V | $T_{ON}$ | | 200 | | μs |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 1.8 V | | | 170 | | |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 12 V | | | 260 | | |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 12 V | | | 250 | | |
| Output Turn−off Delay | $V_{CC}$ = 3.3 V; $V_{IN}$ = 1.8 V | $T_{OFF}$ | | 2.0 | | μs |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 1.8 V | | | 1.6 | | |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 12 V | | | 0.7 | | |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 12 V | | | 0.4 | | |
| Power Good Turn−on Time | $V_{CC}$ = 3.3 V; $V_{IN}$ = 1.8 V | $T_{PG,ON}$ | | 1.02 | | ms |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 1.8 V | | | 0.95 | | |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 12 V | | | 1.52 | | |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 12 V | | | 1.23 | | |
| Power Good Turn−off Time | $V_{CC}$ = 3.3 V; $V_{IN}$ = 1.8 V | $T_{PG,OFF}$ | | 20 | | ns |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 1.8 V | | | 14 | | |
| | $V_{CC}$ = 3.3 V; $V_{IN}$ = 12 V | | | 20 | | |
| | $V_{CC}$ = 5.0 V; $V_{IN}$ = 12 V | | | 14 | | |

13. See below figure for Test Circuit and Timing Diagram.
14. Tested with the following conditions: $V_{TERM}$ = $V_{CC}$; $R_{PG}$ = 100 kΩ; $R_L$ = 10 Ω; $C_L$ = 0.1 μF.

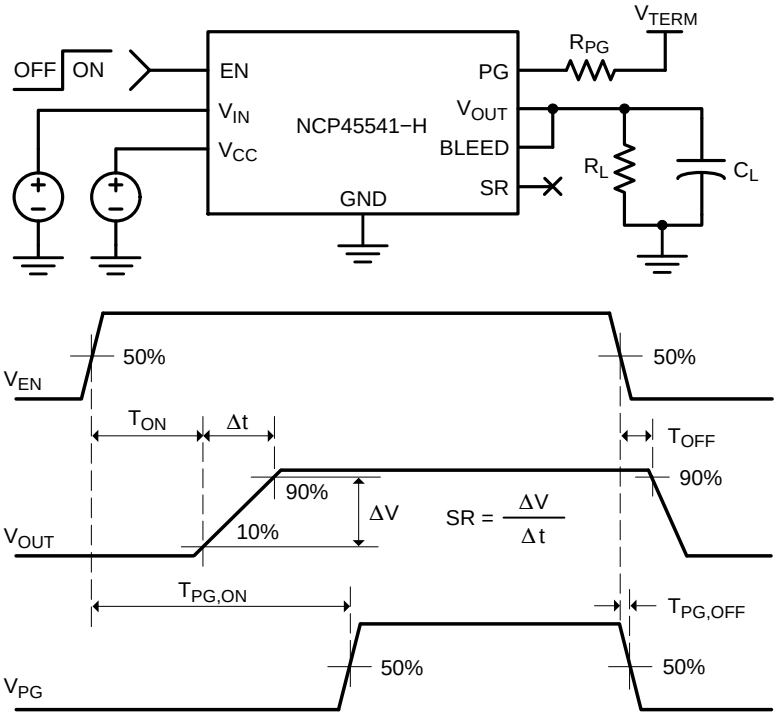


**Figure 2. Switching Characteristics Test Circuit and Timing Diagrams**

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise specified)

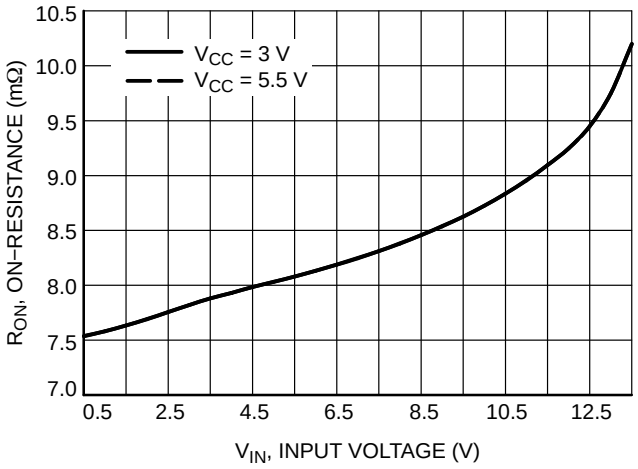


**Figure 3. On−Resistance vs. Input Voltage**

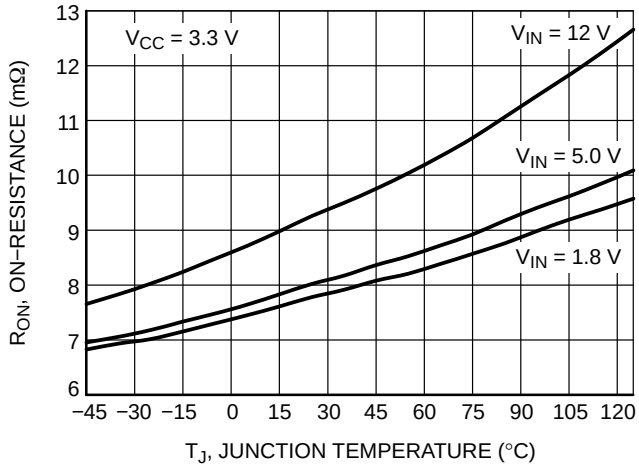


**Figure 4. On−Resistance vs. Temperature**

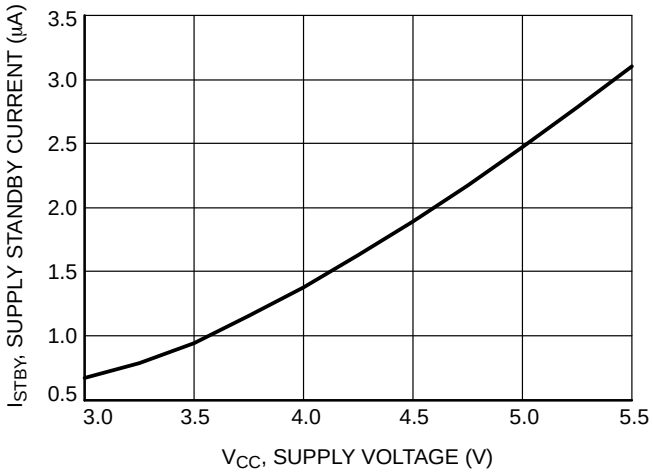


**Figure 5. Supply Standby Current vs. Supply Voltage**

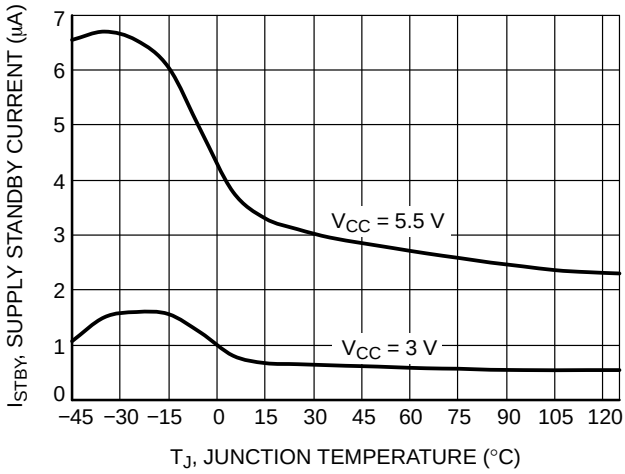


**Figure 6. Supply Standby Current vs. Temperature**

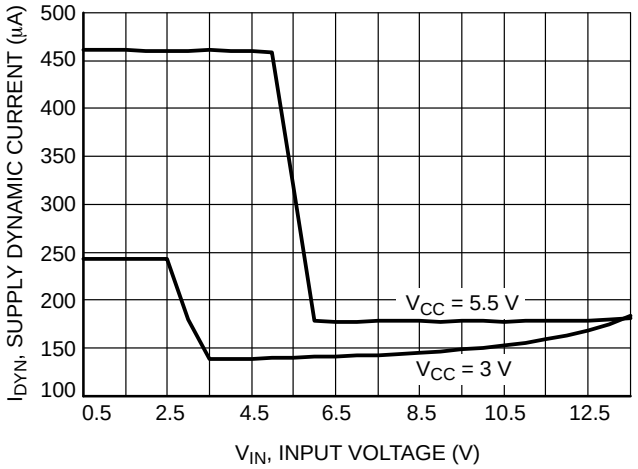


**Figure 7. Supply Dynamic Current vs. Input Voltage**

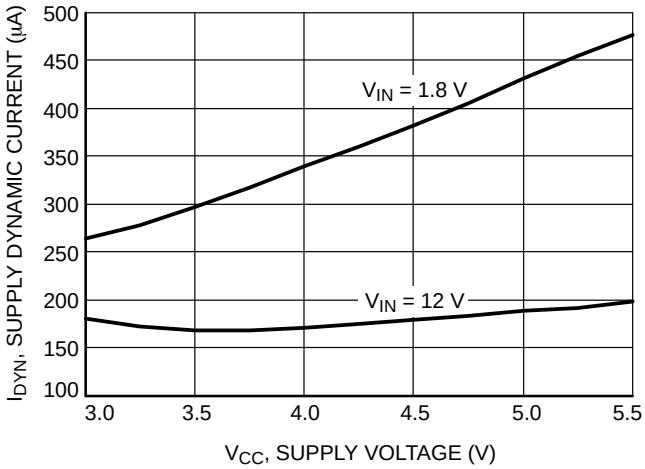


**Figure 8. Supply Dynamic Current vs. Supply Voltage**

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise specified)

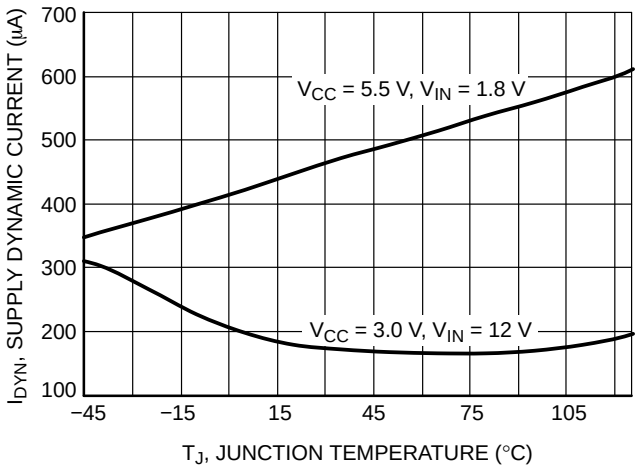


**Figure 9. Supply Dynamic Current vs. Temperature**

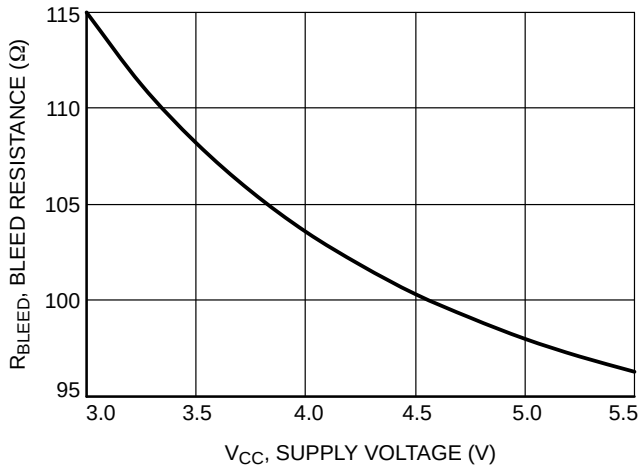


**Figure 10. Bleed Resistance vs. Supply Voltage**

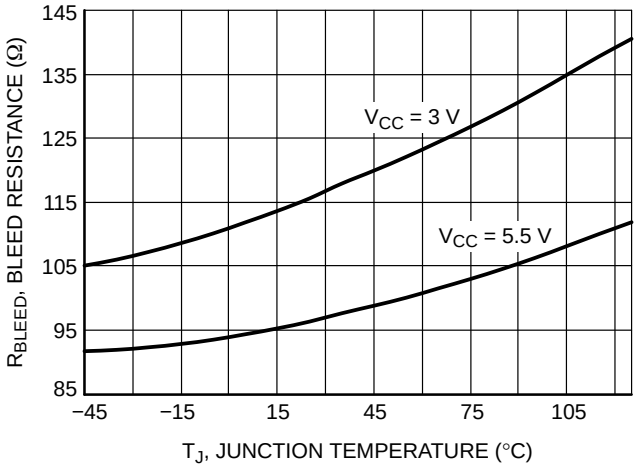


**Figure 11. Bleed Resistance vs. Temperature**

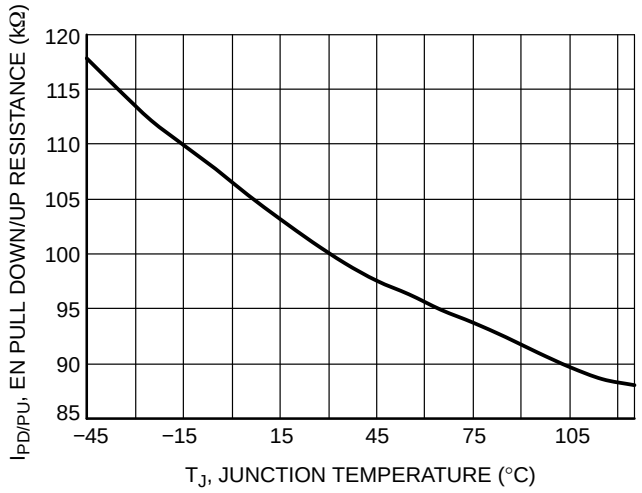


**Figure 12. EN Pull Down/Up Resistance vs. Temperature**

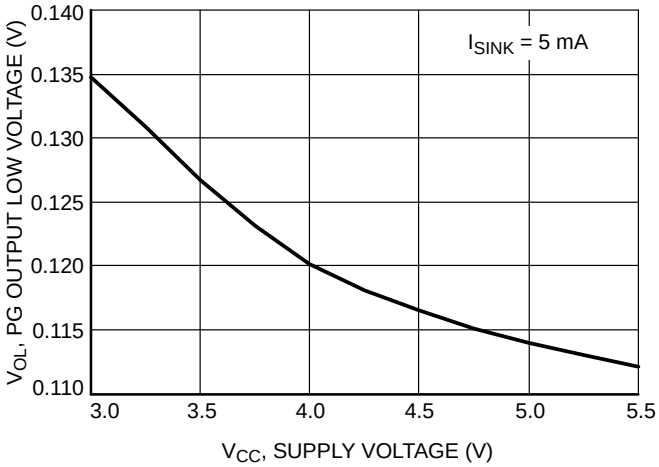


**Figure 13. PG Output Low Voltage vs. Supply Voltage**

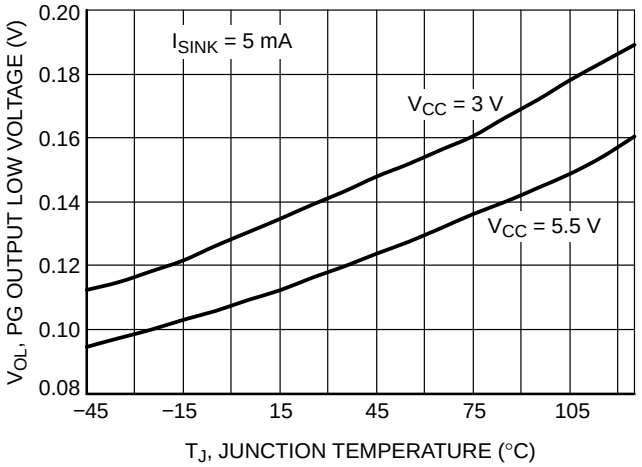


**Figure 14. PG Output Low Voltage vs. Temperature**

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise specified)

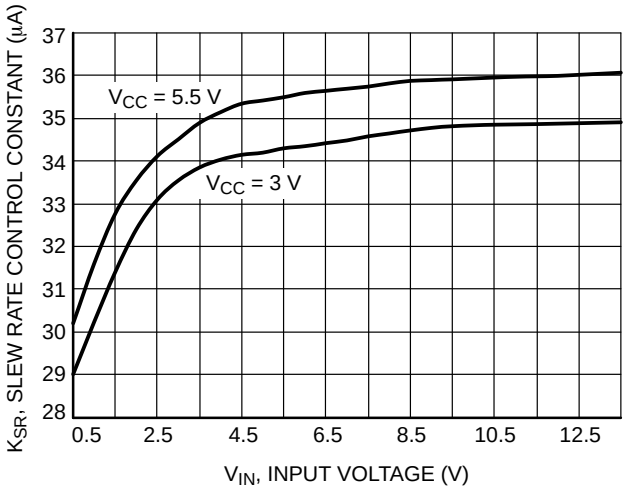


**Figure 15. Slew Rate Control Constant vs. Input Voltage**

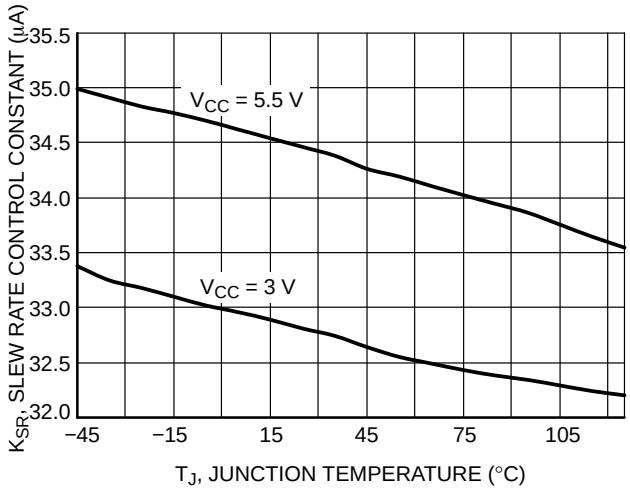


**Figure 16. Slew Rate Control Constant vs. Temperature**

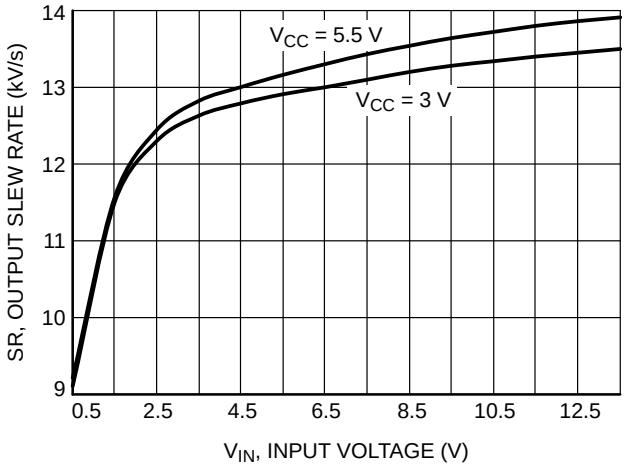


**Figure 17. Output Slew Rate vs. Input Voltage**

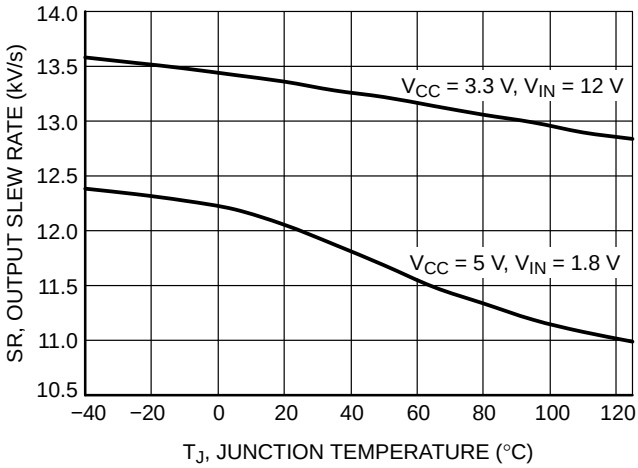


**Figure 18. Output Slew Rate vs. Temperature**

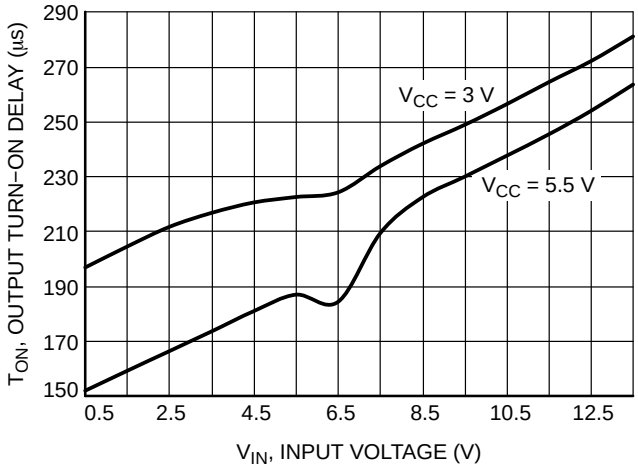


**Figure 19. Output Turn−on Delay vs. Input Voltage**

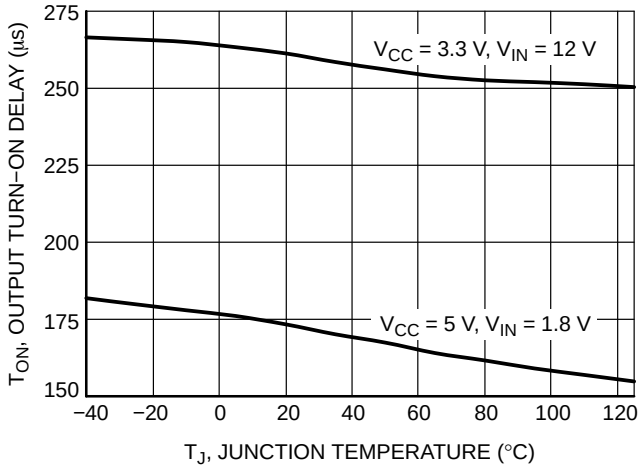


**Figure 20. Output Turn−on Delay vs. Temperature**

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise specified)

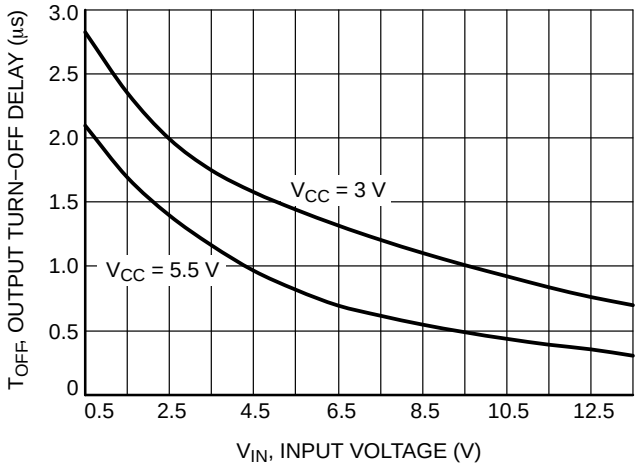


**Figure 21. Output Turn−off Delay vs. Input Voltage**

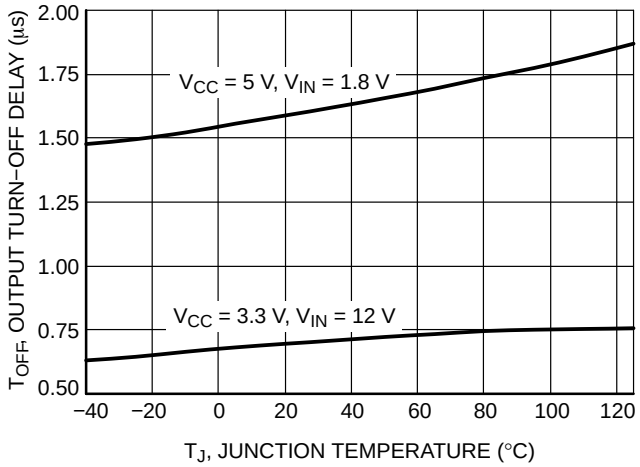


**Figure 22. Output Turn−off Delay vs. Temperature**

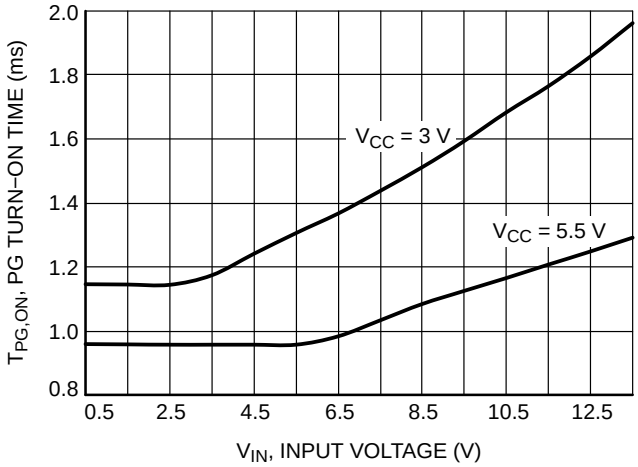


**Figure 23. Power Good Turn−on Time vs. Input Voltage**

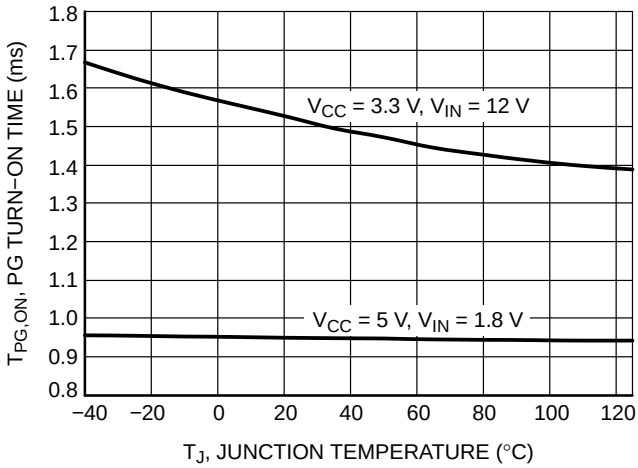


**Figure 24. Power Good Turn−on Time vs. Temperature**

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise specified)

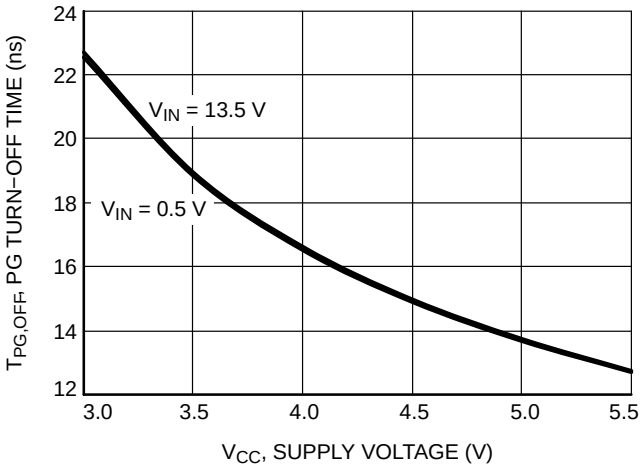


**Figure 25. Power Good Turn−off Time vs. Supply Voltage**

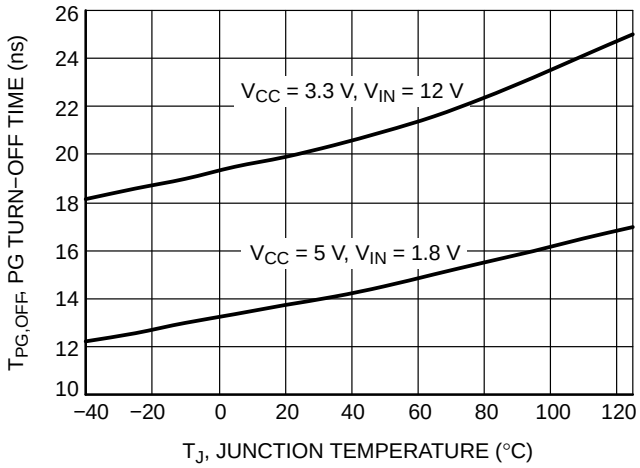


**Figure 26. Power Good Turn−off Time vs. Temperature**

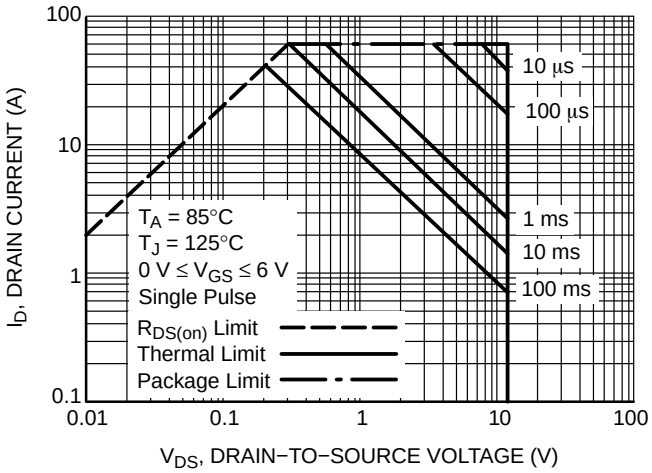


**Figure 27. Maximum Rated Forward Biased Safe Operating Area**

## APPLICATIONS INFORMATION

### Enable Control

The NCP45541 has two part numbers, NCP45541−H and NCP45541−L, that only differ in the polarity of the enable control.

The NCP45541−H device allows for enabling the MOSFET in an active−high configuration. When the $V_{CC}$ supply pin has an adequate voltage applied and the EN pin is at a logic high level, the MOSFET will be enabled. Similarly, when the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not being driven.

The NCP45541−L device allows for enabling the MOSFET in an active−low configuration. When the $V_{CC}$ supply pin has an adequate voltage applied and the EN pin is at a logic low level, the MOSFET will be enabled. Similarly, when the EN pin is at a logic high level, the MOSFET will be disabled. An internal pull up resistor to $V_{CC}$ on the EN pin ensures that the MOSFET will be disabled when not being driven.

### Power Sequencing

The NCP45541 devices will function with any power sequence, but the output turn−on delay performance may vary from what is specified. To achieve the specified performance, there are two recommended power sequences:

1. $V_{CC} \rightarrow V_{IN} \rightarrow V_{EN}$
2. $V_{IN} \rightarrow V_{CC} \rightarrow V_{EN}$

$V_{CC}$ must be at 2 V or higher when EN is asserted to ensure that the enable is latched properly for correct operation. If EN comes up before $V_{CC}$ reaches 2 V, then the EN may not take effect.

### Load Bleed (Quick Discharge)

The NCP45541 devices have an internal bleed resistor, $R_{BLEED}$, which is used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch that is enabled whenever the MOSFET is disabled. The MOSFET and the bleed switch are never concurrently active.

It is required that the BLEED pin be connected to $V_{OUT}$ either directly (as shown in Figure 29) or through an external resistor, $R_{EXT}$ (as shown in Figure 28). $R_{EXT}$ should not exceed 100 MΩ and can be used to increase the total bleed resistance and decrease the load bleed rate.

Care must be taken to ensure that the power dissipated across $R_{BLEED}$ is kept at a safe level. The maximum continuous power that can be dissipated across $R_{BLEED}$ is 0.4 W. $R_{EXT}$ can be used to decrease the amount of power dissipated across $R_{BLEED}$.

### Power Good

The NCP45541 devices have a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active−high, open−drain output that requires an external pull up resistor, $R_{PG}$, greater than or equal to 1 kΩ to an external voltage source, $V_{TERM}$, compatible with input levels of other devices connected to this pin (as shown in Figures 28 and 29).

The power good output can be used as the enable signal for other active−high devices in the system (as shown in Figure 30). This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

### Slew Rate Control

The NCP45541 devices are equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swap applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground (as shown in Figures 28 and 29). With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}}\ [V/s] \qquad \text{(eq. 1)}$$

where $K_{SR}$ is the specified slew rate control constant, found in Table 4, and $C_{SR}$ is the slew rate control capacitor added between the SR pin and ground. The slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the $C_{SR}$ is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value. The SR pin can be left floating if the slew rate does not need to be decreased.

### Capacitive Load

The peak in−rush current associated with the initial charging of the application load capacitance needs to stay below the specified $I_{MAX}$. CL (capacitive load) should be less than Cmax as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \qquad \text{(eq. 2)}$$

Where $I_{MAX}$ is the maximum load current, and SRtyp is the typical default slew rate when no external load capacitor is added to the SR pin.

### OFF to ON Transition Energy Dissipation

The energy dissipation due to load current traveling from $V_{IN}$ to $V_{OUT}$ is very low during steady state operation due to the low $R_{ON}$. When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from $V_{IN}$ to $V_{OUT}$ transitions from high impedance to $R_{ON}$, and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN} \cdot \left(I_{INRUSH} + 0.8 \cdot I_{LOAD}\right) \cdot dt \qquad \text{(eq. 3)}$$

Where $V_{IN}$ is the voltage on the $V_{IN}$ pin, $I_{INRUSH}$ is the inrush current caused by capacitive loading on $V_{OUT}$, and dt is the time it takes $V_{OUT}$ to rise from 0 V to $V_{IN}$. $I_{INRUSH}$ can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \qquad \text{(eq. 4)}$$

Where dv/dt is the programmed slew rate, and $C_L$ is the capacitive loading on $V_{OUT}$. To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to $E_{TRANS}$ listed in operating ranges table.

## ecoSWITCH LAYOUT GUIDELINES

### Electrical Layout Considerations

Correct physical PCB layout is important for proper low noise accurate operation of all ecoSWITCH products.

**Power Planes:** The ecoSWITCH is optimized for extremely low Ron resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the VIN and VOUT pins of the ecoSWITCH to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSWITCH requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. Direct coupling of VIN to VOUT should be avoided, as this will adversely affect slew rates. The figure below shows an example of correct power plane layout. The number and location of pins for specific ecoSWITCH products may vary. This demonstrates large planes for both VIN and VOUT, while avoiding capacitive coupling between the two planes.

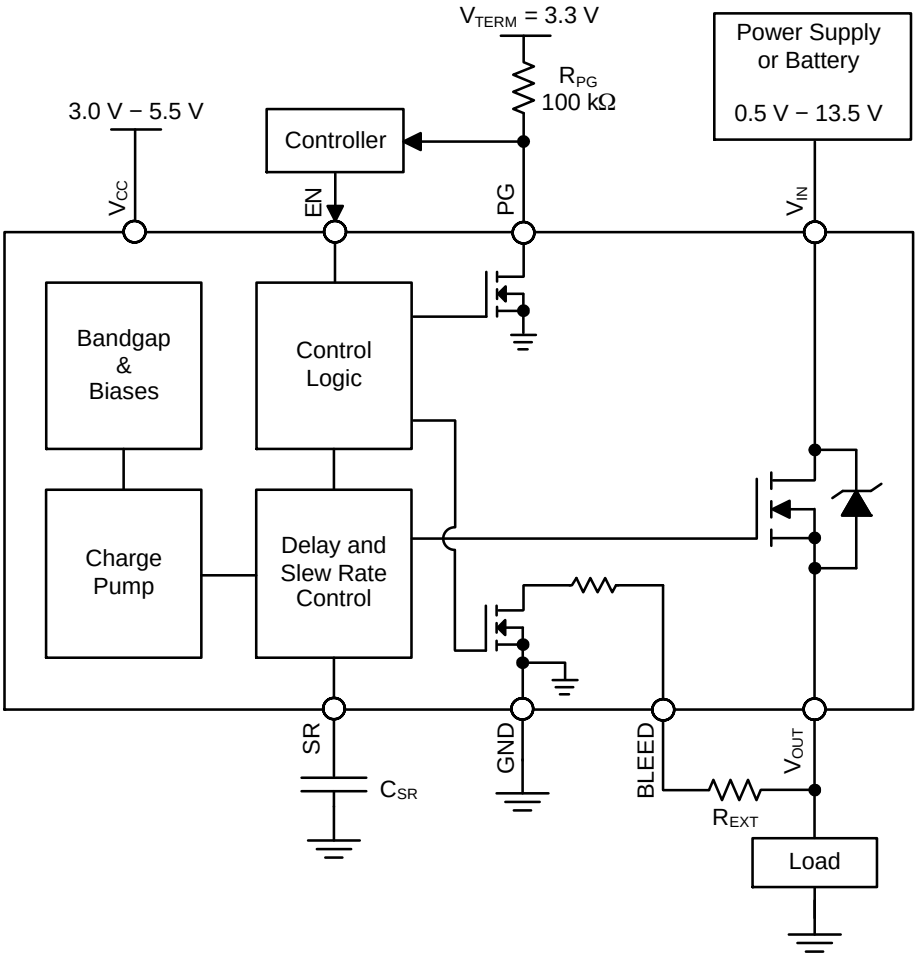


**Figure 28. Typical Application Diagram − Load Switch**

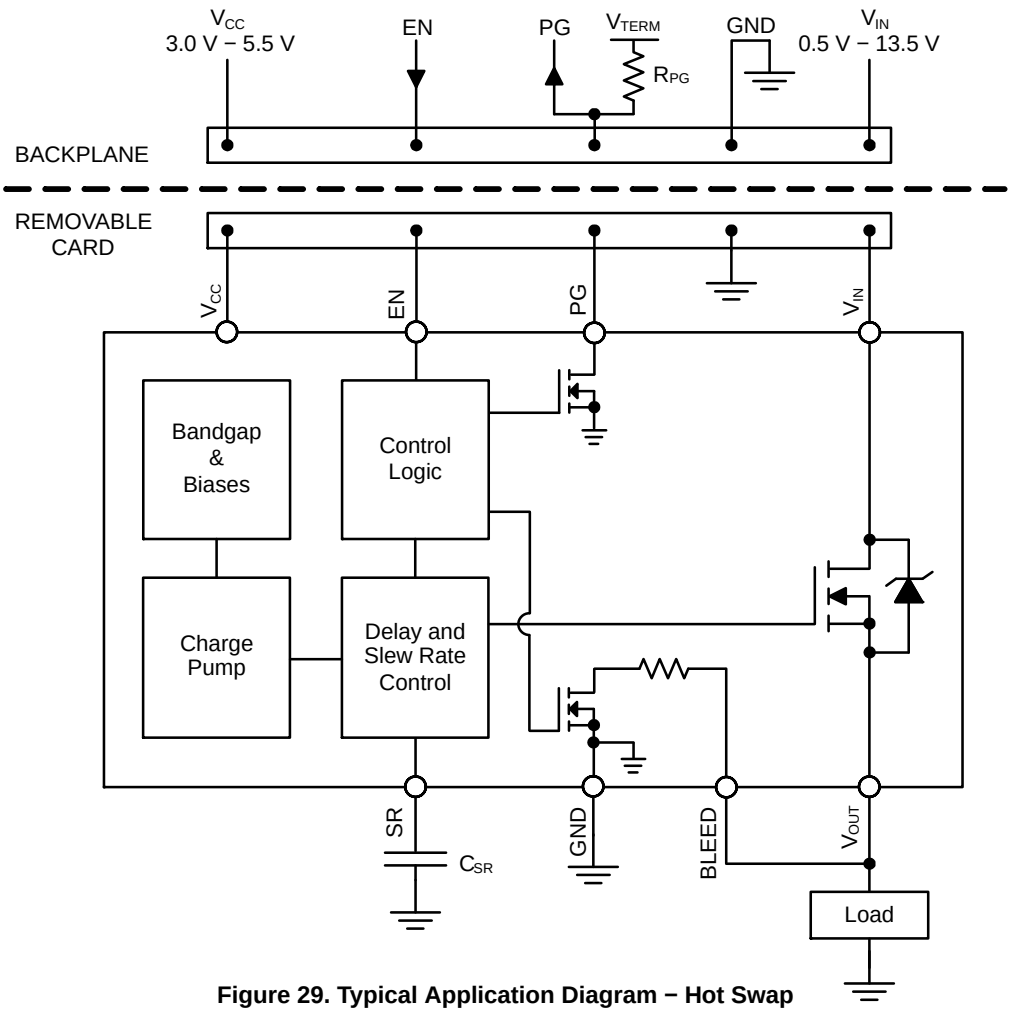


**Figure 29. Typical Application Diagram − Hot Swap**

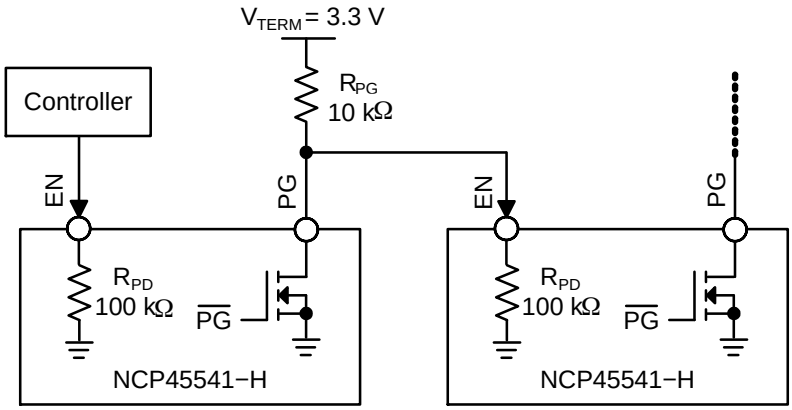


**Figure 30. Simplified Application Diagram − Power Sequencing with PG Output**

## ORDERING INFORMATION

| Device | EN Polarity | Package | Shipping† |
|---|---|---|---|
| NCP45541IMNTWG−H | Active−High | DFN12 (Pb−Free) | 3000 / Tape & Reel |
| NCP45541IMNTWG−L | Active−Low | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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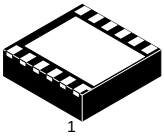
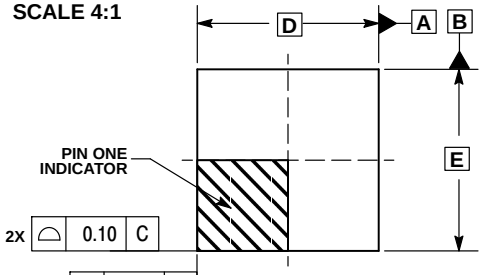
**DFN12 3x3, 0.5P**
CASE 506CD
ISSUE A

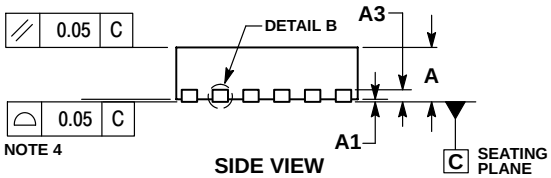
DATE 18 FEB 2014



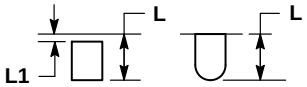
SCALE 4:1



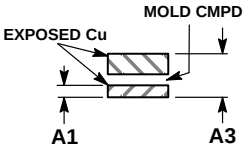

TOP VIEW



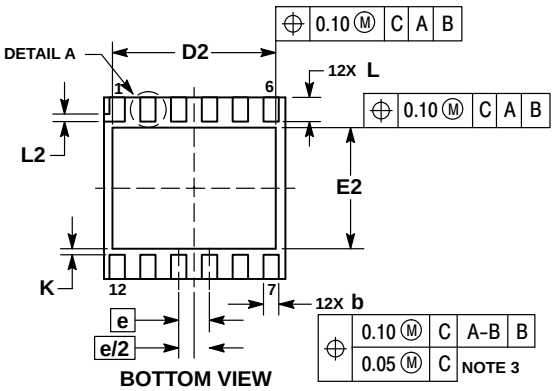

SIDE VIEW




DETAIL A
ALTERNATE CONSTRUCTIONS

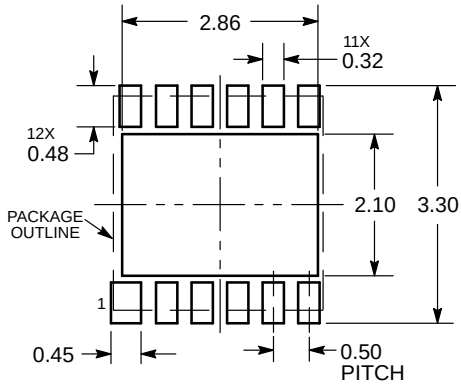



DETAIL B
ALTERNATE CONSTRUCTION




BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 3.00 BSC | |
| D2 | 2.60 | 2.80 |
| E | 3.00 BSC | |
| E2 | 1.90 | 2.10 |
| e | 0.50 BSC | |
| L | 0.20 | 0.40 |
| L1 | −−− | 0.15 |
| L2 | 0.10 REF | |
| K | 0.15 MIN | |

GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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