NCP5369N

Integrated Driver and MOSFET

The NCP5369N integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a 6 mm x 6 mm 40−pin QFN package. The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP5369N integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Switching Frequencies Up to 1 MHz
- Capable of Output Currents Up to 35 A
- Internal Bootstrap Diode
- Zero Current Detection
- Undervoltage Lockout
- Internal Thermal Warning / Thermal Shutdown
- These are Pb−Free Devices

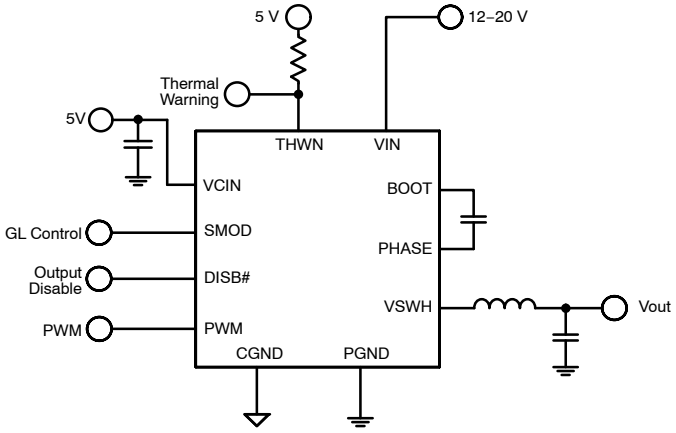

Figure 1. Application Schematic

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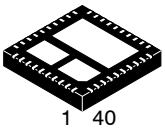


QFN40
MN SUFFIX
CASE 485AZ

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5369NMNTXG	QFN40 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

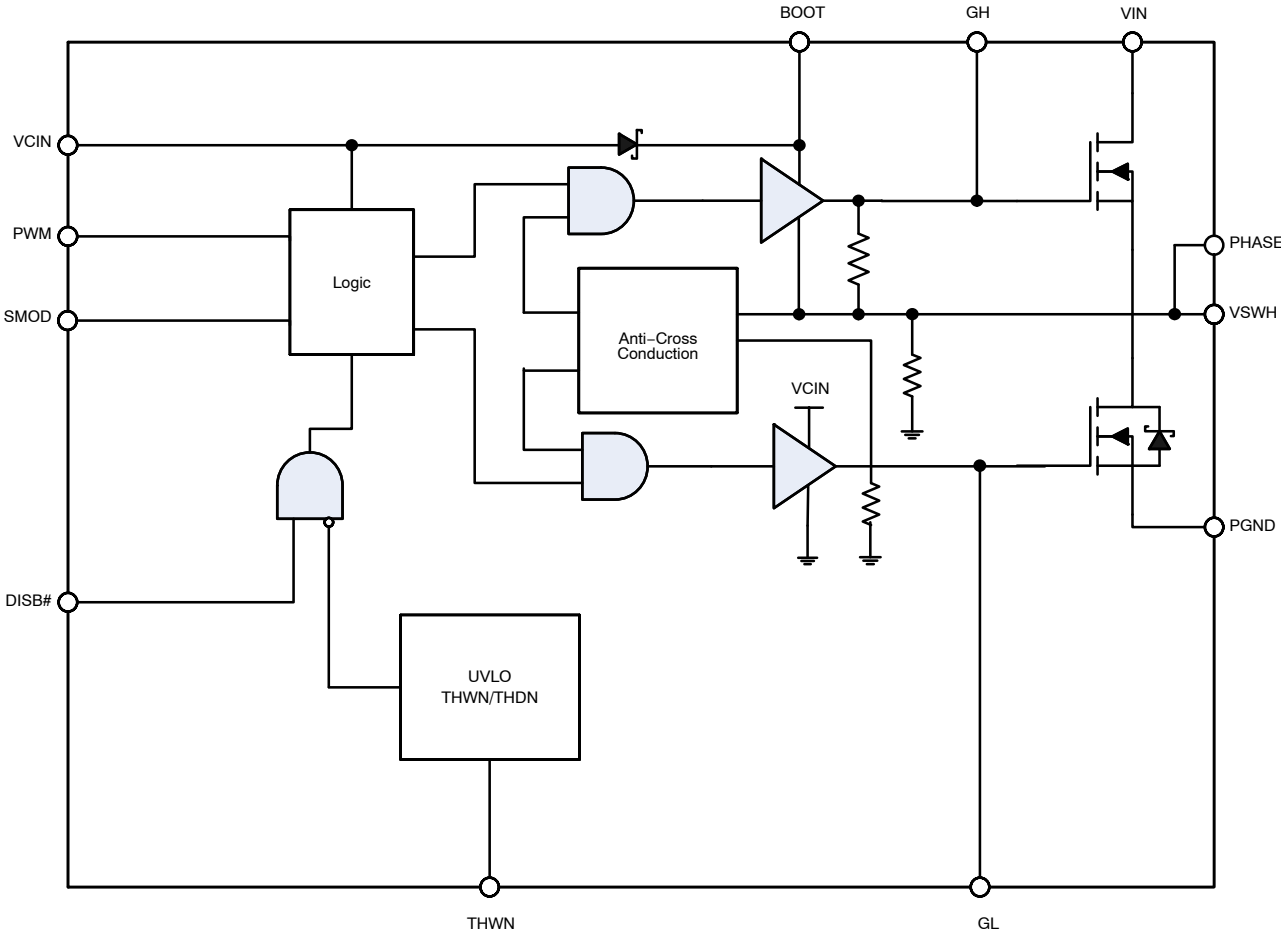


Figure 2. Simplified Block Diagram

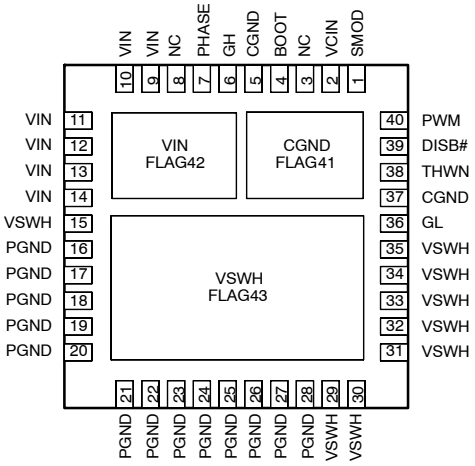


Figure 3. Pin Connections (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	SMOD	GL Control
2	VCIN	Control Input Voltage
3, 8	NC	No Connect
4	BOOT	Bootstrap Voltage
5, 37, FLAG 41	CGND	Control Signal Ground
6	GH	High Side FET Gate Access
7	PHASE	Provides a return path for the high side driver of the internal IC. Place a high frequency ceramic capacitor of 0.1 μF to 1.0 μF from this pin to BOOT pin.
9−14, FLAG 42	VIN	Input Voltage
15, 29−35, FLAG 43	VSWH	Switch Node Output
16−28	PGND	Power Ground
36	GL	Low Side FET Gate Access
38	THWN	Thermal Warning
39	DISB#	Output Disable Pin
40	PWM	PWM Drive Logic

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Pin Name / Rating	Min	Max	Unit
VCIN	Control Input Voltage	−0.3	7	V
VIN	Power Input Voltage	−0.3	30	V
BOOT	Bootstrap Voltage	−0.3 V wrt/VSWH (pin 35)	35 V wrt/PGND 40 V < 50 ns wrt/PGND 7 V wrt/GH 7.7 V < 50 ns wrt/GH	V
VSWH	Switch Node Output	−5 V −10 V < 200 ns	35 V 40 V < 50 ns	V
GH	High Side Gate Access	−0.3 V wrt/VSWH (pin 35)	7 V wrt/VSWH (pin 35) 7.7 V < 50 ns wrt/VSWH (pin 35)	V
SMOD	GL Control	−0.3	6.5	V
PWM	PWM Drive Logic	−0.3	6.5	V
DISB#	Output Disable	−0.3	6.5	V
THWN	Thermal Warning	−0.3	6.5	V
T_J	Junction Temperature	−55 to 150		°C
T_S	Storage Temperature	−55 to 150		°C
$R_{\theta JPCB}$	Thermal Resistance, High−Side FET	13		°C/W
$R_{\theta JPCB}$	Thermal Resistance, Low−Side FET	5		°C/W
MSL	Moisture Sensitivity Level	3		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Control Input Voltage	VCIN	4.5	5	5.5	V
Input Voltage	VIN	4.5	12	25	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 1) (VCIN = 5 V, VIN = 12 V, T_A = −10°C to +100°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
VCIN Current (normal mode)	–	DISB# = 5 V, PWM = OSC, FSW = 400 kHz		14	20	mA
VCIN Current (shutdown mode)	–	DISB# = GND		15	30	μA
UNDERVOLTAGE LOCKOUT						
UVLO Startup	–		3.8	4.35	4.5	V
UVLO Hysteresis	–		150	200	250	mV
BOOTSTRAP DIODE						
Forward Voltage	–	VCIN = 5 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT						
PWM Input Voltage High	V_{PWM_HI}		3.7	–	–	V
PWM Input Voltage Mid−State	V_{PWM_MID}		1.3	–	3.0	V
PWM Input Voltage Low	V_{PWM_LO}		–	–	0.7	V
PWM Input Leakage				50		nA
Zero Cross Detect Threshold				−6		mV
ZCD Blanking Timer				250		ns
OUTPUT DISABLE						
Output Disable Input Voltage High	$V_{DISB\#\_HI}$		2.0	–	–	V
Output Disable Input Voltage Low	$V_{DISB\#\_LO}$		–	–	0.8	V
Output Disable Hysteresis	–		–	500	–	mV
Output Disable Propagation Delay			–	20	40	ns
SMOD PIN INPUT						
SMOD	V_{SMOD_HI}		2.0	–	–	V
SMOD	V_{SMOD_LO}		–	–	0.8	V
THERMAL WARNING/SHUTDOWN						
Thermal Warning Temperature				150		°C
Thermal Warning Hysteresis				15		°C
Thermal Shutdown Temperature				180		°C
Thermal Shutdown Hysteresis				25		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

APPLICATIONS INFORMATION

Theory of Operation

The NCP5369N is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCIN and PGND.

High−Side Driver

The high−side driver is designed to drive a floating low RDS(on) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH) pin.

The bootstrap circuit is comprised of the internal diode and an external bootstrap capacitor. When the NCP5369N is starting up, the VSWH pin is at ground, so the bootstrap capacitor will charge up to VCIN through the bootstrap diode See Figure 1. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the VSWH pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 5 V plus the charge of the bootstrap capacitor (approaching 17 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Zero Current Detect

When PWM is set high, DRVH will be set high after the adaptive non−overlap delay. When PWM is set low, DRVL will be set high after the adaptive non−overlap delay.

When PWM is set to the mid state, DRVH will be set low, and after the adaptive non−overlap delay, DRVL will be set high. DRVL remains high during the ZCD blanking time. When the timer has expired, the VSWH pin will be monitored for zero cross detection. After the detection, DRVL will be set low. The zero current detection timing is illustrated in Figure 4.

The threshold on VSWH to determine zero current undergoes an auto−calibration cycle every time DISB# is brought from low to high. This auto−calibration cycle typically takes 55 μs to complete.

Low−side MOSFET Control

Besides the tri-state PWM input, the SMOD can controls the low-side MOSFET on/off without any delay. This allows controller implements advanced features of immediate OVP protection and body−diode braking. The SMOD timing is illustrated in Figure 5. The combination of tri−state PWM and SMOD control is listed in the table below.

PWM	SMOD	GH	GL
H	Do not care	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
M	H	OFF	OFF, after blanking time and ZCD is triggered
M	L	OFF	OFF, immediately

With the above logic table, the NCP5369N supports two types of PWM controllers. The first type has tri−state PWM output, including NCP81102, NCP81119, NCP6153, NCP6133, NCP6151 and NCP6131. The other type has 2−state PWM output and SMOD output with its own zero current detection, including NCP81105, NCP81001, NCP81111 and NCP4200 family.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The NCP5369N prevents cross conduction by monitoring the status of the MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, the gate of the low−side MOSFET (GL pin) will go low after a propagation delay (tpdlGL). The time it takes for the low−side MOSFET to turn off (tfGL) is dependent on the total charge on the low−side MOSFET gate. The NCP5369N monitors the gate voltage of both MOSFETs and the switchnode voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhGH) the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, the gate of the high−side MOSFET (GH pin) will go low after the propagation delay (tpdlGH). The time to turn off the high−side MOSFET (tfGH) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay (tpdhGL) the turn on of the low−side MOSFET.

Thermal Warning / Thermal Shutdown

When the temperature of the driver reaches 150°C, the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops below 135°C, the THWN will go high.

If the driver temperature exceeds 180°C, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls below 155°C, the part will resume normal operation. The THWN pin has a maximum current capability of 30 mA.

Power Supply Decoupling

The NCP5369N can source and sink relatively large current to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (VCIN) a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal diode. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. A bootstrap capacitance greater than 100 nF and a minimum 50 V rating is recommended. A good quality ceramic capacitor should be used.

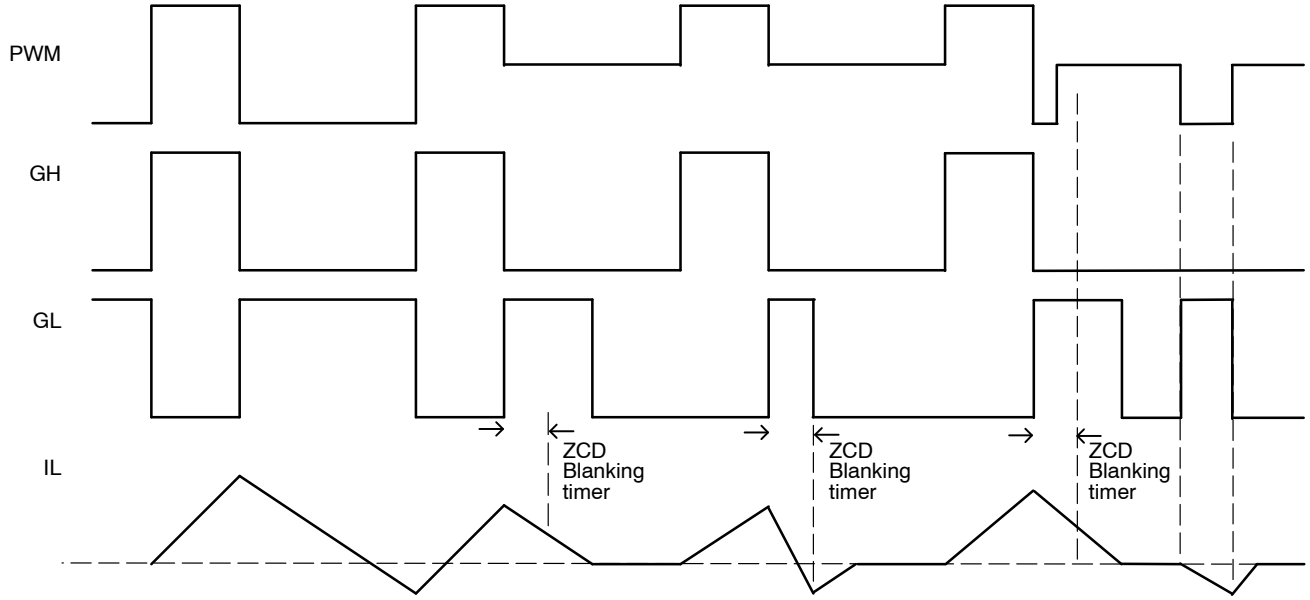


Figure 4. Zero Current Detection

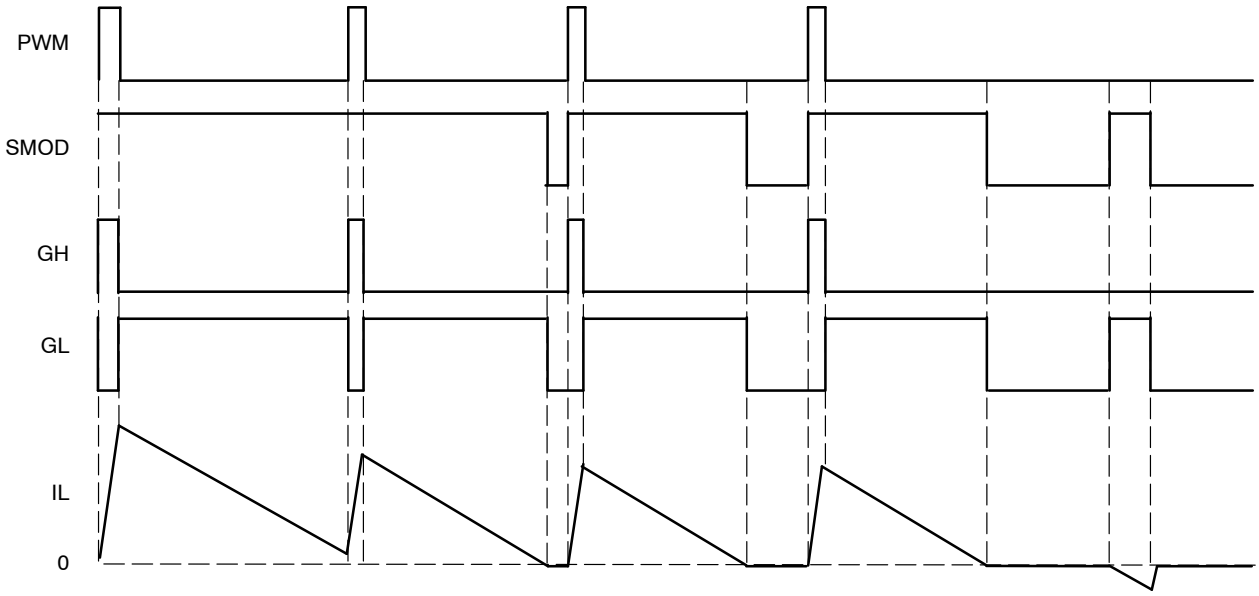
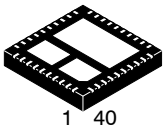


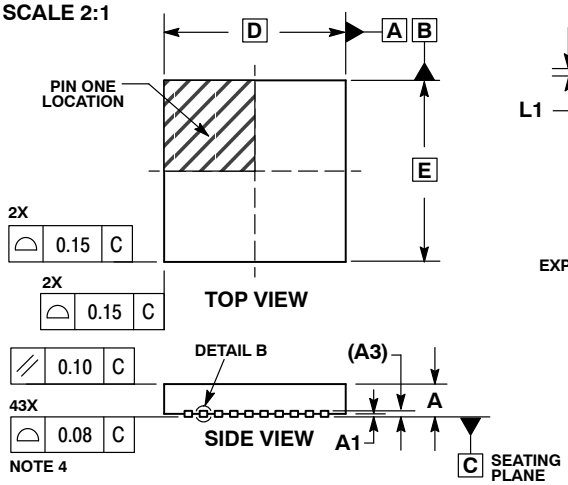
Figure 5. SMOD Control

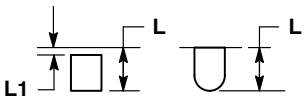
QFN40 6x6, 0.5P
CASE 485AZ
ISSUE O

DATE 09 JAN 2009

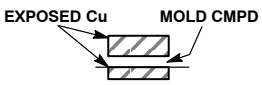


SCALE 2:1

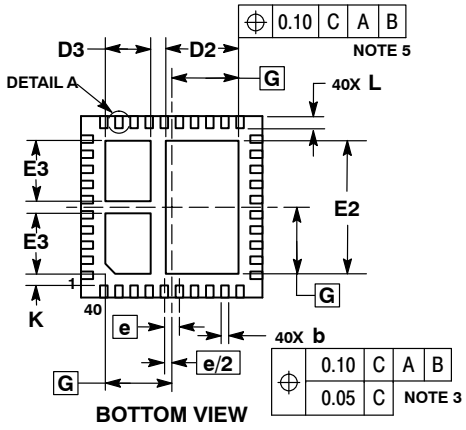




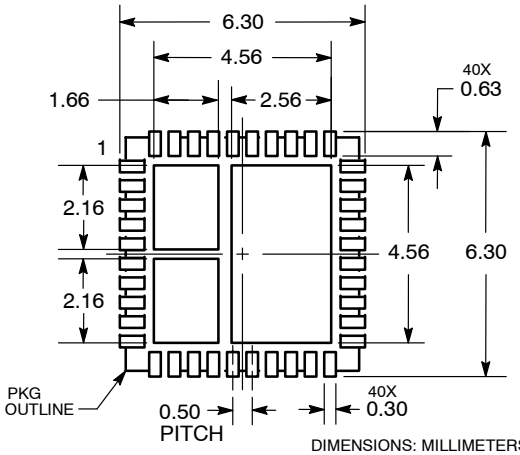
DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.30	2.50
D3	1.40	1.60
E	6.00 BSC	
E2	4.30	4.50
E3	1.90	2.10
e	0.50 BSC	
G	2.20 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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