High Efficiency Charge Pump Converter

The NCP5603 is an integrated circuit dedicated to the medium power White LED applications. The power conversion is achieved by means of a charge pump structure, using two external ceramic capacitors, making the system extremely tiny. The device supplies a constant voltage to the load from a low battery voltage source. It is particularly suited for the High Efficiency LED used in low cost, low power applications, with high extended battery life.

Features

- Wide Battery Supply Voltage Range: $2.7 < V_{CC} < 5.5 V$
- Automatic Operating Mode 1X, 1.5X and 2X Improves Efficiency
- Dimmable Output Current
- Up to 350 mA Output Pulsed Current
- Selectable Output Voltage
- High Efficiency Up To 90%
- Supports 2.5 kV ESD, Human Body Model
- THIS DEVICE IS IN SECONTATIVE FOR REPRESENTATIVE FOR REPRESENTATIVE REPRESENTATIVE • Supports 200 V Machine Model ESD
- Low 40 mA Short Circuit Current
- Pb-Free Package is Available

Applications

- High Power LED
- Back Light Display
- High Power Flash



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ORDERING INFORMATION

Device	Package	Shipping [†]
NCP5603MNR2	DFN10	3000/ Tape & Reel
NCP5603MNR2G	DFN10 (Pb-Free)	3000/ Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.





PIN FUNCTION DESCRIPTION

Pin	Symbol	Туре	Description		
1	V _{out}	OUTPUT, PWR	This pin supplies the regulated voltage to the external LED. Since high current transients are present in this pin, care must be observed to avoid voltage spikes in the system. Good high frequency layout technique must be observed.		
2	C1N	POWER	One side of the external charge pump capacitor (C _{FLY}) is connected to this pin, associated with C1P, pin 9. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.		
3	V _{bat}	POWER	This pin shall be connected to the power source, and must be decoupled to Ground by a low ESR capacitor (2.2 μ F/6.3 V ceramic or better (see Note 1)).		
4	Fsel	INPUT, Digital	This pin is used to program the operating frequency: Fsel = 0 \rightarrow Fop = 262 kHz Fsel = 1 \rightarrow Fop = 650 kHz		
5	Vsel	INPUT, Digital	This pin setup the output voltage: Vsel = $0 \rightarrow V_{out} = 4.5 \text{ V}$ Vsel = $1 \rightarrow V_{out} = 5.0 \text{ V}$		
6	EN/PWM	INPUT, Digital	 This pin controls the activity of the NCP5603 chip: EN/PWM = Low → the chip is deactivated, the load is disconnected EN/PWM = High → the chip is activated and the load is connected to the regulated output current. The NCP5603 can operate either in a continuous mode (EN/PWM = High), or can be controlled by a PWM pulse applied to EN/PWM to dim the output light. When EN/PWM is Low, the external load is disconnected from the converter, providing a very low standby current. The pull down built-in resistance makes sure the chip is deactivated even if the EN/PWM pin is disconnected (see Note 2). 		
7	C2N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2P, pin 10. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.		
8	GND	GROUND	This pin combines the Signal ground and the Power ground and must be connected to the system ground. Using good quality ground plane is mandatory to avoid spikes on the logic signal lines.		
9	C1P	POWER	One side of the external charge pump capacitor (C _{FLY}) is connected to this pin, associated with C1N, pin 2. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.		
10	C2P	POWERS	One side of the external charge pump capacitor is connected to this pin, associated with C2N, pin 7. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.		

1. Using ceramic 16 V working voltage capacitors is recommended to compensate the DC bias effect encountered with such type of capacitors. 2. Any external impedance connected to pin 6 shall be 10 k Ω or higher.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{bat}	7.0	V
Power Supply Current	I _{bat}	800	mA
Digital Input Pins	V _{in}	-0.5 V < Vbat < Vbat +0.5 V < 6.0 V	V
Digital Input Pins	lin	± 5.0	mA
Output Voltage	V _{out}	5.5	V
ESD Capability (Note 3) Human Body Model Machine Model	V _{ESD}	2.5 200	kV V
DFN10, 3x3 Package Power Dissipation @ Tamb = +85°C Thermal Resistance, Junction-to-Air (R _{0JA})	P _{DS} R _{θJA}	580 68.5	mW °C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature Range	TJ	-40 to +125	°C
Maximum Junction Temperature	T _{Jmax}	+150	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Latchup Current Maximum Rating		100 mA per JEDEC standard, JESD78	
Moisture Sensitivity Level (MSL)		1 per IPC/JEDEC standard, J-STD-020A	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device series contains ESD protection and exceeds the following tests: Human Body Model (HBM) ±2.5 kV per JEDEC Standard: JESD22–A114
- Machine Model (MM) ± 200 V per JEDEC Standard: JESD22-A115. 4. The maximum package power dissipation limit must not be exceeded.

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ELECTRICAL CHARACTERISTICS @ 2.85 V < Vbat < 5.5 V	(-40°C to +85°C ambient temperature, unless otherwise noted).
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Characteristic	Din	Symbol	Min	Turn	Mox	Unit
Characteristic	Pin	Symbol	IVIIN	тур	Max	Unit
Power Supply	3	V _{bat}	2.85	-	5.5	V
Quiescent Current @ V _{bat} = 3.7 V, I _{out} = 0 μA @ Pulsed Clock Fop = 262 kHz @ Pulsed Clock Fop = 650 kHz @ Continuous Clock Fop = 262 kHz @ Continuous Clock Fop = 650 kHz	3	lqsc	- - -	- 1.0 2.1	0.8 1.2 - -	mA
Shutdown Current @ I_{out} = 0 mA, EN/PWM = L @ 2.85 < V_{bat} < 4.2 V @ V_{bat} = 5.5 V	3	I _{stdb}	-	-	2.5 4.0	μΑ
Output Voltage Regulation @ Vsel = 1, 2.85 V < V _{bat} < 4.3 V @ Vsel = 0, 2.85 V < V _{bat} < 4.3 V	3	V _{out}	4.75 4.275	5.0 4.5	5.25 4.725	V
$\begin{array}{l} \mbox{Continuous DC Load Current (Note 7)} \\ \mbox{Cin} = 1.0 \ \mu\mbox{F}, \ \mbox{C}_{FLY} = 1.0 \ \mu\mbox{F}, \ \mbox{Cout} = 1.0 \ \mu\mbox{F} \\ \mbox{$@Vsel} = 1, 3.2 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 3.2 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 1, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$@Vsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{V} < V_{bat} < 4.3 \ \mbox{V} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{W} < 0.5 \ \mbox{W} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{W} < 0.5 \ \mbox{W} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{W} < 0.5 \ \mbox{W} \\ \mbox{$Wsel} = 0, 2.85 \ \mbox{W} < 0.5 \ \mbox{W} \\ \mbox{W} \ \mbox{W} $	3	l _{out}	- -		60 200 80 120	mA
$ \begin{array}{l} \mbox{Pulsed Output Current} \\ \mbox{Cin} = 10 \ \mu\mbox{F}, \ \mbox{C}_{FLY} = 1.0 \ \mu\mbox{F}, \ \mbox{Cout} = 10 \ \mu\mbox{F}, \ \ \mbox{V}_{bat} = 3.6 \ \ \mbox{V} \\ \mbox{Pwidth} = 500 \ \ \mbox{ms}, \ -40^\circ\mbox{C} < T_A < +65^\circ\mbox{C} \end{array} $	3	IFLH	FOR	350	<u> </u>	mA
Output Continuous Short Circuit Current, V _{out} = 0 V	3	lsch	-nS	40	100	mA
Operating Frequency (Note 5) @ Fsel = 0, 2.85 V < V _{bat} < 4.5 V @ Fsel = 1, 2.85 V < V _{bat} < 4.5 V		Fop	210 500	262 650	320 1000	kHz
Output Voltage Ripple (Note 6) Fop = 262 kHz, I_{out} = 60 mA (Note 7) @ C _{out} = 1.0 μ F @ C _{out} = 4.7 μ F	TAC	V _{PP}		150 25	- 60	mV
Digital Input High Level	4, 5, 6	V _{IH}	1.3	-	-	V
Digital Input Low level	4, 5, 6	V _{IL}	-	-	0.4	V
Output Power Efficiency @ $V_{bat} = 3.3 \text{ V}, V_{out} = 5.0 \text{ V}, I_{out} = 60 \text{ mA}, \text{ Fop} = 262 \text{ kHz}$ @ $V_{bat} = 3.9 \text{ V}, V_{out} = 5.0 \text{ V}, I_{out} = 160 \text{ mA}, \text{ Fop} = 650 \text{ kHz}$		Ρη		75 84		%
Thermal Shut Down Protection Hysteresis		T _{HSD}	-	160 20	-	°C

 Temperature range guaranteed by design, not production tested.
 Smaller footprint associated to lower working voltages (10 V or 6.3 V, size 0805 or 0602) can be used, but care must be observed to prevent DC bias effect on the capacitance final value. See capacitor manufacturer data sheets.

7. Ceramic X7R, ESR < 100 m Ω , SMD type capacitors are mandatory to achieve the l_{out} specifications. Depending upon the PCB layout, it might be necessary to use two 2.2 μ F/6.3 V/ceramic capacitors in parallel, yielding an improved V_{out} noise over the temperature range. On the other hand, care must be observed to take into account the DC bias impact on the capacitance value. See ceramic capacitor manufacturer data sheets.

8. Digital inputs undershoot < - 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{bat}.



TYPICAL CHARACTERISTICS

Figure 7. Typical Output Voltage Line Regulation

4.5

5.0

4.0

 V_{bat} (V)

EFFICIENCY (%)

EFFICIENCY (%)

2.5

3.0

3.5

Test conditions: V_{bat} = 3.6 V, V_{out} = 5 V, Load = 4*LW87S, $I_{LED} = 25 mA$

M4.00ms Ch1 /

880mV

2.00V

5.5

Figure 8. Output Voltage Startup from Scratch

5.5

Chl

1.00V

Ch2

TYPICAL CHARACTERISTICS







Figure 11. NCP5603 Output Current

Table 1. Ceramic Preferred Capacitors

Table 1. Ceramic Preferred (Capacitors		FSIGN
Manufacturer	Type/Series	Format	Value
TDK	C3216X5R1C475MT	1206	4.7 μF / 16 V
TDK	C2012X5R1C225MT	0805	2.2 μF / 16 V
TDK	C2012X5R1C105MT	0805	10 μF / 16 V
THIS DEVIC	ELEASENTATIVE REPRESENTATIVE REPRESENTATIVE	NENUCURORM CTORINFORM	







<u>Onsemí</u>,



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DESCRIPTION:	DFN10, 3X3 MM, 0.5 MM PITCH		PAGE 1 OF 1		
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