Enhancement Mode GaN Power Switch with Integrated Gate Clamp and Protection

650 V, 27 mΩ, PDSO-F9

Preliminary Document

NCP58934ABL

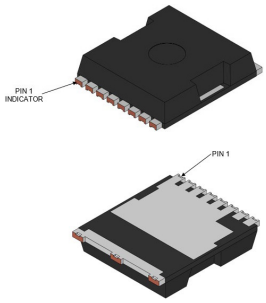
The NCP58934ABL integrates a 650 V enhancement-mode GaN power transistor with gate-drive and protection functions in a single package. An internal gate clamp, supported by LDO-based circuitry, regulates the gate drive voltage over a 10 V to 24 V input range to protect the GaN transistor from excessive gate stress while maintaining excellent switching performance. External resistors can be used to adjust turn-on and turn-off slew rates, allowing the designer to balance EMI performance and conversion efficiency. Integrated protection features include a Miller clamp to help prevent false turn-on during high dV/dt operation. The device is intended for compact, high-frequency, and high-power conversion applications.

Features

- 650 V 27 mΩ GaN HEMT
- Integrated Gate Clamp (External Driver Required)
- 800 V Transient Drain Voltage Capability
- 10 V to 24 V Gate Input Operating Range
- Adjustable Turn-on and Turn-off Slew Rates Using External Resistors
- Integrated Miller Clamp for dV/dT Immunity up to 100 V/ns
- High Frequency Switching Capability up to 2 MHz
- Supports Parallel Operation
- Zero Reverse Recovery Charge

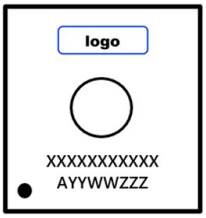
Typical Applications

- Industrial and Computing PSU
- Power Conversion
- High Power Density Power Supplies
- All Double-ended Topologies: Half-bridge, Full-bridge, LLC
- High-voltage Synchronous Buck Converter
- High-voltage Synchronous Boost Converter
- Two-switch Forward Converter
- Synchronous PFC Stage
- Totem Pole PFC



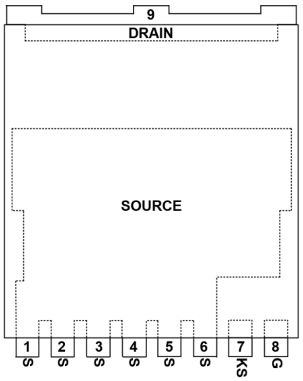
PDSO-F9 10.38x9.90x2.30, 1.20P
CASE 207AA

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZZ = Assembly Lot Code

PIN ASSIGNMENT



Transparent Top View

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.

June, 2026 − Rev. P1
Publication Order Number:
NCP58934ABL/D

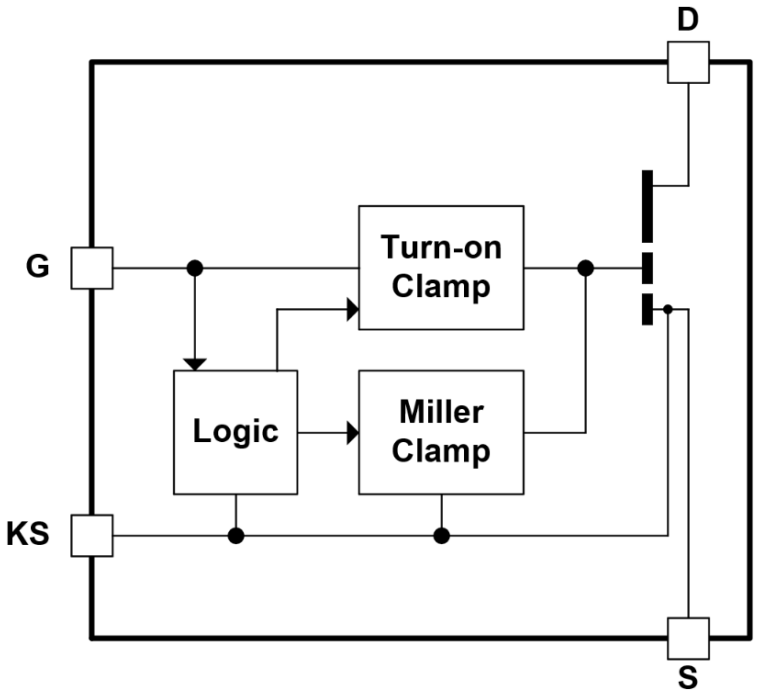


Figure 1. Block Diagram

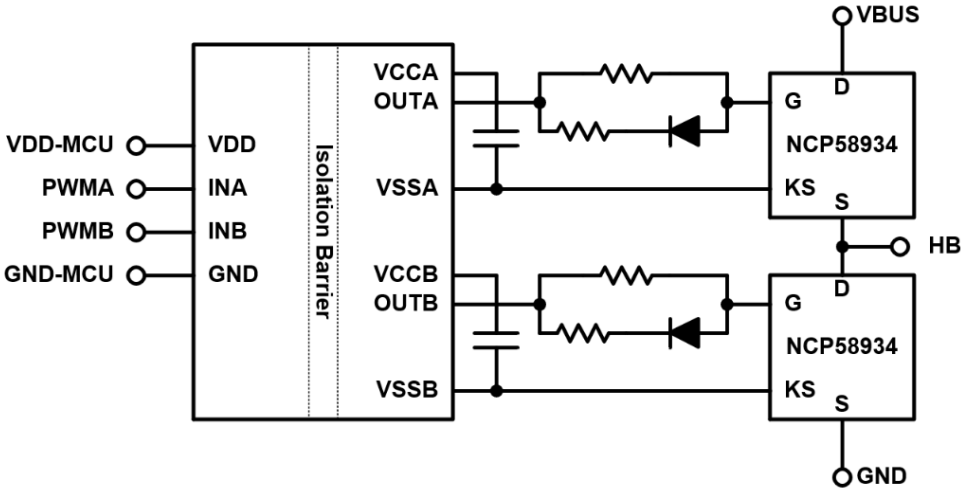


Figure 2. Half-bridge Application Schematic with Signal Isolator

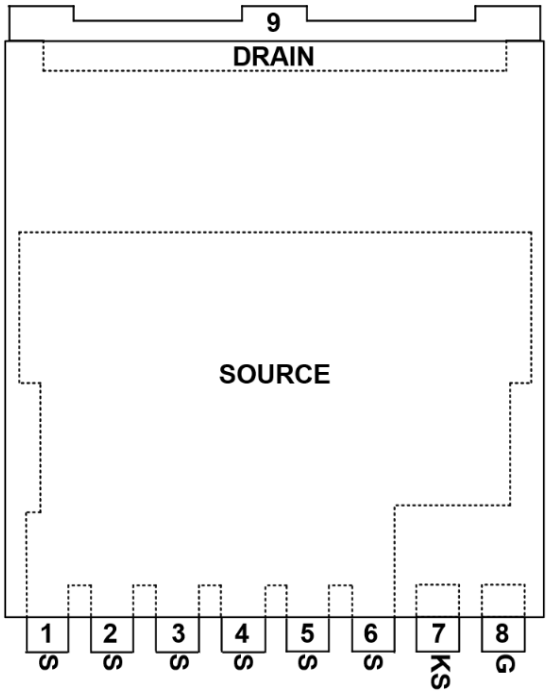


Figure 3. Pin Connections (Top Transparent View)

PIN DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1−6, Thermal Pad (Bot)	SOURCE	GaN power switch source	Power path connection for the GaN HEMT SOURCE.
7	KS	GaN power switch Kelvin source	Gate driver return path. This pin is internally connected to the source pad of the GaN HEMT.
8	G(GATE)	Gate driver input	Output of external gate driver should be connected to this pin. Internal clamping circuits will limit VGS of the GaN HEMT.
9	DRAIN	GaN power switch drain	Power path connection for the GaN HEMT DRAIN.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Continuous Gate Input Voltage, Referenced to SOURCE (Note 1)	V_{GS}	−0.3 to 26	V
Transient Gate Input Voltage, Referenced to SOURCE, t_{PULSE} < 100 ns	$V_{GS(PULSE)}$	−5 to 26	V
Continuous Drain-to-Source Voltage	V_{DSS}	650	V
Transient Drain-to-Source Voltage, Non-repetitive, t_{PULSE} < 200 μs	$V_{DS(TRAN)}$	800	V
Allowable Drain-to-Source Voltage Slew Rate, Device is OFF	dV_{DS}/dt	100	V/ns
Continuous Drain Current, T_C = 25 °C	I_{DS}	63	A
Continuous Drain Current, T_C = 100 °C	I_{DS}	40	A
Pulsed Drain Current, T_J = 25 °C, Pulse-width < 10 μs	$I_{DS(PULSE)}$	127	A
Pulsed Drain Current, T_J = 125 °C, Pulse-width < 10 μs	$I_{DS(PULSE)}$	64	A
Maximum Power Dissipation, T_{CASE} = 25 °C	P_{MAX}	347	W
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1	kV
Lead Temperature Soldering, Reflow (SMD Styles Only), Pb-Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referring to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods: ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114), ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115), Latch-up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Typical Value	Unit
Thermal Characteristics, TOLL			°C/W
Thermal Resistance, Junction-to-Case (Exposed Source Pad)	$R_{\theta JC(bot)}$	0.36	
Thermal Resistance, Junction-to-Air (Note 4)	$R_{\theta JA}$	56	

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 2 oz copper thickness, two layers FR4 PCB substrate.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Gate Input Voltage	V_{GS}	10	24	V
Turn-on Gate Pin Series Resistor	$R_{G(ON)}$	1	50	Ω
Turn-off Gate Pin Series Resistor	$R_{G(OFF)}$	1	10	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_G = 15 V, R_G = 10 Ω, for typical values T_A = 25 °C, V_{BUS} = 400 V ,unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
GaN TRANSISTOR SECTION						
SOURCE-DRAIN Third-Quadrant Voltage	I_{SD} = 18 A, V_{GS} = 0 V	V_{SD}		2.3		V
DRAIN Leakage Current	V_{DS} = 650 V, T_J = 25 °C, V_{GS} = 0 V	I_{DSS}		8	100	μA
	V_{DS} = 650 V, T_J = 150 °C, V_{GS} = 0 V	I_{DSS}		TBD		μA
DRAIN-SOURCE On-state Resistance	I_{DS} = 18 A, T_J = 25 °C	$R_{DS(ON)}$		27	35	mΩ
	I_{DS} = 18 A, T_J = 150 °C	$R_{DS(ON)}$		55		mΩ
Output Capacitance	V_{GS} = 0 V, V_{DS} = 400 V	C_{OSS}		176		pF
Output Capacitance, Energy Related (Note 5) (Note 6)	V_{GS} = 0 V, V_{DS} = 0 to 400 V	$C_{OSS(ER)}$		253		pF
Output Capacitance, Time Related (Note 6) (Note 7)	V_{GS} = 0 V, V_{DS} = 0 to 400 V	$C_{OSS(TR)}$		331		pF
Output Charge (Note 6)	V_{GS} = 0 V, V_{DS} = 0 to 400 V	Q_{OSS}		132		nC
Energy Stored in Output Capacitance (Note 6)	V_{GS} = 0 V, V_{DS} = 0 to 400 V	E_{OSS}		20.2		μJ
Reverse Recovery Charge (Note 6)		Q_{RR}		0		nC
GATE INPUT SECTION						
Gate Input ON Minimum		$V_{GS(ON)}$			9	V
Gate Input OFF Maximum		$V_{GS(OFF)}$	0.5			V
Gate Input Quiescent Current	V_G = 15 V, V_{DS} = 0 V	I_{GQ}		1.9	5.2	mA
TIMING CHARACTERISTICS SECTION						
Minimum Input On Time	R_G = 1 Ω, Minimum input on time to guarantee datasheet timing specifications	$t_{ON(MIN)}$	80			ns
Minimum Input Off Time	R_G = 1 Ω, Minimum input off time to guarantee datasheet timing specifications	$t_{OFF(MIN)}$	40			ns
Input to Switch Turn-on Propagation Delay (Note 8)	R_G = 1 Ω	$t_{PD(ON)}$		23		ns
Input to Switch Turn-off Propagation Delay (Note 8)	R_G = 1 Ω	$t_{PD(OFF)}$		8		ns
Rise Time (Note 8)	R_G = 10 Ω, I_{DS} = 18 A, V_{BUS} = 400 V	t_R		6.6		ns
Fall Time (Note 8)	R_G = 1 Ω, I_{DS} = 18 A, V_{BUS} = 400 V	t_F		13		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. $C_{OSS(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.
6. The parameter is not tested in the production; value is guaranteed by the design.
7. $C_{OSS(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.
8. Refer to Timing Characterization Reference section.

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Switching Test Circuit

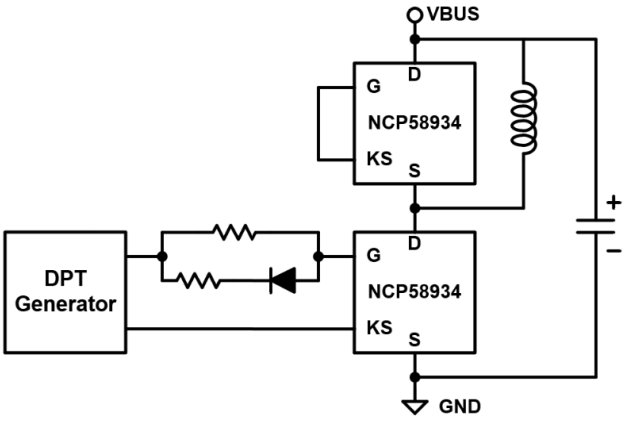


Figure 4. Half-bride Stage Arranged as Double-pulse Tester (DPT) Circuit

A typical approach to how to determine timing parameters of switching devices is to test them in double-pulse tester or use double-pulse testing technique. The half-bridge is a basic switching structure adopted in wide range of converter topologies, that is easy to convert into double-pulse tester. Figure 4 shows a principle schematic diagram of circuit that is used to measure switching parameters. The low-side device NCP58934 is the part that actively switches. When the device is turned on, an inductor current is built to a certain level. The inductor current for this switching interval is almost the same as Drain current and its level is basically related to $+V_{BUS}$ voltage, inductance, and turn-on pulse width. When the low-side device is turned off, inductor current cannot be interrupted, so the high-side NCP58934 naturally turns on, operating in third quadrant and its function is the same as freewheeling diode which enables inductor current re-circulation. Operation in the third quadrant should be well considered to avoid generating excessive losses and thus device overheating. Dedicated sequence of pulses creates operating conditions that are sufficient for generating switching waveforms and measuring required parameters. The specific timing measurement is shown in Figure 5.

Timing Characterization Reference

The timing of the turn-on transition is composed of two parameters: input-to-switch turn-on propagation delay and switch-V_{DS}-voltage falling time. The first component is the propagation delay of the driver from when the input goes high to when the GaN HEMT starts turning-on while its V_{DS} voltage drops to 90% of $+V_{BUS}$. The rise time, t_r, is the time it takes for switch-V_{DS} voltage to slew between 90 percent and 10 percent of $+V_{BUS}$ voltage. Turn-on impedance of the gate driver has significant impact on turn-on slew rate while the turn-on propagation delay influence is minor. The timing definition of the turn-off transition also has two components: input-to-switch turn-off propagation delay and fall time, t_F. Reference levels are the same, however, the difference lays in opposite order, as depicted in Figure 5.

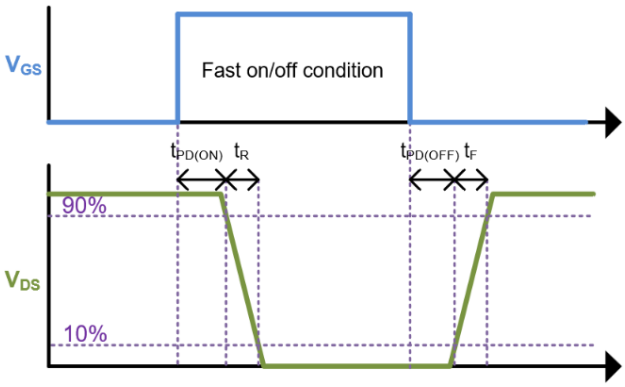


Figure 5. Measurement Reference for Determining Timing

High Speed Measurement Practice

In general, the GaN HEMTs have a significantly faster switching performance than silicon and silicon-carbide MOSFETs. It's essential to use proper measuring techniques to evade the parasitic elements introduced by test equipment, that may distort device parameters and lead to inaccurate measurement results. A long probing ground wire inserts undesired inductance into the probe measurement path, which results in overshoot and ringing linked to the rising and falling edges of the measured signals. Minimizing the length of the ground loop is important especially for signals which have very high dv/dt level. At least, it's recommended to use a so called "pigtail" that helps to reduce probe grounding inductance and thus provides more accurate measurement. Further, it's advised to use an oscilloscope and a probe with bandwidth more than 350 MHz, while edge slope time distortion of approximate 1.5 ns should be considered.

Maximum Package Power Dissipation

The power dissipation level is the maximum allowed power dissipation for package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

FUNCTIONAL DESCRIPTION

Overview

The NCP58934 is a 650 V power IC that integrates a high-performance enhancement-mode GaN FET with advanced control and protection features in a single device. It incorporates a gate clamp that supports a wide gate-input voltage range from 10 V to 24 V. An accurate LDO-based circuit tightly regulates the gate voltage to protect the GaN FET from excessive voltage stress while maintaining switching performance. External gate resistors can be used to adjust both turn-on and turn-off slew rates, allowing optimization of EMI and efficiency. The device also includes a Miller clamp with strong gate pull-down capability to help prevent false turn-on during high dV/dt switching events. These functions are implemented without requiring a continuous external supply for the internal bias circuitry. With the GaN FET and protection features integrated in a TOLL package, the NCP58934 enables simple power-stage implementation with low external component count for high-frequency and high-power applications. It is important to remember that this device still requires an external gate driver to function correctly.

Input Via G(GATE) Pin

The NCP58934 includes a G input pin for control of the integrated GaN FET. When the G input voltage rises above the input-high threshold of $V_{G(ON)}$, the device propagates the input signal to the GaN FET gate, turning the device on and establishing a low-resistance conduction path from Drain to Source with a typical on-state resistance of 27 mΩ. When the G input voltage falls below the input-low threshold of $V_{G(OFF)}$, the device blocks propagation of the input signal and pulls the GaN FET gate down to Source, turning the device off and interrupting the Drain-to-Source current path. Figure 5 shows the relationship between the input signal and the output response. The NCP58934 also includes a 10 ns typical turn-on deglitch filter on the G input to reject unwanted pulses.

The NCP58934 supports a wide G input voltage range from 10 V to 24 V for design flexibility. Internal circuitry is powered directly from the G input, eliminating the need for a continuous external supply for the internal bias circuitry.

Turn-on Slew-rate (dv/dt) Adjustment

The NCP58934 allows independent adjustment of the GaN FET turn-on and turn-off slew rates. As shown in Figure 6, this is implemented using external gate resistors and a diode connected between the driver output and the G pin. This network independently sets the current available to charge and discharge the GaN gate, enabling separate control of the turn-on and turn-off transitions.

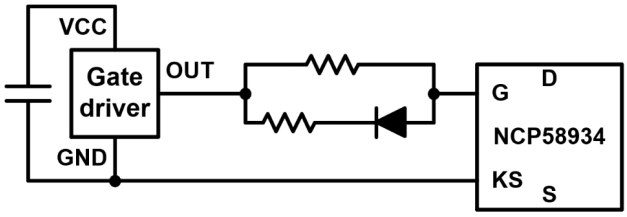


Figure 6. Passive Network for Adjustable Turn-on and Turn-off Slew Rate Control

Drain-to-Source Voltage and its Maximum Recommended Levels

The NCP58934 is designed with sufficient margin to handle both transient and continuous voltage stresses common in half-bridge topologies such as buck, boost, LLC, and totem-pole PFC. Figure 7 illustrates recommended limits. For *non-repetitive* events − including line surges, lightning strikes, startup, short-circuit, and load transients − the device supports a transient drain-to-source voltage rating of $V_{DS(TRAN)}$ = 800 V for durations under 200 μs, ensuring robustness without derating. For *repetitive* conditions, such as normal switching and steady-state operation after turn-off, overshoot caused by parasitic inductances must be clamped to $V_{DS(MAX)}$ = 650 V. After the overshoot dissipates, the voltage settles at $V_{PLATEAU}$, which is recommended not to exceed 80% of $V_{DS(MAX)}$, or ≤520 V, meaning the DC bus voltage (V_{BUS}) should be limited to 520 V.

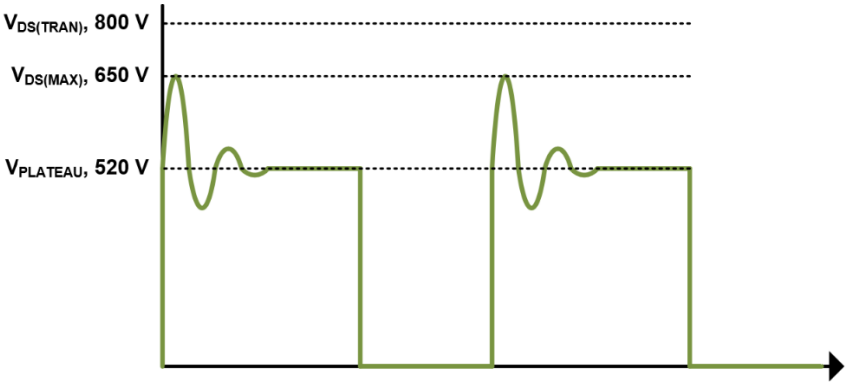


Figure 7. Drain-to-Source Voltage Definition

ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
ENGNCP58934ABLTXG	PDSO-F9 10.38x9.90x2.30, 1.20P	1200 / Tape & Reel

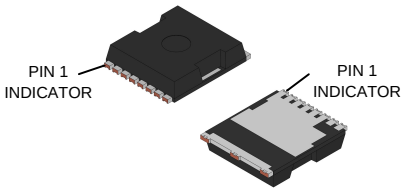
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

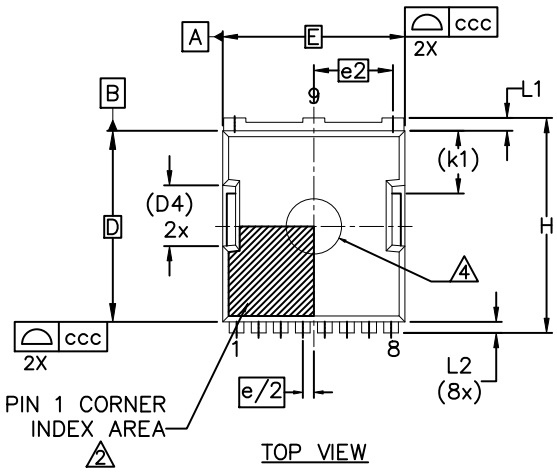
REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	5/11/2026
P1	Update − Package and Shipping information, Marking Diagram.	6/25/2026

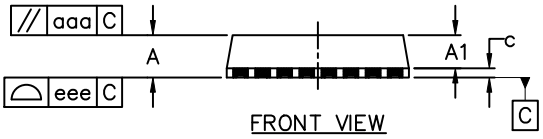
PDSO-F9 10.38x9.90x2.30, 1.20P
CASE 207AA
ISSUE O

DATE 25 FEB 2026

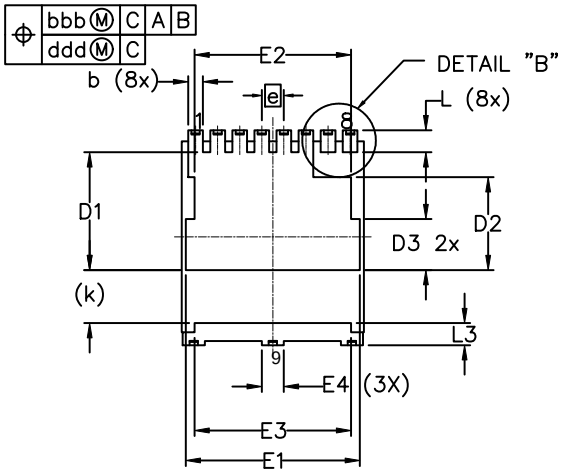




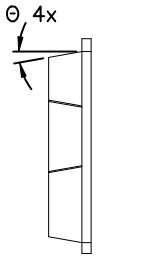
TOP VIEW



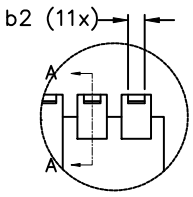
FRONT VIEW



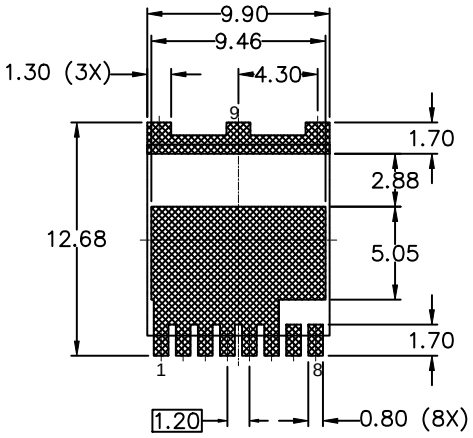
BOTTOM VIEW



SIDE VIEW

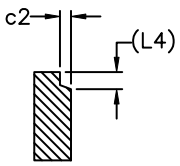


DETAIL "B"
SCALE: 2X



LAND PATTERN
RECOMMENDATION

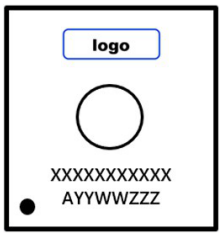
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



SECTION "A−A"
SCALE: 4X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.15	2.30	2.45
A1	1.65	1.80	1.95
b	0.70	0.80	0.90
b2	0.31	0.43	0.55
c	0.40	0.50	0.60
c2	0.10	–	–
D	10.38 BSC		
D1	6.20	6.40	6.60
D2	4.85	5.05	5.25
D3	2.57	2.77	3.97
D4	3.30 REF		
E	9.90 BSC		
E1	9.26	9.46	9.66
E2	8.30	8.50	8.70
E3	8.30	8.50	8.70
E4	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e2	4.30 BSC		
H	11.48	11.68	11.88
L	1.00	1.20	1.40
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	0.23 REF		
k	2.88 REF		
k1	3.41 REF		
Θ	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.20		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH AND BURR.
4. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.

DOCUMENT NUMBER:	**98AON70698H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**PDSO-F9 10.38x9.90x2.30, 1.20P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales