# NCP706A

# 1 A, 1% Precision Very Low Dropout Voltage Regulator with Enable and Active Discharge

ON Semiconductor®

www.onsemi.com

The NCP706A is a Very Low Dropout Regulator which provides up to 1 A of load current and maintains excellent output voltage accuracy of 1% including line, load and temperature variations. The operating input voltage range from 2.4 V up to 5.5 V makes this device suitable for Li−ion battery powered products as well as post−regulation applications. The product is available in 3.0 V fixed output voltage option. NCP706A is fully protected against overheating and output short circuit.

Very small 8−pin XDFN8 1.6 x 1.2, 04P package makes the device especially suitable for space constrained portable applications such as tablets and smartphones. Parts feature active output discharge function.

### Features

- Operating Input Voltage Range: 2.4 V to 5.5 V
- Fixed Output Voltage Option: 3.0 V
  Other Output Voltage Options Available on Request.
- Low Quiescent Current of Typ. 200 μA
- Very Low Dropout: 155 mV Max. at $I_{OUT}$ = 1 A
- ±1% Accuracy Over Load/Line/Temperature
- High PSRR: 60 dB at 1 kHz
- Internal Soft−Start to Limit the Inrush Current
- Thermal Shutdown and Current Limit Protections
- Stable with a 1.0 μF Ceramic Output Capacitor
- Available in XDFN8 1.6 x 1.2, 04P 8−pin Package
- Active Output Discharge
- These are Pb−Free Devices

### Typical Applications

- Tablets, Smartphones,
- Wireless Handsets, Portable Media Players
- Portable Medical Equipment
- Other Battery Powered Applications

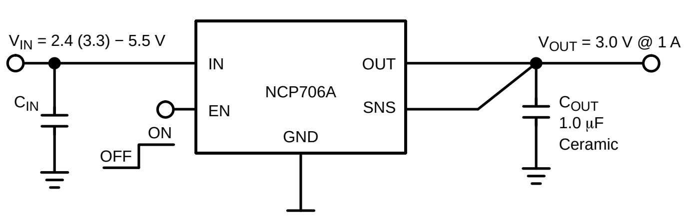
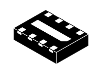
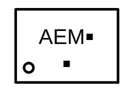



**Figure 1. Typical Application Schematic**



XDFN8
CASE 711AS

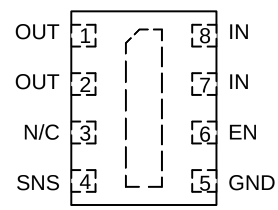
**MARKING DIAGRAM**



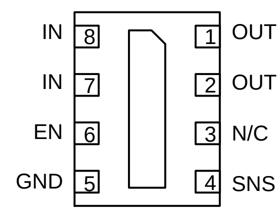

AE = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**PIN CONNECTION**




(Top View)




(Bottom View)

**ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 8 of this data sheet.

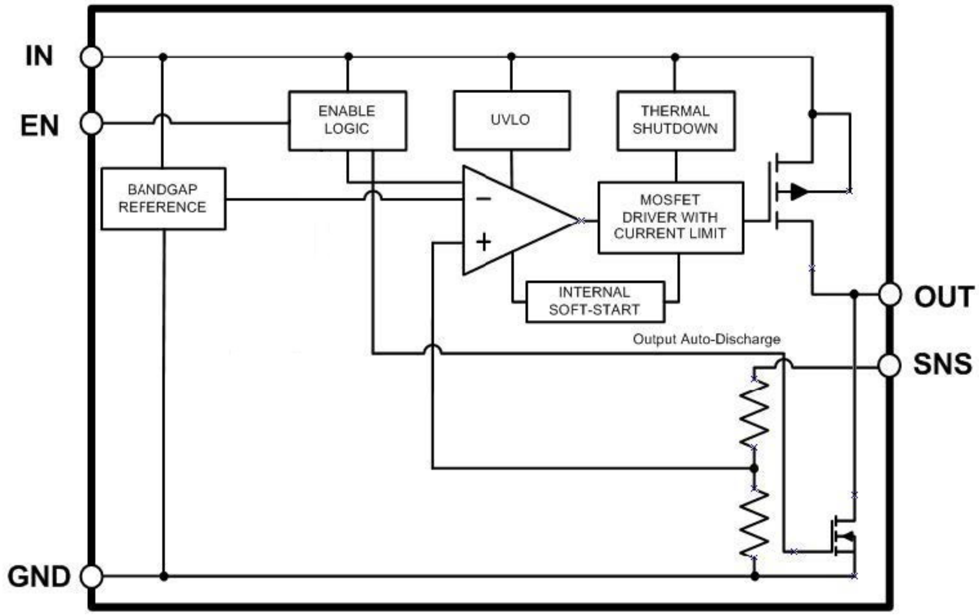



**Figure 2. Simplified Internal Schematic Block Diagram**

## PIN FUNCTION DESCRIPTION

| Pin No. XDFN8 | Pin Name | Description |
|---|---|---|
| 1 | OUT | Regulated output voltage. A minimum 1.0 μF ceramic capacitor is needed from this pin to ground to assure stability. |
| 2 | OUT | |
| 3 | N/C | Not connected. This pin can be tied to ground to improve thermal dissipation. |
| 4 | SNS | Remote sense connection. This pin should be connected to the output voltage rail. |
| 5 | GND | Power supply ground. |
| 6 | EN | Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. |
| 7 | IN | Input pin. A small capacitor is needed from this pin to ground to assure stability. |
| 8 | IN | |
| − | Exposed Pad | This pad enhances thermal performance and is electrically connected to GND. It is recommended that the exposed pad is connected to the ground plane on the board or otherwise left open. |

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (Note 1) | $V_{IN}$ | −0.3 V to 6 V | V |
| Output Voltage | $V_{OUT}$ | −0.3 V to $V_{IN}$ + 0.3 V | V |
| Enable Input | $V_{EN}$ | −0.3 V to $V_{IN}$ + 0.3 V | V |
| Output Short Circuit Duration | $t_{SC}$ | Indefinite | s |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 150 | °C |
| Storage Temperature | $T_{STG}$ | −55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2000 | V |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latch−up Current Maximum Rating tested per JEDEC standard: JESD78

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, XDFN8 1.6x1.2, 04P<br>Thermal Resistance, Junction−to−Air | $R_{\theta JA}$ | 160 | °C/W |

### ELECTRICAL CHARACTERISTICS − VOLTAGE VERSION 3.0 V

−40°C ≤ $T_J$ ≤ 125°C; $V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 3.3 V, whichever is greater; $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, $V_{EN}$ = 0.9 V, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 3)

| Parameter | Test Conditions | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Input Voltage | | | $V_{IN}$ | 2.4 | | 5.5 | V |
| Undervoltage lock−out | $V_{IN}$ rising, $I_{OUT}$ = 0 | | UVLO | 1.2 | 1.6 | 1.9 | V |
| Output Voltage Accuracy | $V_{OUT}$ + 0.3 V ≤ $V_{IN}$ ≤ 4.5 V, $I_{OUT}$ = 0 – 1 A | | $V_{OUT}$ | 2.97 | 3.0 | 3.03 | V |
| Line Regulation | $V_{OUT}$ + 0.3 V ≤ $V_{IN}$ ≤ 4.5 V, $I_{OUT}$ = 10 mA | | $Reg_{LINE}$ | | 2 | | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 1 A, $V_{IN}$ = 3.3 V | | $Reg_{LOAD}$ | | 2 | | mV |
| Load Transient | $I_{OUT}$ = 10 mA to 1 A in 10 μs, $V_{IN}$ = 3.5 V<br>$C_{OUT}$ = 10 μF | | $Tran_{LOAD}$ | | ±120 | | mV |
| Dropout voltage (Note 4) | $I_{OUT}$ = 1 A, $V_{OUT(nom)}$ = 3.0 V | | $V_{DO}$ | | 155 | 230 | mV |
| Output Current Limit | $V_{OUT}$ = 90% $V_{OUT(nom)}$ | | $I_{CL}$ | 1.1 | | | A |
| Quiescent current | $I_{OUT}$ = 0 mA | | $I_Q$ | | 170 | 230 | μA |
| Ground current | $I_{OUT}$ = 1 A | | $I_{GND}$ | | 200 | | μA |
| Shutdown current | $V_{EN}$ ≤ 0 V, $V_{IN}$ = 2.0 to 5.5 V | | | | 0.1 | 1 | μA |
| EN Pin High Threshold<br>EN Pin Low Threshold | $V_{EN}$ Voltage increasing<br>$V_{EN}$ Voltage decreasing | | $V_{EN\_HI}$<br>$V_{EN\_LO}$ | 0.9 | | <br>0.4 | V |
| EN Pin Input Current | $V_{EN}$ = 5.5 V | | $I_{EN}$ | | 100 | 500 | nA |
| Turn−on Time | $C_{OUT}$ = 4.7 μF, from assertion EN pin to 98% $V_{out(nom)}$ | | $t_{ON}$ | | 150 | | μs |
| Power Supply Rejection Ratio | $V_{IN}$ = 3.5 V + 200 mVpp modulation, $V_{OUT}$ = 3.0 V<br>$I_{OUT}$ = 0.5 A, $C_{OUT}$ = 4.7 μF | f = 100 Hz<br>f = 1 kHz<br>f = 10 kHz | PSRR | | 65<br>58<br>52 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 3.0 V, $V_{IN}$ = 4.0 V, $I_{OUT}$ = 0.5 A<br>f = 100 Hz to 100 kHz | | $V_{NOISE}$ | | 300 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature | Temperature increasing from $T_J$ = +25°C | | $T_{SD}$ | | 160 | | °C |
| Thermal Shutdown Hysteresis | Temperature falling from $T_{SD}$ | | $T_{SDH}$ | | 20 | | °C |
| Active Output Discharge | $V_{EN}$ ≤ 0.4 V, $V_{IN}$ = 4.5 V | | $R_{DIS}$ | | 60 | | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
4. Characterized when $V_{OUT}$ falls 90 mV below the regulated voltage at $V_{IN}$ = 3.3 V, $I_{OUT}$ = 10 mA.

## TYPICAL CHARACTERISTICS

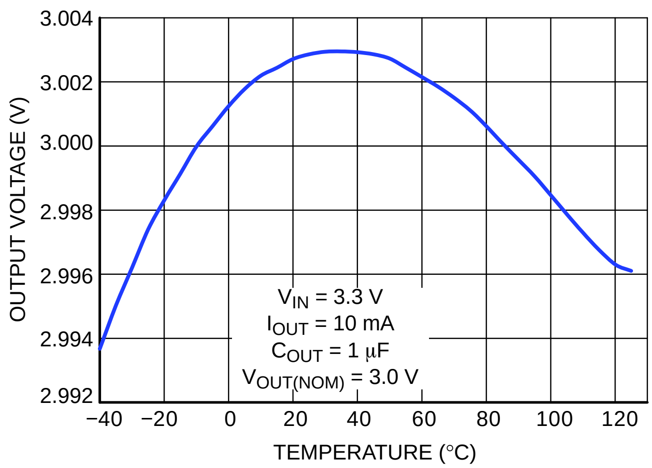



Figure 3. Output Voltage vs. Temperature

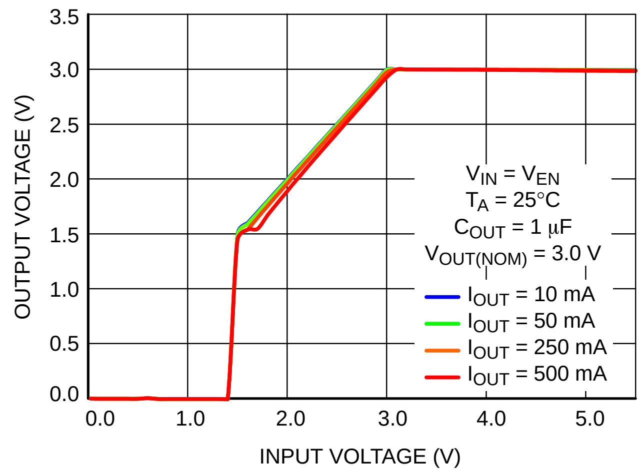



Figure 4. Output Voltage vs. Input Voltage

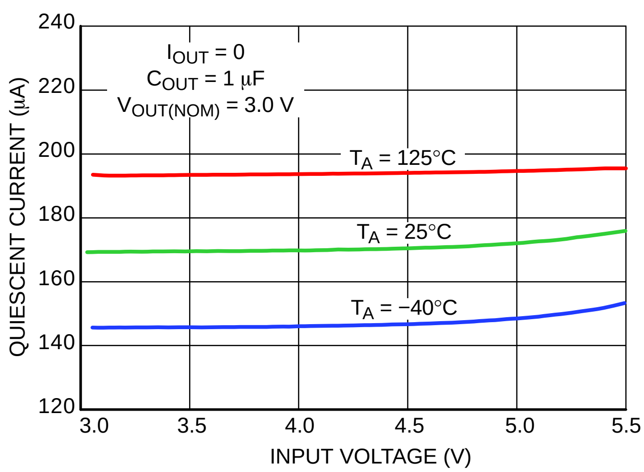



Figure 5. Quiescent Current vs. Input Voltage

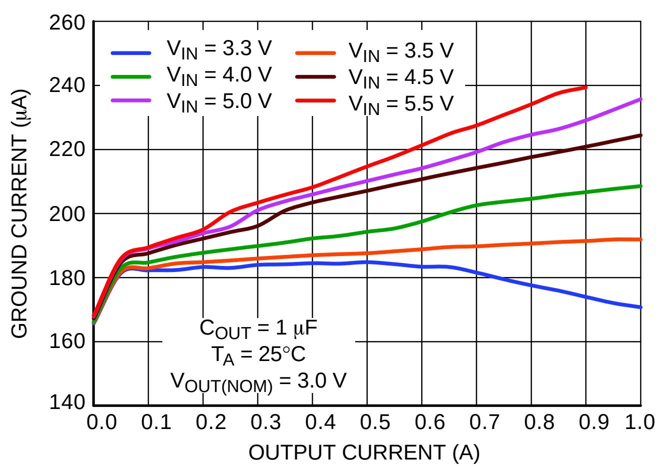



Figure 6. Ground Current vs. Output Current

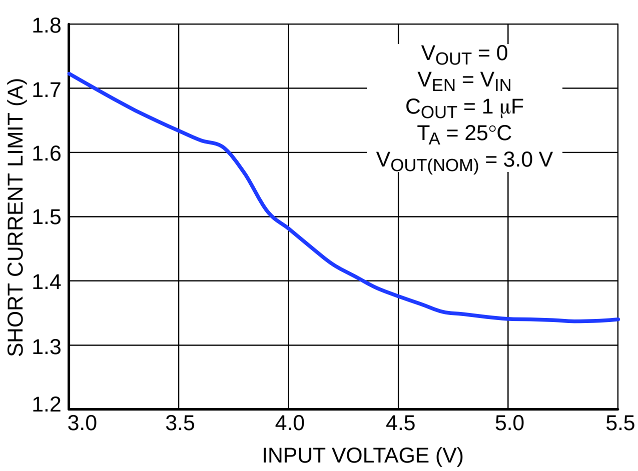



Figure 7. Short Current Limitation vs. Input Voltage

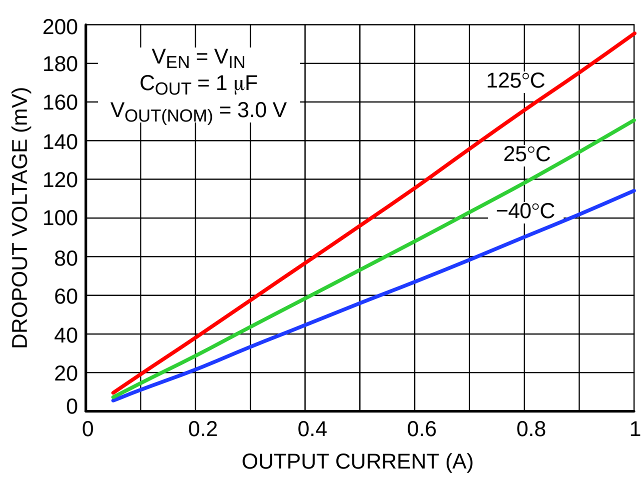



Figure 8. Dropout Voltage vs. Output Current

## TYPICAL CHARACTERISTICS

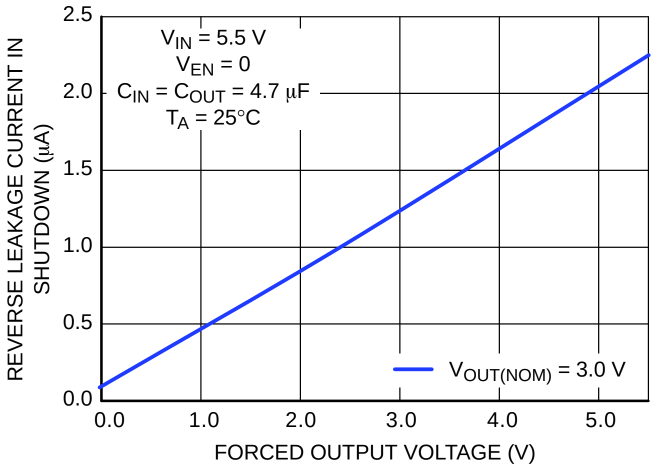



**Figure 9. Reverse Leakage Current in Shutdown**

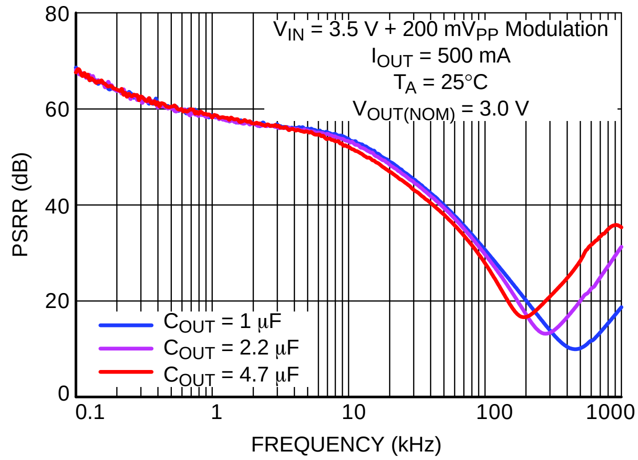



**Figure 10. PSRR vs. Frequency & Output Capacitor**

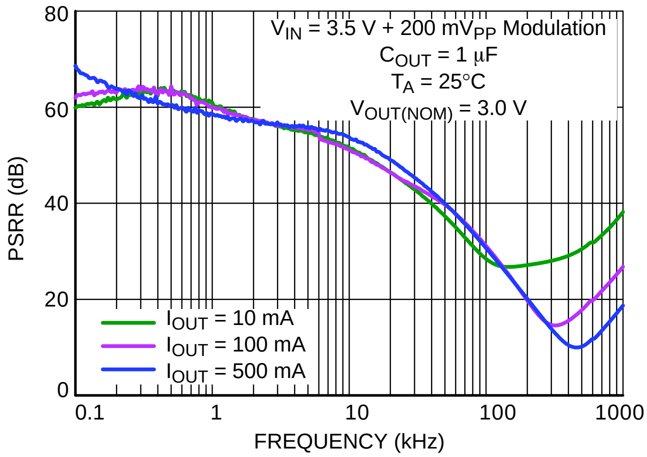



**Figure 11. PSRR vs. Frequency & Output Current**

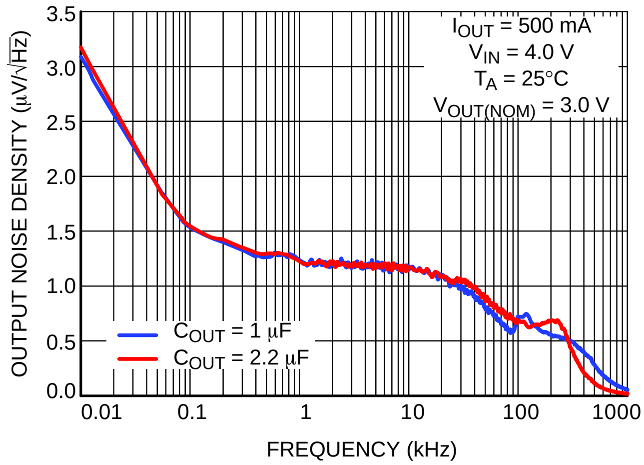



**Figure 12. Output Noise Density vs. Frequency**

## TYPICAL CHARACTERISTICS

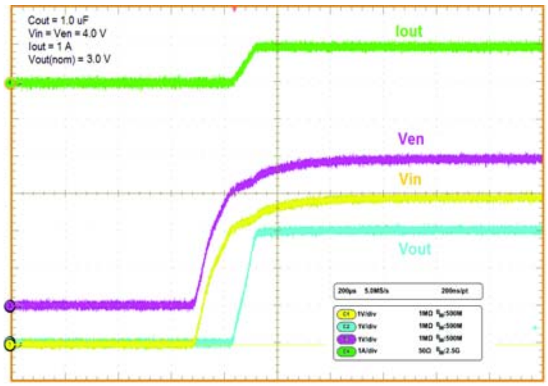



**Figure 13. Turn−on by Coupled Input and Enable Pins**

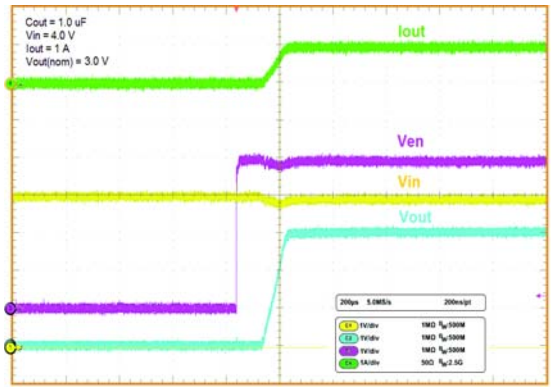



**Figure 14. Turn−on by Enable Signal**

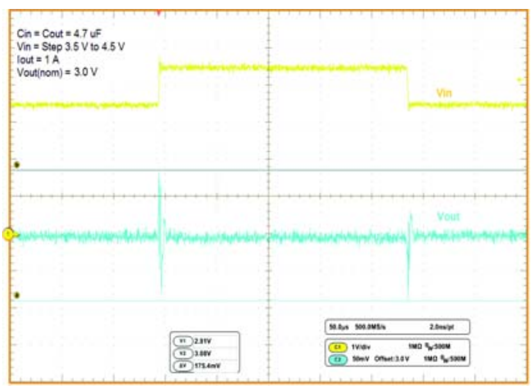



**Figure 15. Line Transient Response**

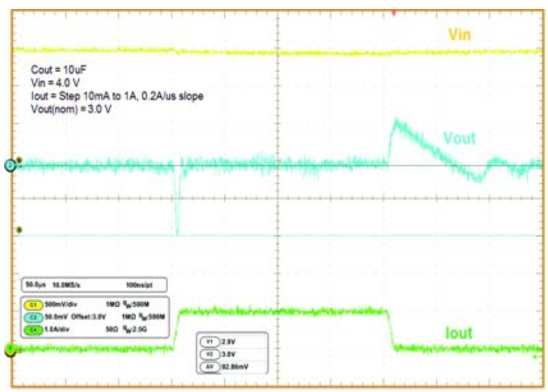



**Figure 16. Load Transient Response**

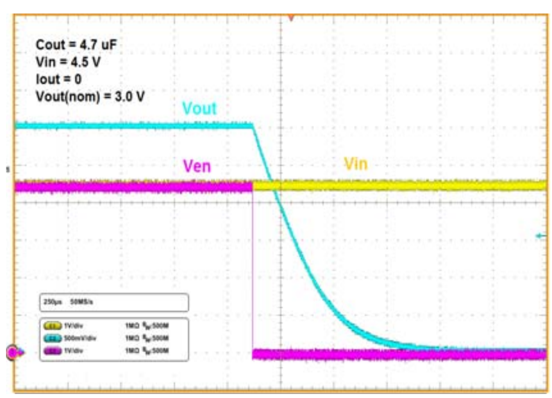



**Figure 17. Turn−off by Enable Signal**

## APPLICATIONS INFORMATION

### Input Decoupling (Cin)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected as close as possible to the pins of NCP706A device. Higher values and lower ESR will improve the overall line transient response.

### Output Decoupling (Cout)

The minimum decoupling value for NCP706AMX300TAG device is 1 μF. The regulator accepts ceramic chip capacitors MLCC. If a tantalum capacitor is used, and its ESR is large, the loop oscillation may result. Larger values improve noise rejection and PSRR.

### Enable Operation

The enable pin EN will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $V_{IN}$.

### Hints

Please be sure the $V_{in}$ and GND lines are sufficiently wide. If their impedance is high, noise pickup or unstable operation may result.

Set external components, especially the output capacitor, as close as possible to the circuit.

The sense pin SNS trace is recommended to be kept as far from noisy power traces as possible and as close to load as possible.

### Thermal

As power across the NCP706A increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature rise for the part. This is stating that when the NCP706A has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation.

The power dissipation across the device can be roughly represented by the equation:

$$P_D = \left(V_{IN} - V_{OUT}\right) * I_{OUT} \ [W] \qquad \text{(eq. 1)}$$

The maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature differential between the junction and ambient, PCB orientation and the rate of air flow.

The maximum allowable power dissipation can be calculated using the following equation:

$$P_{MAX} = \left(T_J - T_A\right)/\theta_{JA} \ [W] \qquad \text{(eq. 2)}$$

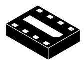
Where $(\mathbf{T_J - T_A})$ is the temperature differential between the junction and the surrounding environment and $\boldsymbol{\theta_{JA}}$ is the thermal resistance from the junction to the ambient.

Connecting the exposed pad and non connected pin 3 to a large ground pad or plane helps to conduct away heat and improves thermal relief.

### ORDERING INFORMATION

| Device | Nominal Ooutput Voltage | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCP706AMX300TAG | 3.0 V | AE | XDFN8 (Pb−Free) | 3000 / Tape & Reel |

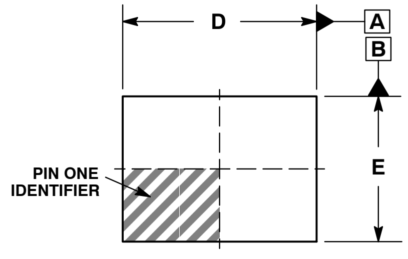
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



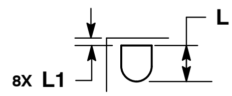
SCALE 4:1

**XDFN8 1.6x1.2, 0.4P**
CASE 711AS
ISSUE D

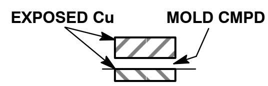
DATE 08 DEC 2015



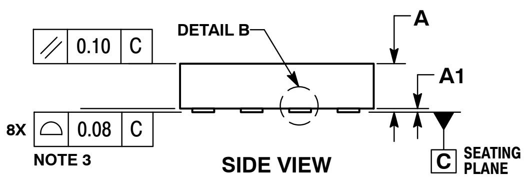

**TOP VIEW**



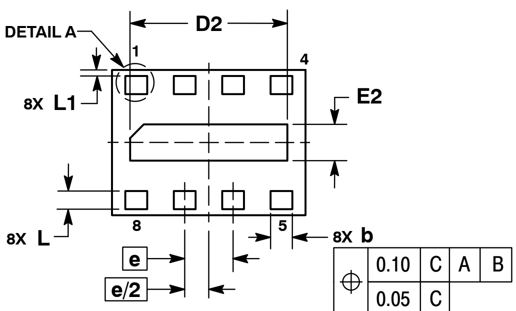

**DETAIL A**
OPTIONAL
CONSTRUCTION




**DETAIL B**
OPTIONAL
CONSTRUCTION




**SIDE VIEW**

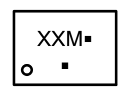



**BOTTOM VIEW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS MIN | NOM | MAX |
|---|---|---|---|
| A | 0.300 | 0.375 | 0.450 |
| A1 | 0.000 | 0.025 | 0.050 |
| b | 0.130 | 0.180 | 0.230 |
| D | 1.500 | 1.600 | 1.700 |
| D2 | 1.200 | 1.300 | 1.400 |
| E | 1.100 | 1.200 | 1.300 |
| E2 | 0.200 | 0.300 | 0.400 |
| e | | 0.40 BSC | |
| L | 0.150 | 0.200 | 0.250 |
| L1 | 0.000 | 0.050 | 0.100 |

**GENERIC MARKING DIAGRAM***

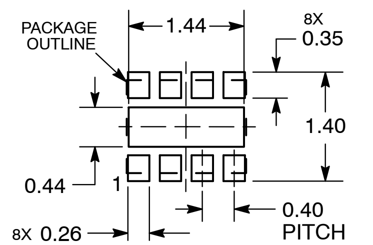



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

**RECOMMENDED MOUNTING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98AON87768E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | XDFN8, 1.6X1.2, 0.4P | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

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