Precision Operational Amplifier, Low Offset, 10 MHz, Rail-to-Rail Input/Output

NCS20166, NCV20166

The NCS20166 features rail−to−rail input and output, and 10 MHz bandwidth. This low quiescent current, low noise amplifier is trimmed to provide a low initial input offset voltage. This op amp operates over a supply range from 3.0 V to 5.5 V. All versions are specified for operation from −40°C to +125°C.

Features

- Gain Bandwidth: 10 MHz Typical
- Offset Voltage: 550 μV Max (V_S = 5 V)
- Supply Voltage: 3 V to 5.5 V
- Quiescent Current: 1.55 mA Max
- Voltage Noise Density: 10 nV/$\sqrt{Hz}$ Typical
- Rail−to−Rail Input and Output
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Current Sensing
- Current Sensing in Motor Control Circuits
- Current Monitor for Power Supplies
- Battery Powered Instrumentation
- Transducer or Sensor Interface
- Medical Instrumentation

End Products

- Industrial
- Power Supplies
- Computers and Servers
- Automotive
- Medical Instrumentation

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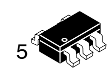
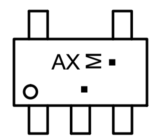


SC−74A (SOT23−5)
CASE 318BQ

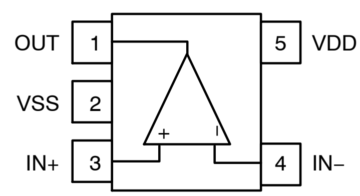
MARKING DIAGRAM



AX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



SC−74A (SOT23−5)
SN2 Pinout

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

April, 2020 − Rev. 0
Publication Order Number:
NCS20166/D

ORDERING INFORMATION

Device	Configuration	Marking	Package	Shipping†
INDUSTRIAL AND AUTOMOTIVE				
NCS20166SN2T1G	Single	AX	SC−74A (SOT23−5)	3000 / Tape and Reel
NCV20166SN2T1G*		AX		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV prefix for automotive and other applications requiring unique site and control change requirements; AEC−Q100 qualified and PPAP capable
** Contact local sales office for more information

Table 1. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage (V_{DD} − V_{SS})	6	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	V_{SS} – 0.3 to V_{DD} + 0.3	V
Differential Input Voltage (Note 1)	±V_s	V
Input Current (Note 1)	±10	mA
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature	–40 to +125	°C
Storage Temperature	–65 to +150	°C
Junction Temperature	+150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	+260	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	2000	V
Charged Device Model (CDM)	1000	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
Moisture Sensitivity Level (MSL)	1	
Continuous Total Power Dissipation	200	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Input terminals are diode clamped to the power supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
2. Short−circuit to ground up to T_A = 125°C.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017 (AEC−Q100−002)
   ESD Charged Device Model tested per JEDEC standard JS−002−2014 (AEC−Q100−011)
4. Latch−up Current tested per JEDEC standard JESD78E (AEC−Q100−004)

Table 2. THERMAL INFORMATION (Note 5)

Parameter	Symbol	Package	Value	Unit
Junction−to−Ambient	θ_{JA}	SC−74A (SOT23−5)	198	°C/W

5. As mounted on an 80x80x1.5 mm FR4 PCB with 600 mm^2 and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

Table 3. OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Supply Voltage (V_{DD} − V_{SS})	V_S	3	5.5	V
Specified Operating Temperature Range	T_A	−40	125	°C
Input Common Mode Voltage Range	V_{ICMR}	V_{SS}	V_{DD}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS V_S = 3.0 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ, C_L = 15 pF connected to mid supply, V_{CM} = V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_S = 3 to 5.5 V, T_A = 25°C		±50	±550	μV
		V_S = 3 to 5.5 V		±100	**±1050**	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			**±1**	**±5**	μV/°C
Input Bias Current (Note 6)	I_{IB}			±1		pA
					±600	pA
Input Offset Current (Note 6)	I_{OS}			±1		pA
					±600	pA
Common Mode Rejection Ratio @ Vs = 5.5 V	CMRR	V_{CM} = V_{SS} to V_{DD}	**77**	92		dB
Common Mode Rejection Ratio @ Vs = 3 V			**70**	87		
Input Capacitance	C_{IN}	Differential		6		pF
		Common Mode		12		
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	V_O = V_{SS} + 0.05 V to V_{DD} – 0.05 V		120		dB
Open Loop Output Impedance	Z_{OUT_OL}			See Figure 29		Ω
Output Voltage High, Referenced to Rail (Note 6)	V_{OH}	I_L = 1 mA			**30**	mV
		I_L = 10 mA			**120**	
Output Voltage Low, Referenced to Rail (Note 6)	V_{OL}	I_L = 1 mA			**30**	mV
		I_L = 10 mA			**120**	
Short Circuit Current	I_{SC}	Sinking Current		25		mA
		Sourcing Current		25		
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBWP			10		MHz
Gain Margin	A_M	V_S = 5.5 V, Load = 10 kΩ || 100 pF		10		dB
Phase Margin	ϕ_M	V_S = 5.5 V, Load = 10 kΩ || 100 pF		50		°
Slew Rate	SR	1 V Step, Rising Edge, V_S = 5.5 V A_v = 1, Load = 10 kΩ || 100 pF		6		V/μs
		1 V Step, Falling Edge, V_S = 5.5 V A_v = 1, Load = 10 kΩ || 100 pF		4		
		1 V Step, Rising Edge, V_S = 5.5 V A_v = 1, Load = 10 kΩ || 60 pF		6		
		1 V Step, Falling Edge, V_S = 5.5 V A_v = 1, Load = 10 kΩ || 60 pF		4		
Settling Time	t_S	0.1% V_o = 2 V step, AV = –1		0.5		μs
		0.01% V_o = 2 V step, AV = –1		1		μs
Turn On Time	t_{ON}			3.5		μs
Overload Recovery Time	t_{OR}	V_{IN} ≤ 100 mV Step, A_V = –100		2		μs
Capacitive Load Drive	C_L			See Figure 30		pF

Table 4. ELECTRICAL CHARACTERISTICS V_S = 3.0 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ, C_L = 15 pF connected to mid supply, V_{CM} = V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	V_S = 5.5 V, f_{IN} = 1 kHz, AV = 1, V_{out} = 1 Vrms		0.001		%
Voltage Noise Density	e_N	V_S = 5.5 V, f_{IN} = 1 kHz		10		nV/√Hz
Voltage Noise, Peak–to–Peak	e_{PP}	V_S = 5.5 V, f_{IN} = 0.1 Hz to 10 Hz		3		μV_{PP}
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 5.5 V	**73**	89		dB
Quiescent Current	I_Q	No load		1	1.25	mA
					1.55	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

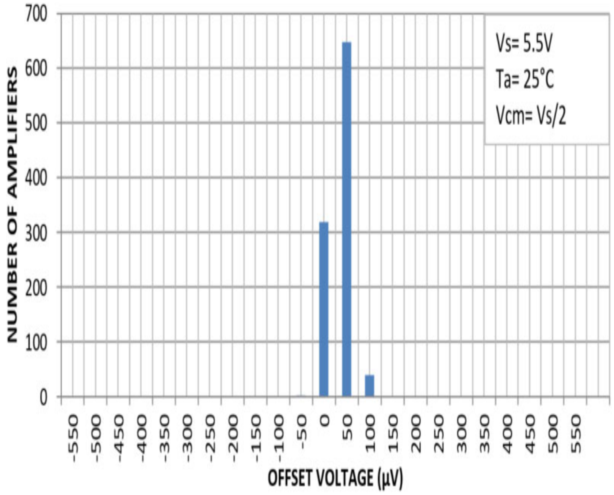


Figure 1. Input Offset Voltage Distribution, V_S = 5.5 V, 25°C

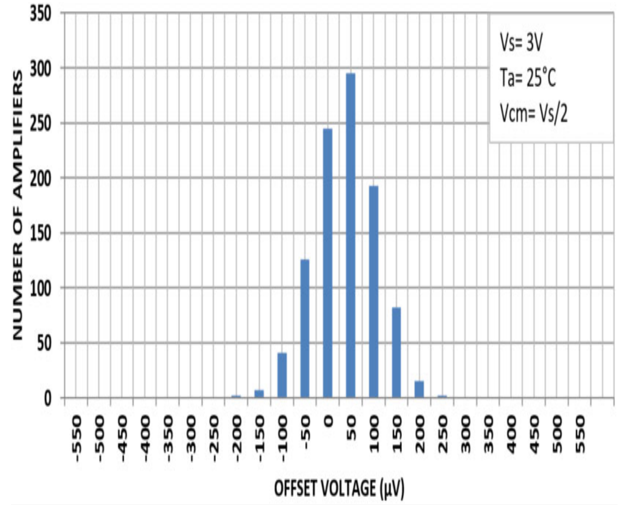


Figure 2. Input Offset Voltage Distribution, V_S = 3 V, 25°C

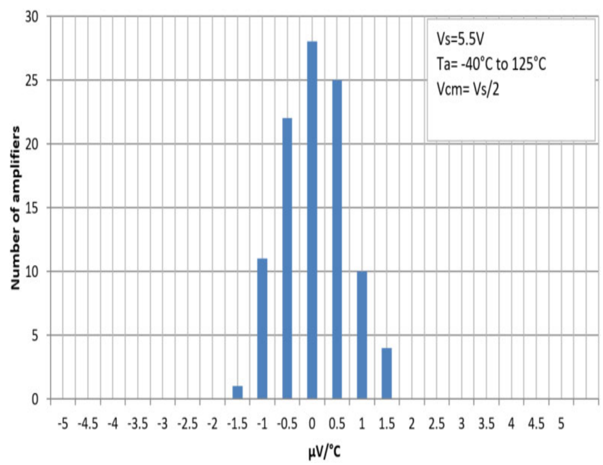


Figure 3. Input Offset Voltage vs. Temperature Distribution, V_S = 5.5 V

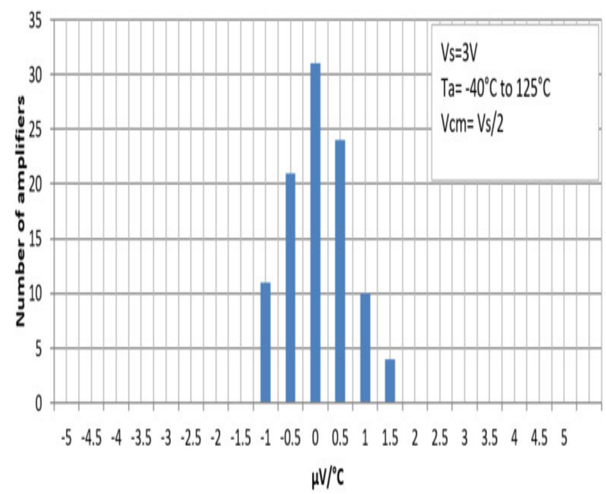


Figure 4. Input Offset Voltage vs. Temperature Distribution, V_S = 3 V

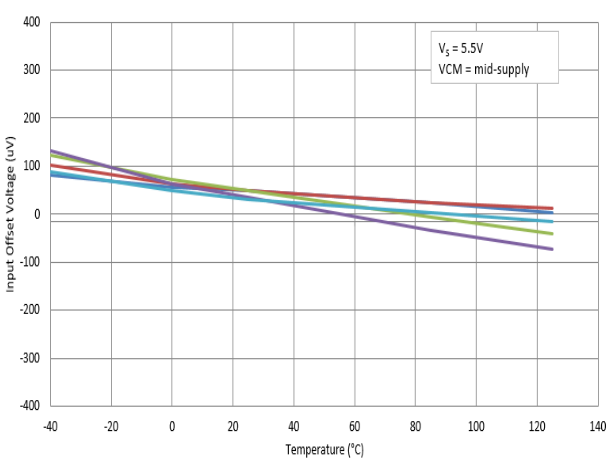


Figure 5. Input Offset Voltage vs. Temperature, V_S = 5.5 V

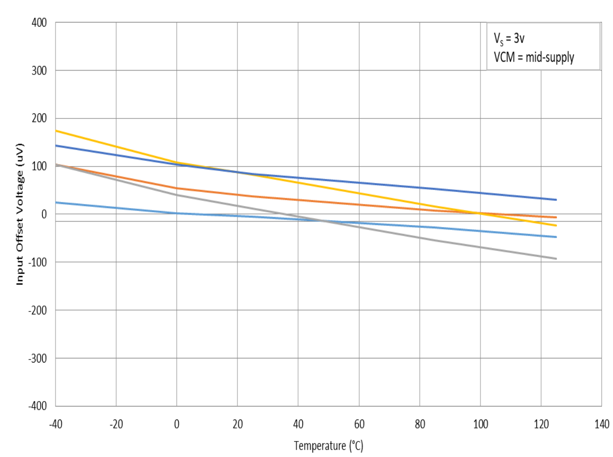


Figure 6. Input Offset Voltage vs. Temperature, V_S = 3 V

TYPICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 5.5$ V, $V_{CM} = V_S/2$, unless otherwise noted.

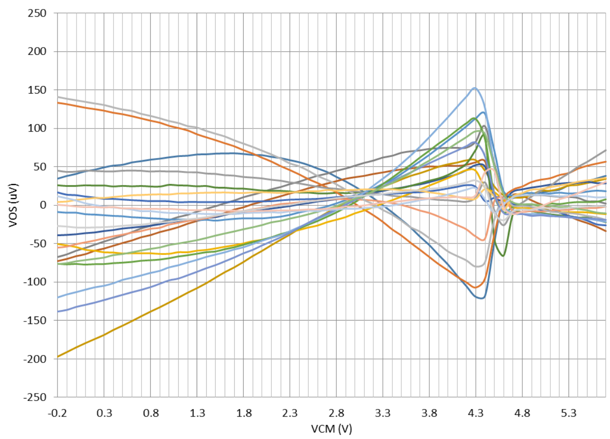


Figure 7. Input Offset Voltage vs. Input Common Mode Voltage, $V_S = 5.5$ V

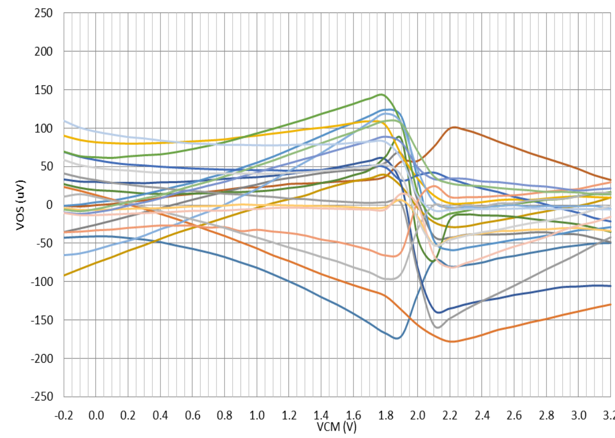


Figure 8. Input Offset Voltage vs. Input Common Mode Voltage, $V_S = 3$ V

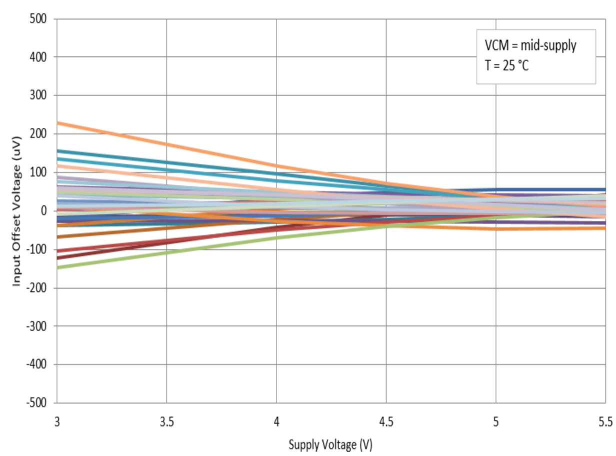


Figure 9. Input Offset Voltage vs. Supply Voltage, 25°C

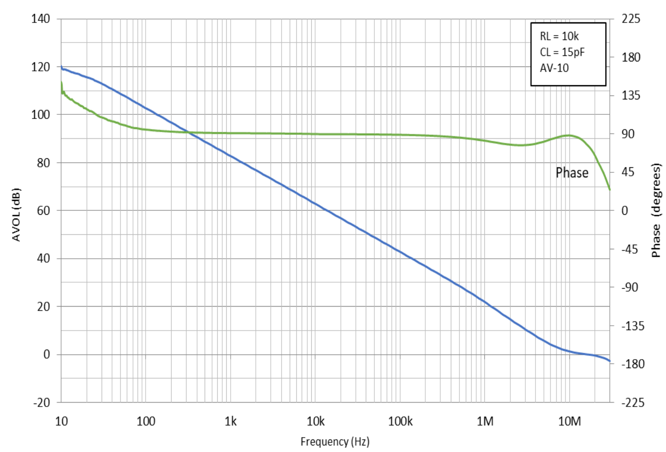


Figure 10. Gain and Phase vs. Frequency, $V_S = 5.5$ V

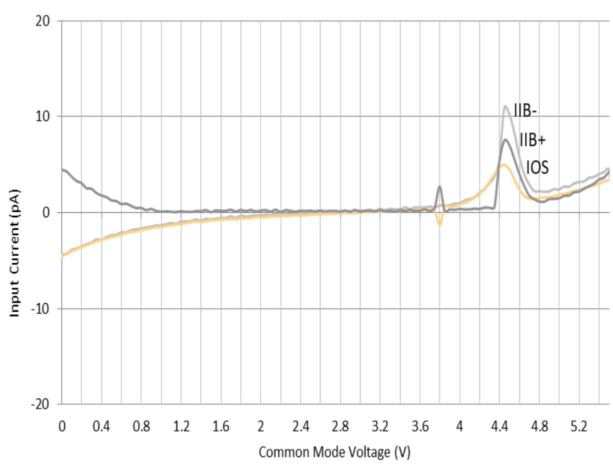


Figure 11. Input Bias and Offset Current vs. Common Mode Voltage, $V_S = 5.5$ V

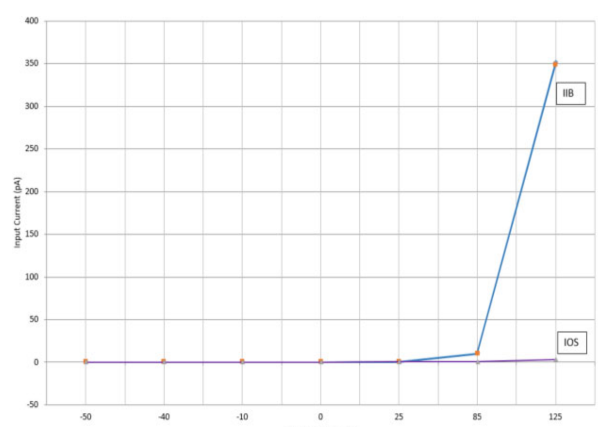


Figure 12. Input Bias Current and Input Offset Current vs. Temperature, $V_S = 5.5$ V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

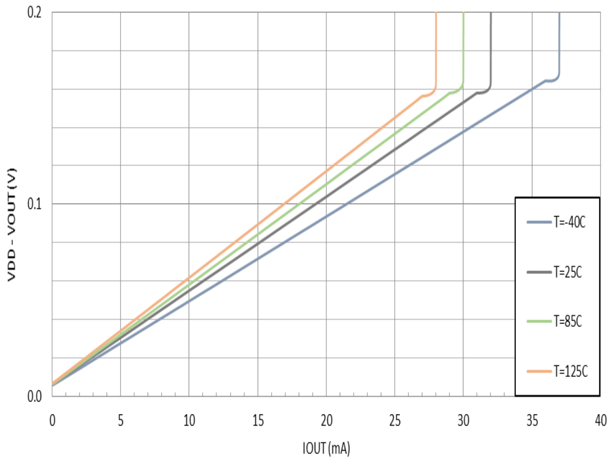


Figure 13. V_{OH} vs. Output Current vs. Temperature, V_S = 5.5 V

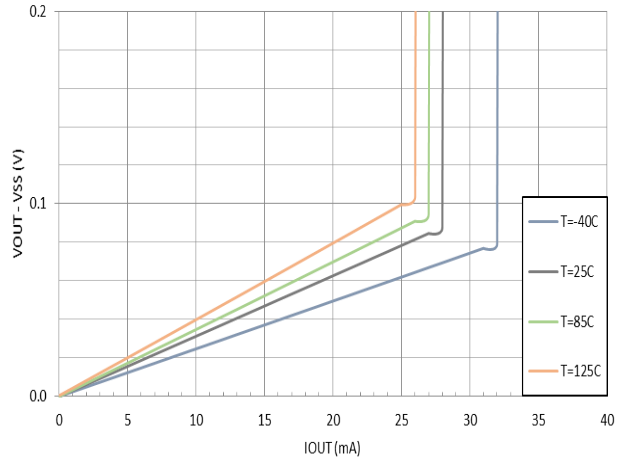


Figure 14. V_{OL} vs. Output Current vs. Temperature, V_S = 5.5 V

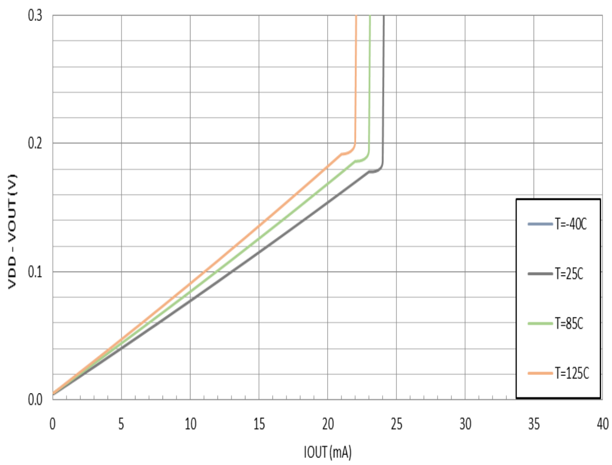


Figure 15. V_{OH} vs. Output Current vs. Temperature, V_S = 3 V

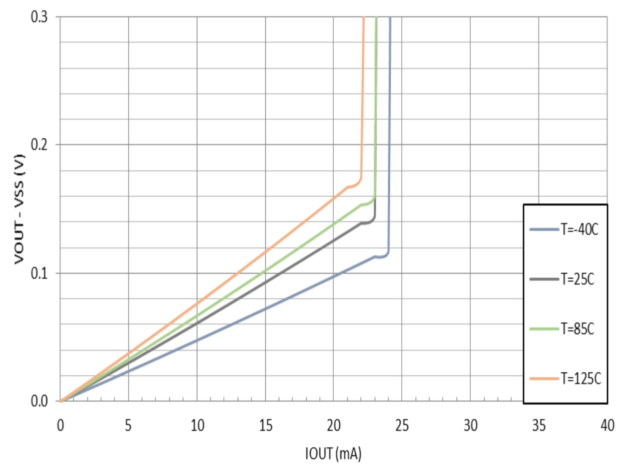


Figure 16. V_{OL} vs. Output Current vs. Temperature, V_S = 3 V

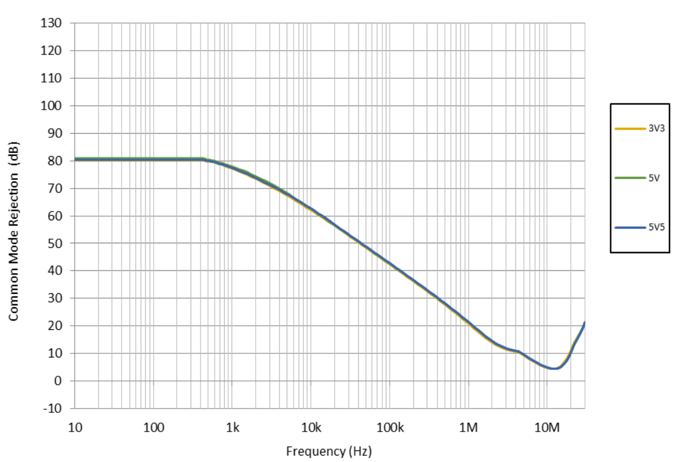


Figure 17. Common Mode Rejection Ratio vs. Frequency

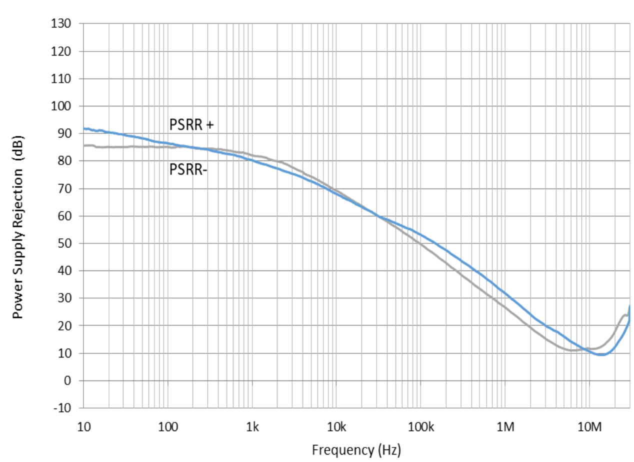


Figure 18. Power Supply Rejection Ratio vs. Frequency, V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

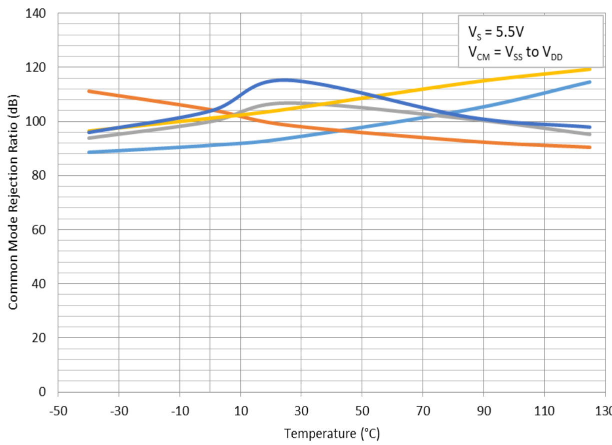


Figure 19. Common Mode Rejection Ratio vs. Temperature, V_S = 5.5 V

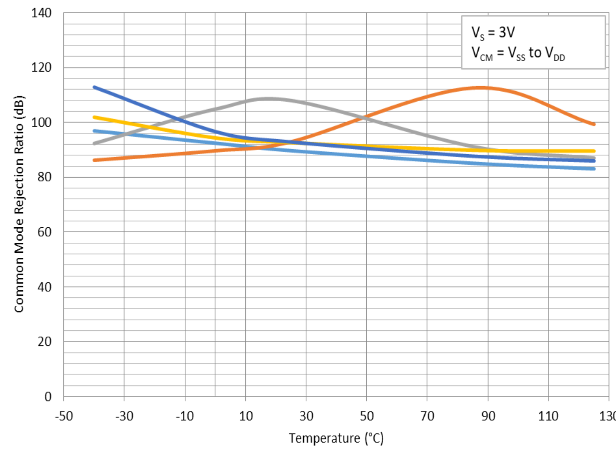


Figure 20. Common Mode Rejection Ratio vs. Temperature, V_S = 3 V

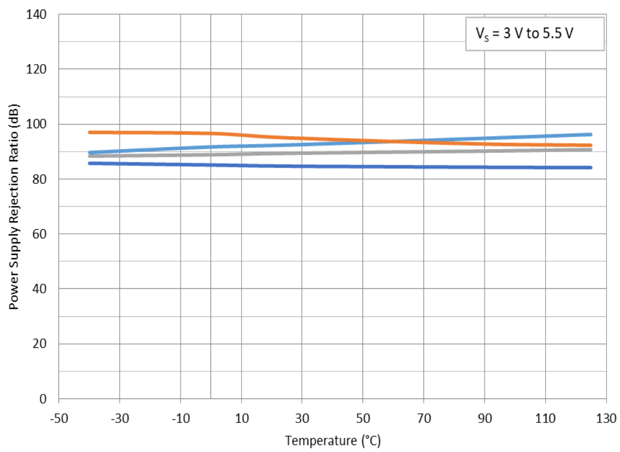


Figure 21. Power Supply Rejection Ratio vs. Temperature

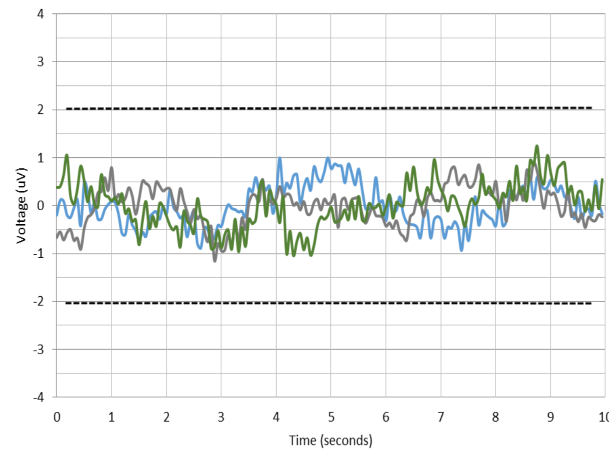


Figure 22. 0.1 Hz 10 Hz Voltage Noise

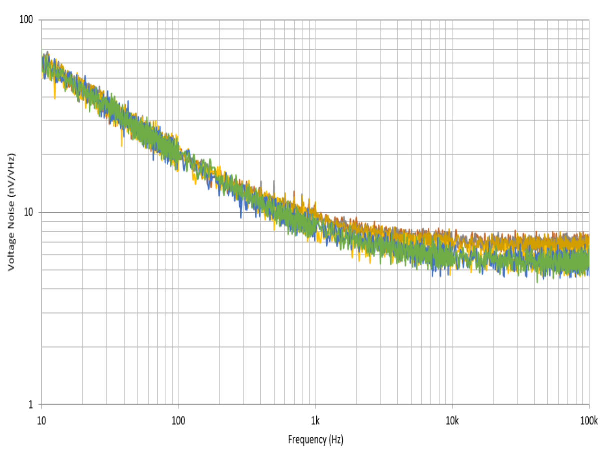


Figure 23. Voltage Noise Density vs. Frequency

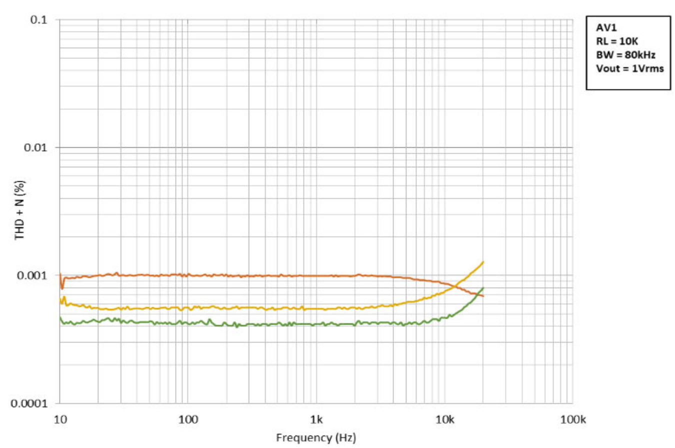


Figure 24. THD + Noise vs. Frequency, V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

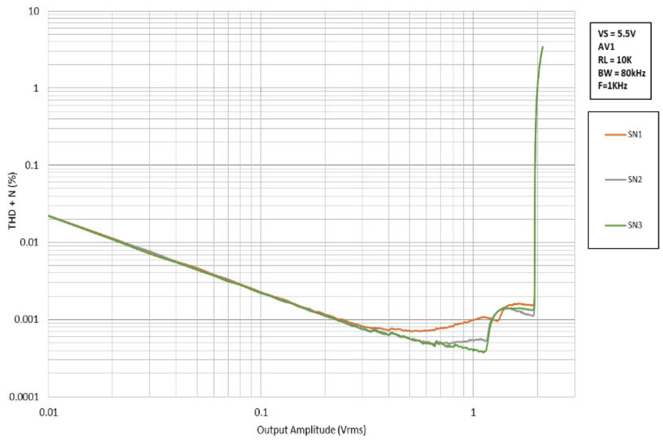


Figure 25. THD + Noise vs. Output Amplitude at 1 KHz

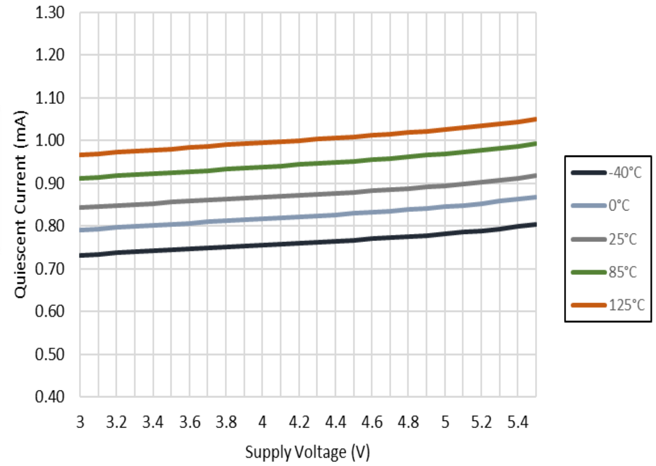


Figure 26. Quiescent Current vs. Supply Voltage

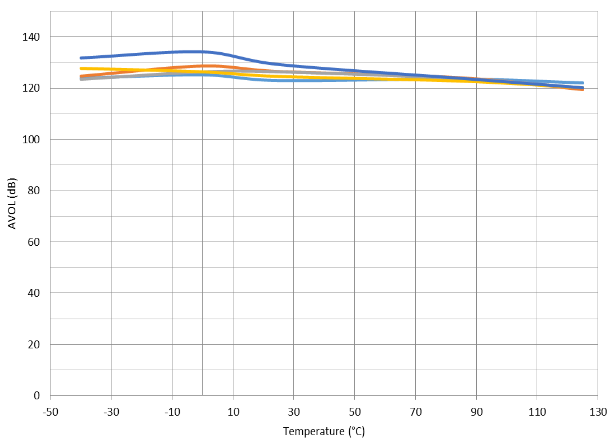


Figure 27. Open Loop Gain vs. Temperature, V_S = 5.5 V

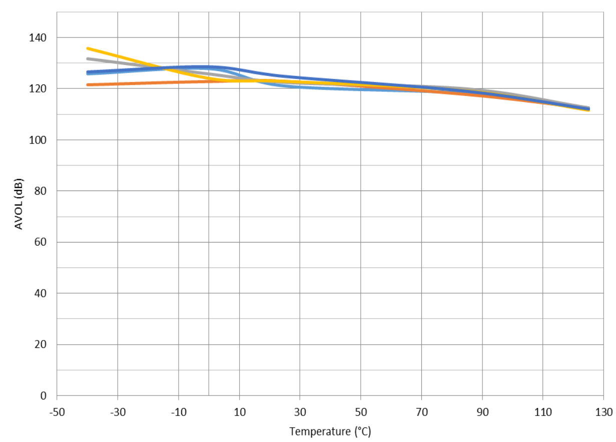


Figure 28. Open Loop Gain vs. Temperature, V_S = 3 V

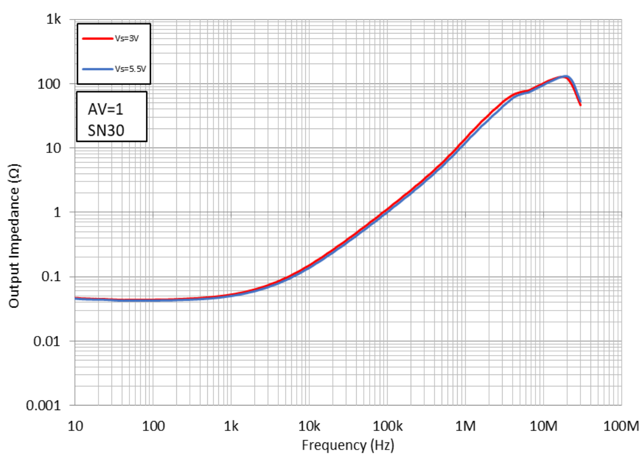


Figure 29. Open Loop Output Impedance vs. Frequency

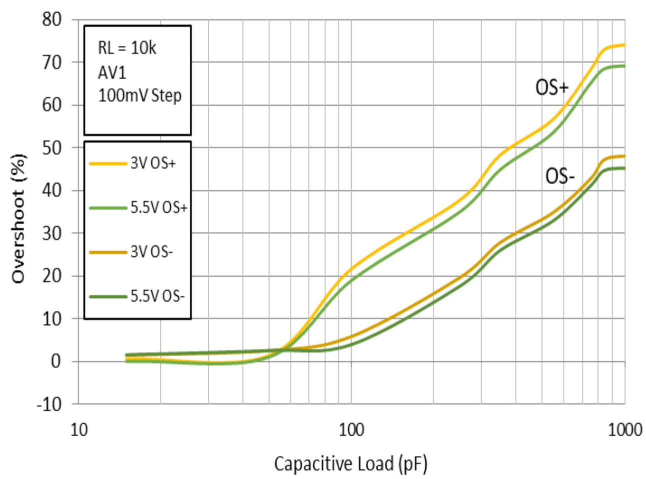


Figure 30. Small Signal Overshoot vs. Capacitive Load

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

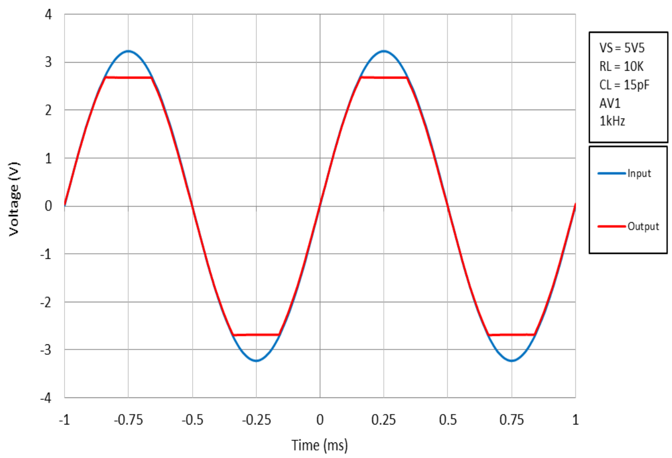


Figure 31. No Phase Reversal, V_S = 5.5 V

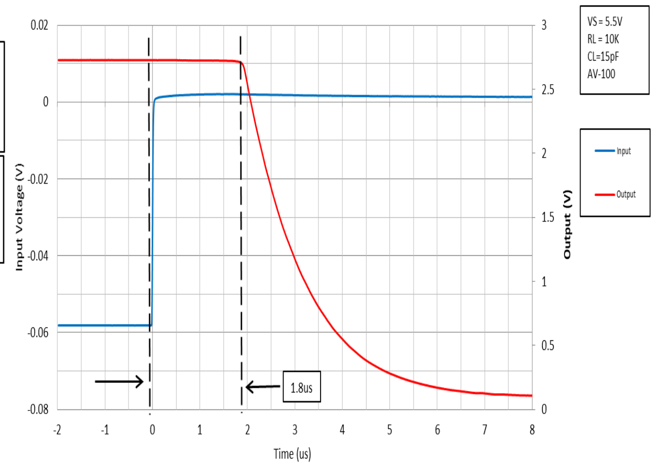


Figure 32. Positive Overload Recovery, V_S = 5.5 V

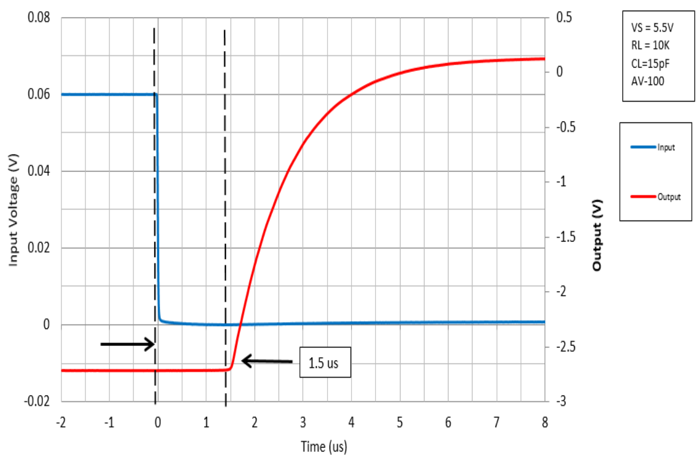


Figure 33. Negative Overload Recovery, V_S = 5.5 V

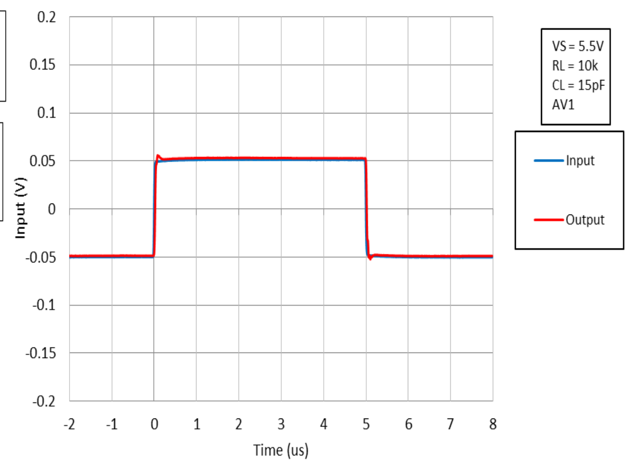


Figure 34. Small Signal Step Response, Non−Inverting, V_S = 5.5 V

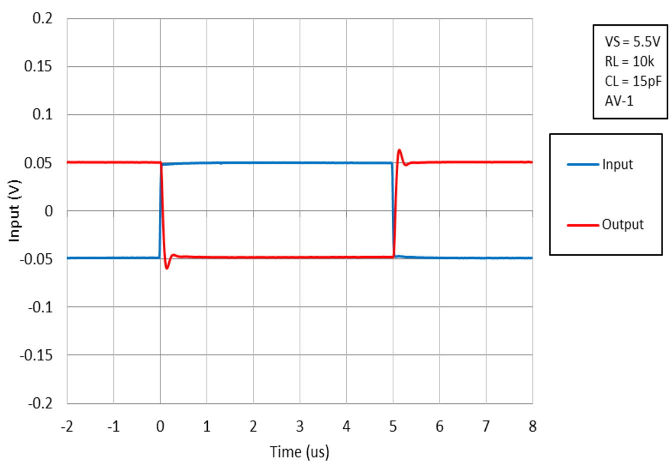


Figure 35. Small Signal Step Response, Inverting, V_S = 5.5 V

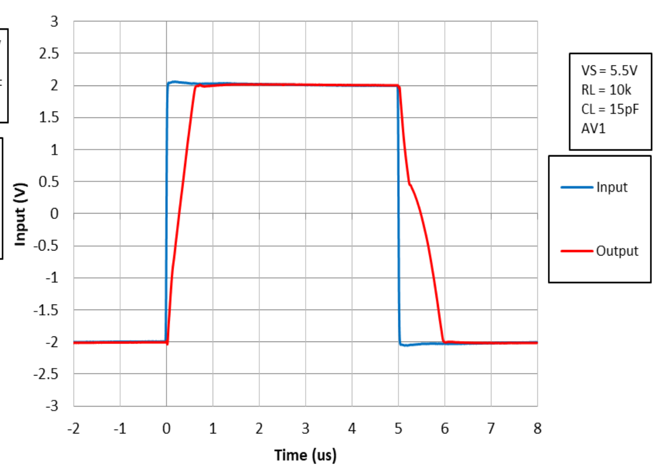


Figure 36. Large Signal Step Response, Non−Inverting, V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

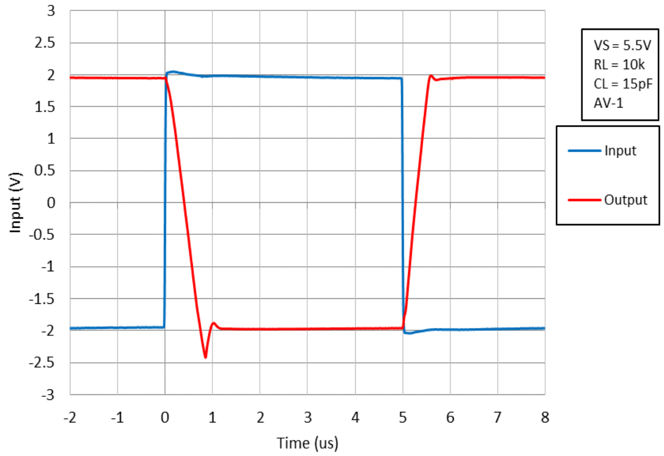


Figure 37. Large Signal Step Response, Inverting, V_S = 5.5 V

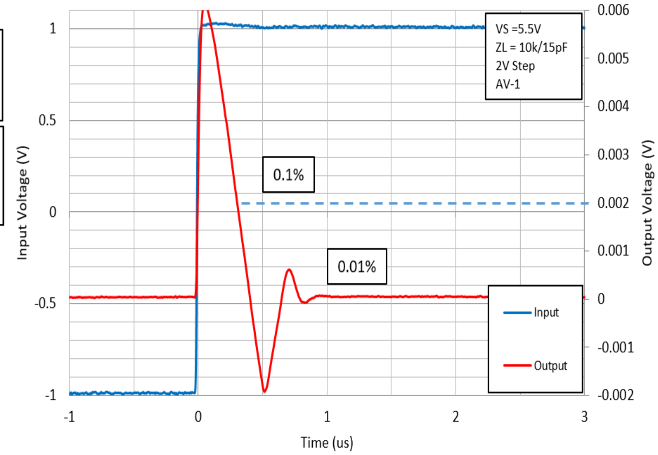


Figure 38. Large Signal Settling Time (2 V Negative Step)

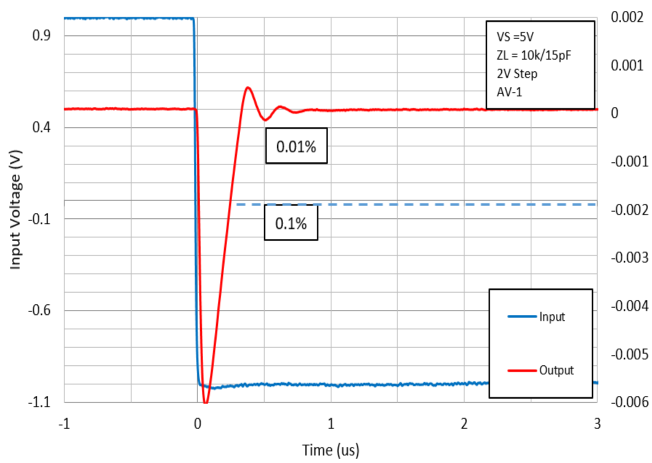


Figure 39. Large Signal Settling Time (2 V Positive Step)

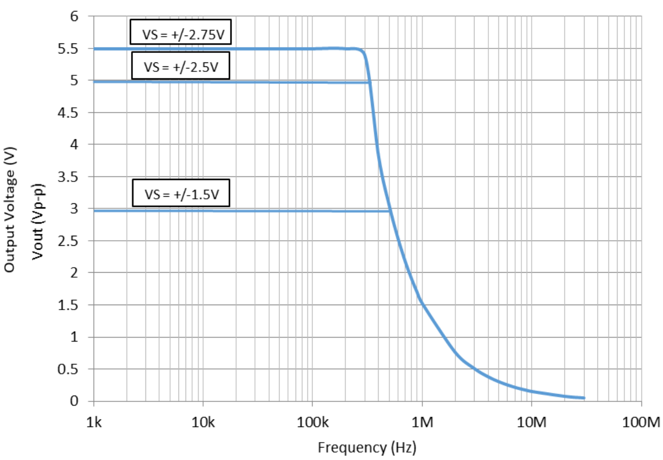


Figure 40. Full Power Bandwidth

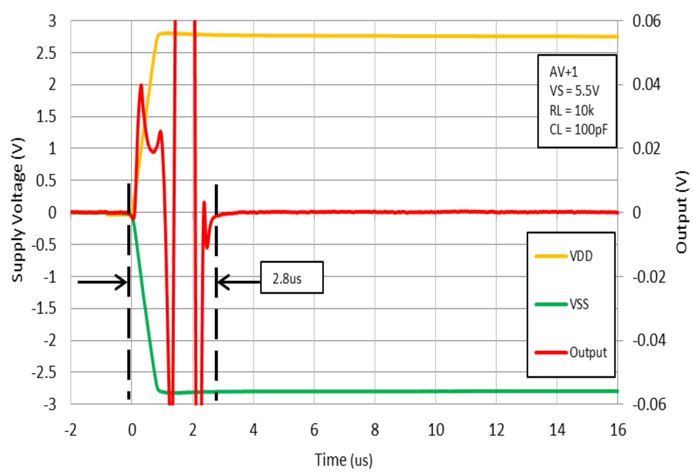


Figure 41. Turn On Time, V_S = 5.5 V

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Low−Side Current Sensing

The goal of low−side current sensing is to detect over−current conditions or as a method of feedback control. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

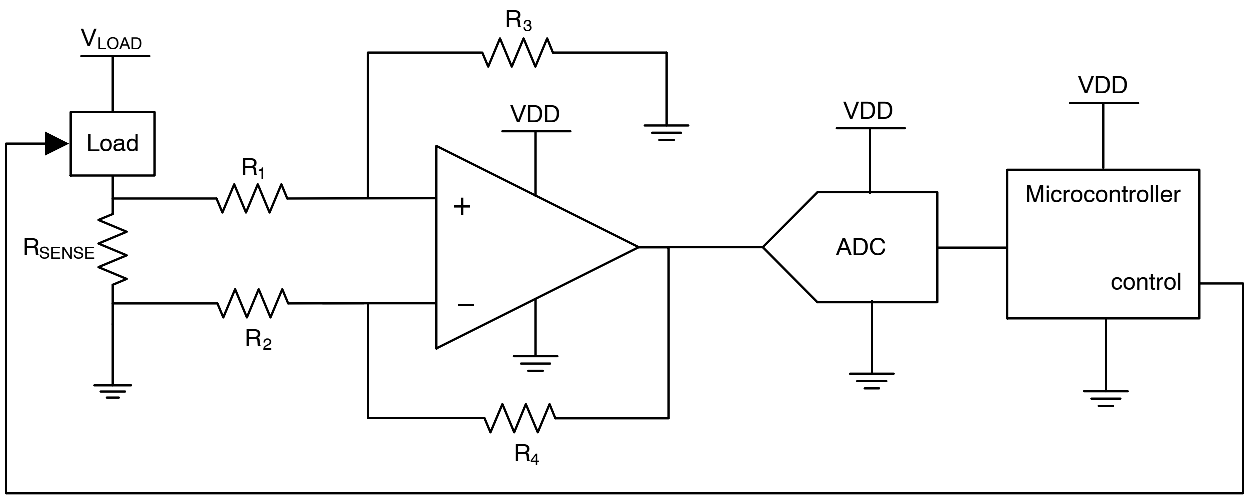


Figure 42. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 43. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

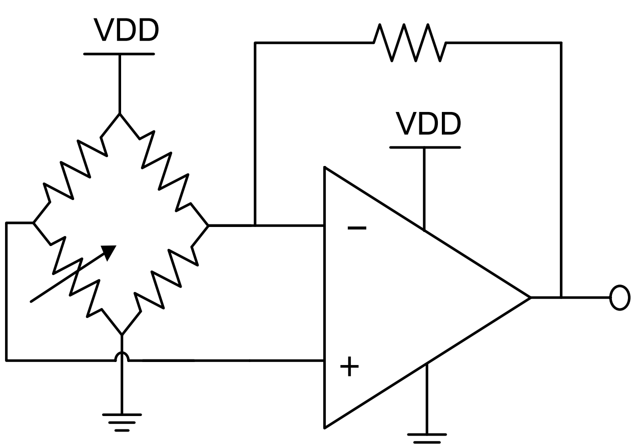
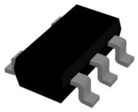


Figure 43. Bridge Circuit Amplification

GENERAL LAYOUT GUIDELINES

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric−coefficients and prevent temperature gradients from heat sources or cooling fans.



SC−74A−5 3.00x1.50x0.95, 0.95P

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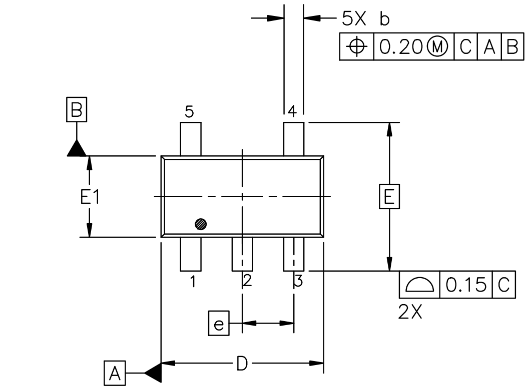
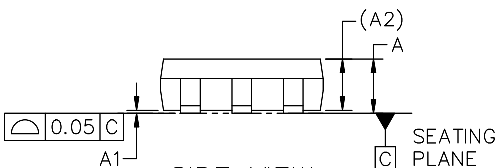


TOP VIEW

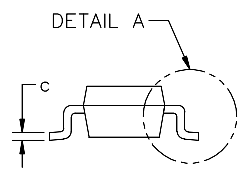
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

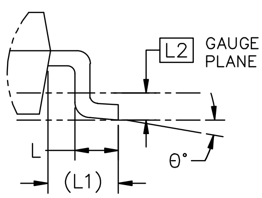
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.01	0.18	0.10
A2	0.95 REF.		
b	0.25	0.37	0.50
c	0.10	0.18	0.26
D	2.85	3.00	3.15
E	2.75 BSC		
E1	1.35	1.50	1.65
e	0.95 BSC		
L	0.20	0.40	0.60
L1	0.62 REF.		
L2	0.25 BSC		
θ	0°	5°	10°



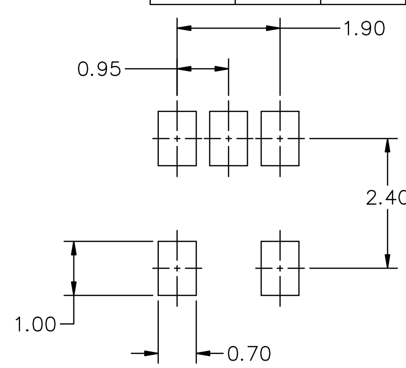
SIDE VIEW



END VIEW



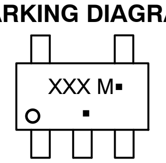
DETAIL "A"
SCALE 2:1



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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