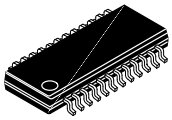
Remote Thermal Monitor and Fan Controller with PECI 3.0 Interface and SMBus Compatible Master

NCT7491

QFN24
MN SUFFIX
CASE 485L



QSOP24
RQ SUFFIX
CASE 492B

The NCT7491 is a two−wire serially programmable hardware monitor. It can monitor 2 remote temperature zones and its own ambient temperature. A PECI 3.0 single wire interface allows the NCT7491 to monitor CPU temperatures. The NCT7491 also implements an SMBus compatible master, allowing it to read automatically from thermal sensors on the SMBus. The NCT7491 can automatically control the speed of 3 fans using PWM control, and monitor the speed of 4 fans. There are 4 analog inputs, used for measuring 12 V, 5 V, 2.5 V and Vccp channels. The NCT7491 supply voltage and PECI V_{TT} voltage are also monitored. Each of the measured temperature, voltage and fan speed values are compared with programmable limits and if any channel is outside the programmed limit an interrupt is generated via the ALERT output pin. A THERM output is also available for fail−safe thermal control. Up to 3 GPIO pins are available for digital control or signalling.

Communication with the NCT7491 is accomplished via the SMBus/I^2C interface which is compatible with industry standard protocols. The SMBus address is set by 2 address selection pins.

The NCT7491 is available in a 24−lead QFN or QSOP package and operates over a supply range of 3.0 V to 3.6 V.

Features

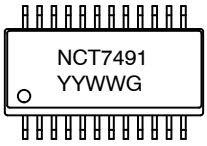
- PECI 3.0 Master for CPU Monitoring
- SMBus Compatible Master
- On−chip Temperature Sensor
- 2 Remote Sensor Channels
- Series Resistance Cancellation on Remote Sensors
- 3 PWM Fan Control Outputs
- 4 Tach Monitoring Input
- PWM Automatic Fan Speed Control
- 4 Analog Inputs for Voltage Monitoring
- Vdd Supply Voltage Monitoring
- PECI V_{TT} Voltage Monitoring
- Overtemperature Outputs
- Limit Comparison of Monitored Channels
- SMBus Address Selection Allows up to 3 Devices
- Meets SMBus 2.0 Electrical Specifications (fully SMBus 1.1 compliant)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS

(Top View)

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



(Top View)

(Bottom View)

NCT7491 = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 79 of this data sheet.

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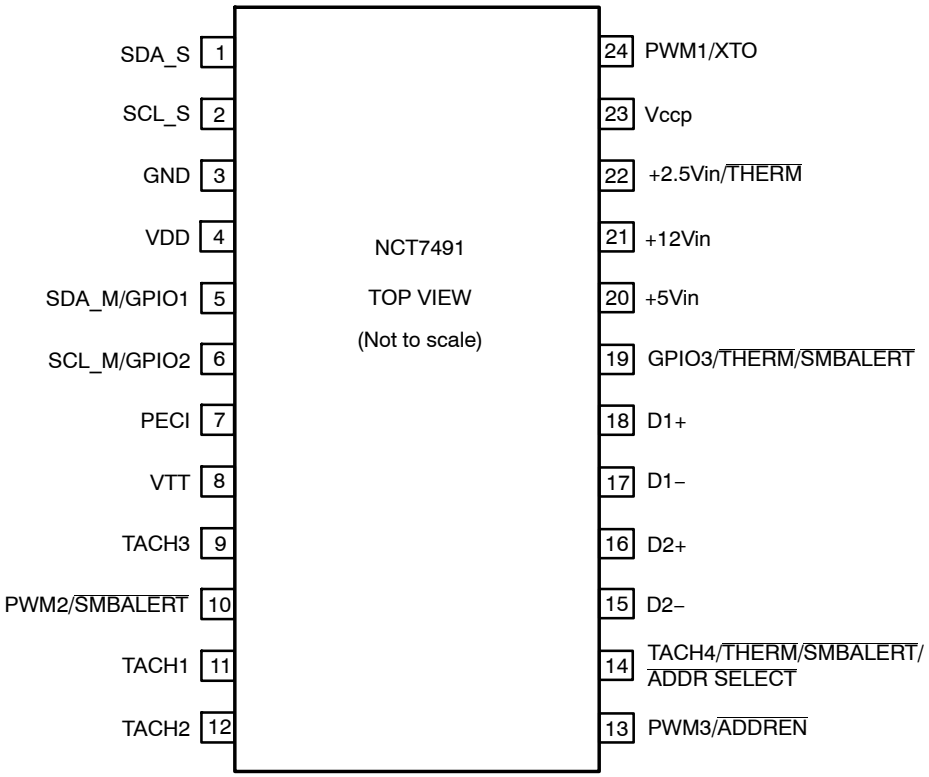
NCT7491 QSOP PINOUT



NCT7491 QFN PINOUT

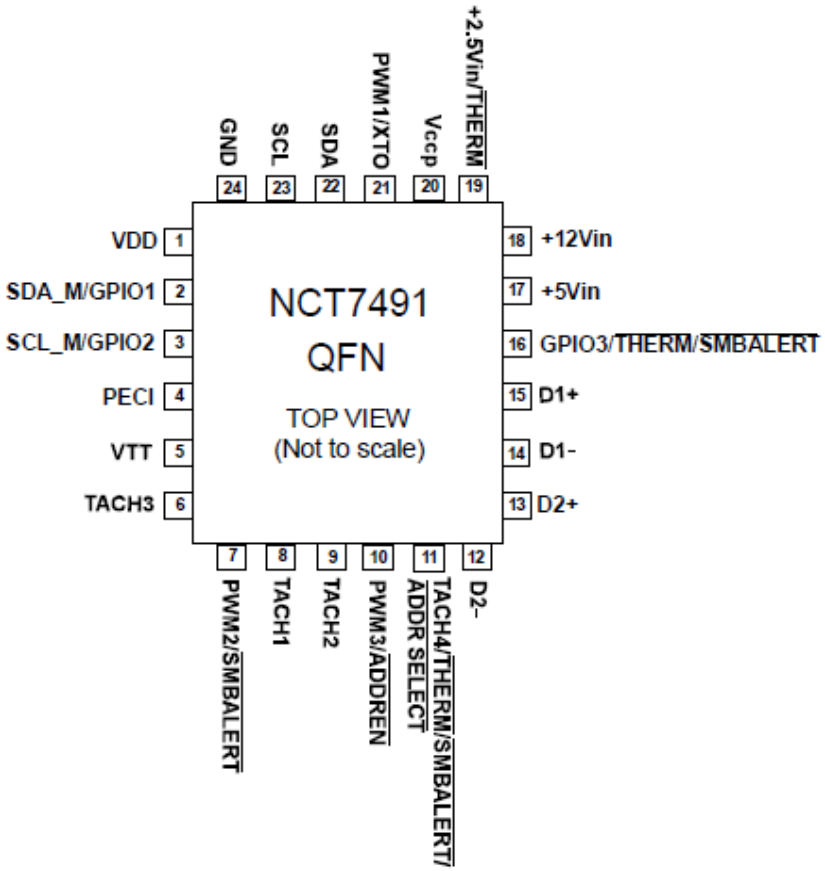


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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Positive Supply Voltage (V_{CC})	3.6 V
Maximum Voltage on +12V_{IN} Pin	14 V
Maximum Voltage on +5V_{IN} Pin	6.25 V
Maximum Voltage on All Open−Drain Outputs (excluding PWM pins)	3.6 V
Maximum Voltage on PWM Pins	+5.5 V
Maximum Voltage on TACH Pins	+5.5 V
Voltage on Remaining Input or Output Pins	−0.3 V to +4.2 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature ($T_{J\ max}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
IR Reflow Peak Temperature	220°C
Pb−Free Peak Temperature	260°C
Lead Temperature (Soldering, 10 sec)	300°C
ESD Rating	
HBM	2 kV
FICDM	0.5 kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Specifications

T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted. All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are at T_A = 25°C and represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge, and V_{IH} = 2.0 V for a rising edge. SMBus timing specifications are guaranteed by design and are not production tested.

Table 2. SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	3.3	3.6	V	
Supply Current, I_{CC}		1.5	5	mA	Interface inactive, ADC active
TEMP−TO−DIGITAL CONVERTER					
Local Sensor Accuracy		±0.5	±3.5	°C	0°C ≤ T_A ≤ 85°C
Local Sensor Resolution		0.25		°C	
Remote Diode Sensor Accuracy		±0.5	±3.5	°C	0°C ≤ T_A ≤ 85°C −40°C ≤ T_D ≤ 125°C
Remote Sensor Resolution		0.25		°C	
Remote Sensor Source Current		30		μA	Low Level 1
		240		μA	High Level 1
		37.5		μA	Low Level 2
		300		μA	High Level 2
Series Resistance Cancellation			270	Ω	

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Table 2. SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENTUATORS)					
Total Unadjusted Error (TUE)			±2	%	For 12 V channel
			±1.5	%	For all other channels
Differential Nonlinearity (DNL)			±1	LSB	8 bits
Power Supply Sensitivity		±0.1		%/V	
Conversion Time (Voltage Input)		11		ms	Averaging enabled, 16 samples per averaged reading.
Conversion Time (Local Temperature)		38		ms	Averaging enabled, 16 samples per averaged reading.
Conversion Time (Remote Temperature)		38		ms	Averaging enabled, 16 samples per averaged reading.
Input Resistance		224		kΩ	For +12 V channel
		110		kΩ	For all other channels
FAN RPM−TO−DIGITAL CONVERTER					
Accuracy			±10	%	$0°C \le T_A \le 85°C$
			±14	%	$-40°C \le T_A \le 125°C$
Full−Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan count = 0xBFFF
		329		RPM	Fan count = 0x3FFF
		5,000		RPM	Fan count = 0x0438
		10,000		RPM	Fan count = 0x021C
OPEN−DRAIN DIGITAL OUTPUTS, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}			8.0	mA	
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = −8.0 mA
High Level Output Current, I_{OH}		0.1	20	μA	$V_{OUT} = V_{CC}$
OPEN−DRAIN SERIAL DATA BUS OUTPUTS (SDA, SDA_M, SCL_M)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = −4.0 mA
High Level Output Current, I_{OH}		0.1	1.0	μA	$V_{OUT} = V_{CC}$
SMBus DIGITAL INPUTS (SCL, SDA, SDA_M)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
Hysteresis		500		mV	
DIGITAL I/O (PECI PIN)					
V_{TT} Supply Voltage	0.85		1.26	V	
Input High Voltage, V_{IH}	0.55*V_{tt}			V	
Input Low Voltage, V_{IL}			0.5*V_{tt}	V	
Hysteresis	0.1V_{tt}			V	Hysteresis between input switching levels
High level output source current, I_{SOURCE}	−6			mA	Output High Voltage, V_{OH} = 0.75*V_{tt}
Low level output sink current, I_{SINK}	0.5		1.0	mA	Output Low Voltage, V_{OL} = 0.25*V_{tt}
Signal noise immunity, V_{noise}	300			mV_{p-p}	Noise glitches from 10 − 100MHz Width up to 50ns

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Table 2. SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	2.0			V	
			5.5	V	Maximum input voltage
Input Low Voltage, V_{IL}			0.8	V	
	−0.3			V	Minimum input voltage
Hysteresis		0.5		V_{p-p}	
DIGITAL INPUT LOGIC LEVELS ($\overline{THERM}$)					
Input High Voltage, V_{IH}			0.75 x V_{TT}	V	
Input Low Voltage, V_{IL}			0.4	V	
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}		±1		μA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}		±1		μA	$V_{IN} = 0$
Input Capacitance, C_{IN}		5		pF	
SLAVE SERIAL BUS TIMING (See Figure 1)					
Clock Frequency, f_{SCLK}	10		100	kHz	
Glitch Immunity, t_{SW}			50	ns	
Bus Free Time, t_{BUF}	4.7			μs	
SCL Low Time, t_{LOW}	4.7			μs	
SCL High Time, t_{HIGH}	4.0		50	μs	
SCL, SDA Rise Time, t_r			1,000	ns	
SCL, SDA Fall Time, t_f			300	ns	
Data Setup Time, $t_{SU;DAT}$	250			ns	
Detect Clock Low Timeout, $t_{TIMEOUT}$	15		35	ms	Can be optionally disabled
MASTER SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}		100		kHz	

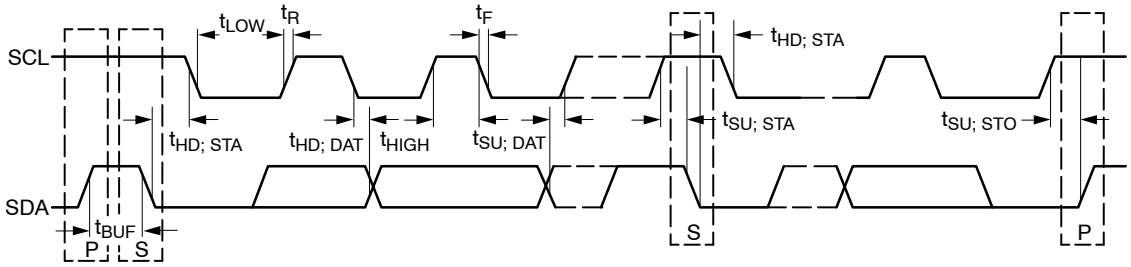

Figure 1. SMBus Timing Diagram for Slave Port and Master Port

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Table 3. QSOP & QFN PACKAGE PIN ASSIGNMENTS

QSOP Pin No.	QFN Pin No.	Pin Name	Description
1	22	SDA_S	SMBus/I^{2}C Slave Serial Bi−directional Data Input/Output. Open−drain pin; Requires a pull−up resistor.
2	23	SCL_S	Serial Clock Slave Input. Open−drain pin; Requires a pull−up resistor.
3	24	GND	Ground
4	1	VDD	Positive Supply Voltage
5	2	SDA_M / GPIO1	Open−drain pin; Requires a pull−up resistor. GPIO1 = General purpose I/O pin SDA_M = SMBus/I^{2}C Master Serial Bi−directional Data Input/Output.
6	3	SCL_M / GPIO2	Open−drain pin; Requires a pull−up resistor. GPIO2 = General purpose I/O pin SCL_M = Serial Clock Master Output.
7	4	PECI	PECI input to report CPU Thermal Information. PECI voltage level is referenced to the VTT input.
8	5	VTT	Voltage reference for PECI. This is the supply voltage for the PECI interface and must be present to communicate over the PECI interface.
9	6	TACH3	Fan tachometer input to measure Fan3
10	7	PWM2 / #SMBALERT	PWM output to control Fan2. Can be configured as an SMBALERT output. Open−drain pin; Requires a pull−up resistor.
11	8	TACH1	Fan tachometer input to measure Fan1
12	9	TACH2	Fan tachometer input to measure Fan2
13	10	PWM3 / #ADDREN	PWM output to control Fan3. If pulled low on power−up the NCT7491 enters Address Select mode and the ADDRESS SELECT pin determines the slave address. Open−drain pin; Requires a pull−up resistor.
14	11	TACH4/ #THERM/ #SMBALERT/ #ADDRESS SELECT	Fan Tachometer Input to Measure Speed of Fan 4. May be reconfigured as a bidirectional THERM. Can be connected to thePROCHOT output of a processor, to time and monitor PROCHOT assertions. Can be used as an output to signal an overtemperature condition. The SMBALERT pin is used to signal out−of−limit comparisons of temperature, voltage, and fan speed. This is compatible with SMBus alert. Can also be used at device powerup to assign the SMBus address. If THERM or SMBALERT is enabled then a pull−up resistor is required.
15	12	D2−	Negative Connection for Remote Temperature Sensor 2.
16	13	D2+	Positive Connection for Remote Temperature Sensor 2.
17	14	D1−	Negative Connection for Remote Temperature Sensor 1.
18	15	D1+	Positive Connection for Remote Temperature Sensor 1.
19	16	GPIO3/ #THERM/ #SMBALERT	General−Purpose Open−Drain Digital Input/Output. Requires a pull−up resistor. Can be configured as a bidirectional THERM pin or as an SMBALERT pin.
20	17	+5Vin	Analog Input. 0 V to 5 V.
21	18	+12Vin	Analog Input. 0 V to 12 V.
22	19	+2.5V / #THERM	Analog Input. 0 V to 2.5 V. May be reconfigured as a bidirectional THERM pin. Can be connected to the PROCHOT output of a processor, to time and monitor PROCHOT assertions. Can be used as an output to signal an overtemperature condition. In THERM mode it is an open−drain bidirectional pin and requires a pull up resistor.
23	20	Vccp	Analog input. Monitors CPU core voltage (to maximum 0f 3.0 V). This pin must be connected to the NCT7491 supply voltage if it is unused.
24	21	PWM1 / XTO	PWM output to control Fan 1. Open−drain pin; Requires a pull−up resistor. Also functions as the output for the XNOR tree test enable mode.

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Table 4. COMPARISON OF NCT7491 AND ADT7490 QSOP PINOUTS

QSOP Pin No.	NCT7491	ADT7490
1	SDA_S	SDA
2	SCL_S	SCL
3	GND	GND
4	VDD	VDD
5	SDA_M / GPIO1	GPIO1
6	SCL_M / GPIO2	GPIO2
7	PECI	PECI
8	VTT	VTT
9	TACH3	TACH3
10	PWM2 / #SMBALERT	PWM2 / #SMBALERT
11	TACH1	TACH1
12	TACH2	TACH2
13	PWM3 /#ADDREN	PWM3 /#ADDREN
14	TACH4/#THERM/#SMBALERT/ #ADDRESS SELECT	TACH4/#THERM/#SMBALERT/ #ADDRESS SELECT
15	D2–	D2–
16	D2+	D2+
17	D1–	D1–
18	D1+	D1+
19	GPIO3/#THERM/#SMBALERT	IMON
20	+5Vin	+5Vin
21	+12Vin	+12Vin
22	+2.5V / #THERM	+2.5V / #THERM
23	Vccp	Vccp
24	PWM1 / XTO	PWM1 / XTO

FUNCTIONAL COMPARISON BETWEEN THE NCT7491 AND THE ADT7490

- NCT7491 supports PECI 3.0 commands.
- NCT7491 uses an SMBus Master port to read digital temperatures.
- I_{MON} voltage monitoring pin (pin 19) on the ADT7490 is replaced with digital pin (SMBALERT/THERM/GPIO) on the NCT7491
- NCT7491 does not support Dynamic Tmin fan control.
- NCT7491 allows any combination of temperature sources to control any fan.
- NCT7491 allows individual PWM responses to THERM events.
- NCT7491 THERM behaviour is more flexible, allowing stepped response to THERM events.
- REPLACE mode for PECI is not supported by the NCT7491
- The NCT7491 register map is organized into two pages. 0x00–0xFF (page 1) and 0x100–0x1FF (page 2)
- The NCT7491 supports PWM look–up table automatic fan control along with the Tmin/Trange control method used in the ADT7490
- The NCT7491 allows temperatures to be written to the device from an external master. These values can be assigned for fan control and Limit/THERM assertion functions
- PECI fan control can be implemented in relative or absolute modes. Absolute mode uses the Tjmax value read from the CPU plus the PECI temperature to determine the actual core temperature.
- The reference for voltage measurement has changed from 2.25 V on the ADT7490 to 2 V on the NCT7491.

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FUNCTIONAL BLOCK DIAGRAM

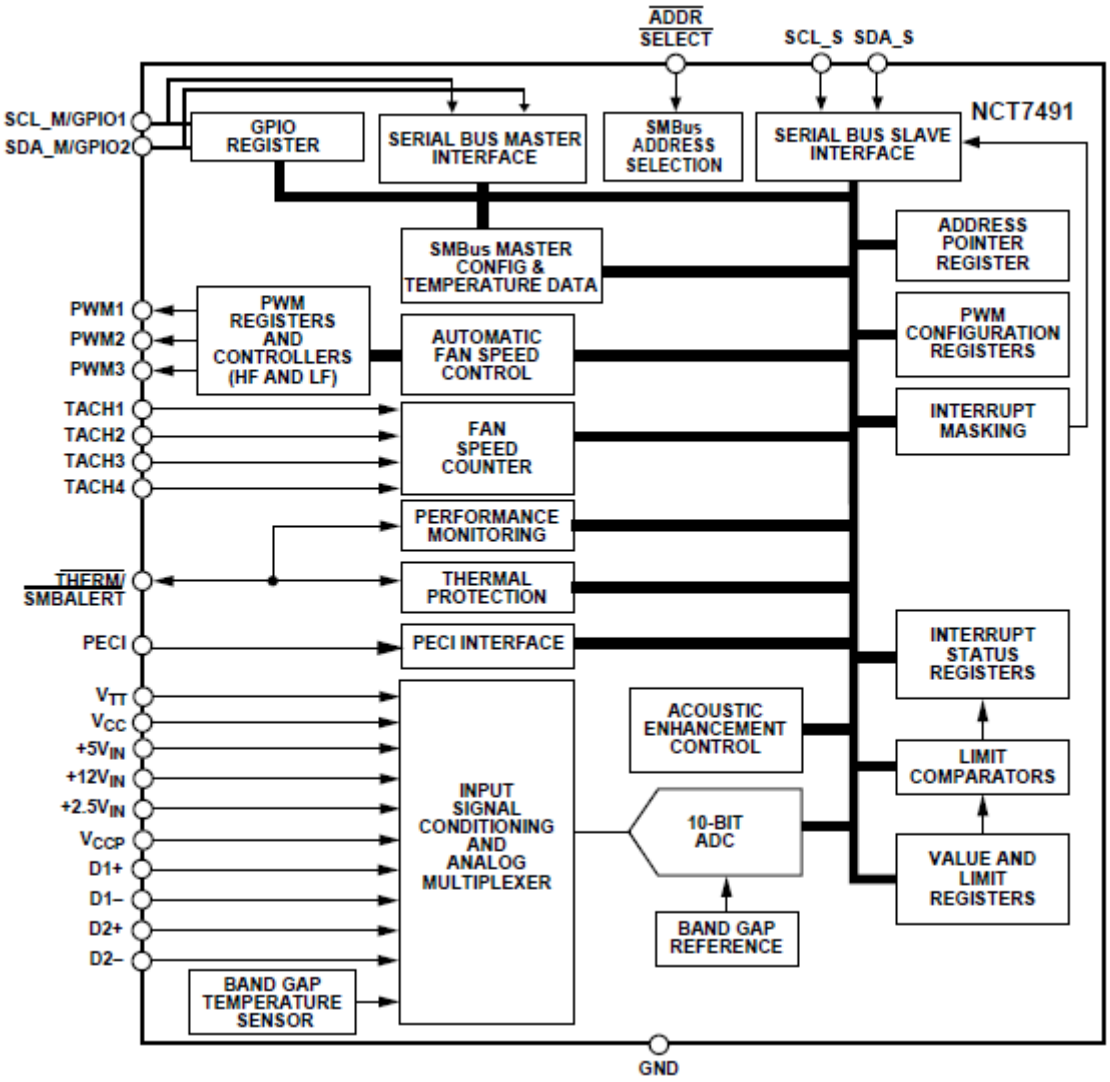

Figure 2. Functional Block Diagram of NCT7491

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TYPICAL SYSTEM CONNECTIONS

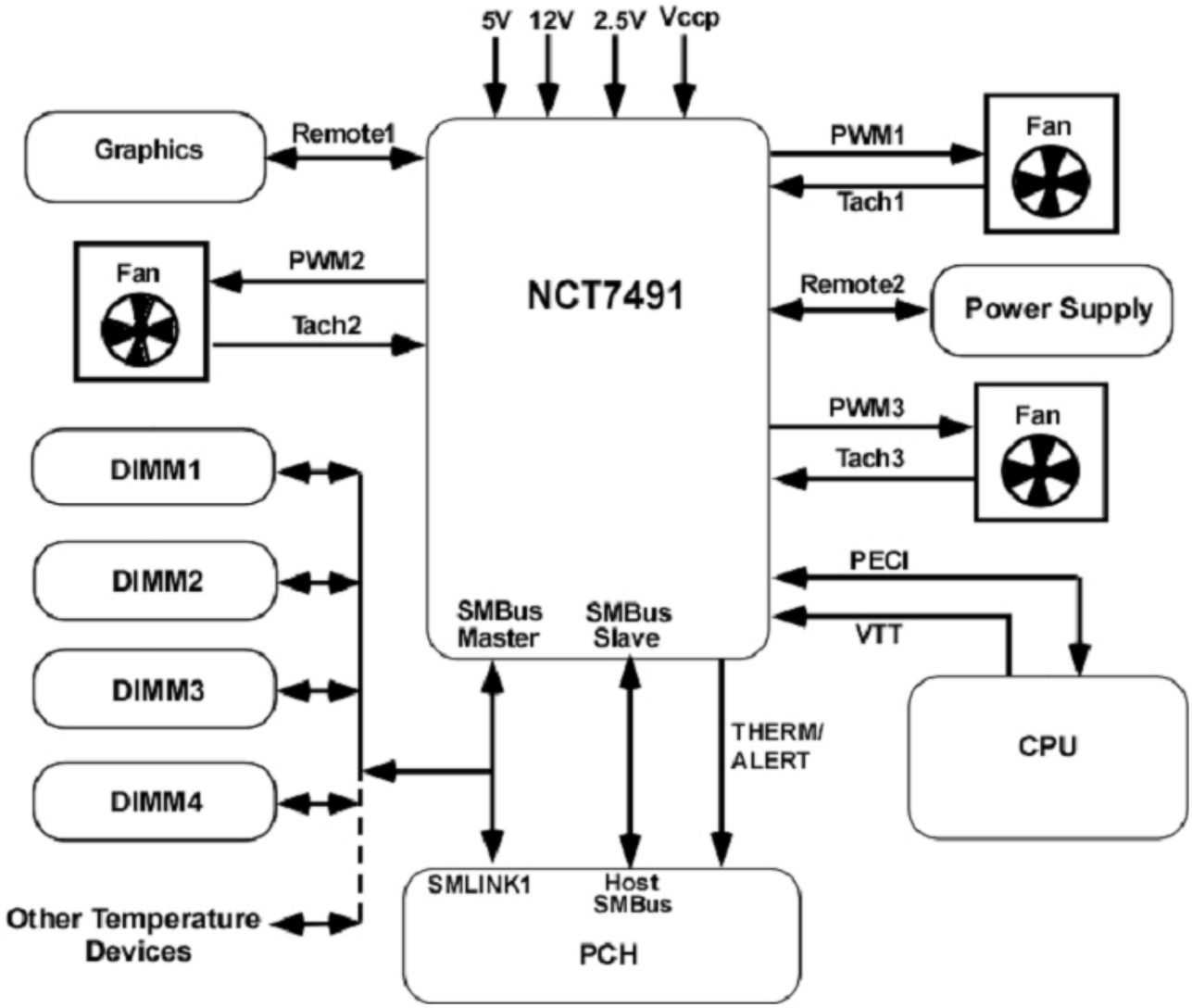

Figure 3. System Connection Diagram

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SMBUS SLAVE INTERFACE

Control of the NCT7491 is carried out using the serial system management bus (SMBus). The NCT7491 is connected to this bus as a slave device, under the control of a master controller. The NCT7491 has a 7−bit serial bus address. When the device is powered up with the ADDREN pin high, the NCT7491 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8−bit address.

If more than one NCT7491 is to be used in a system, each additional NCT7491 is placed in address select mode by strapping ADDREN low on power−up. The logic state of the ADDRESS SELECT pin then determines the device's SMBus address.

The device address is latched on the first valid SMBus transaction, more precisely on the low−to−high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. Any attempted changes in the address have no effect after this.

SMBus Addressing Options

Table 5. SETTING THE SMBUS ADDRESS

ADDREN pin state	ADDRESS SELECT pin state	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ pull−up)	0101101 (0x2D)
1	Don't care	0101110 (0x2E)

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low−to−high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master floats the data line high after the 10th clock rising edge to assert a stop condition. In read mode, the master device overrides the acknowledge bit by floating the data line high during the low period before the ninth clock pulse; this is known as No acknowledge. The master takes the data line low during the low period before the 10th clock rising edge, and then high afetr the 10th clock rising edge to assert a stop condition.

In the NCT7491, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation must contain a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 4. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

- If the NCT7491 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the NCT7491 as before, but only the data byte containing the register address is sent because no data is written to the register. This is shown in Figure 5.
  A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 6.
- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 6.

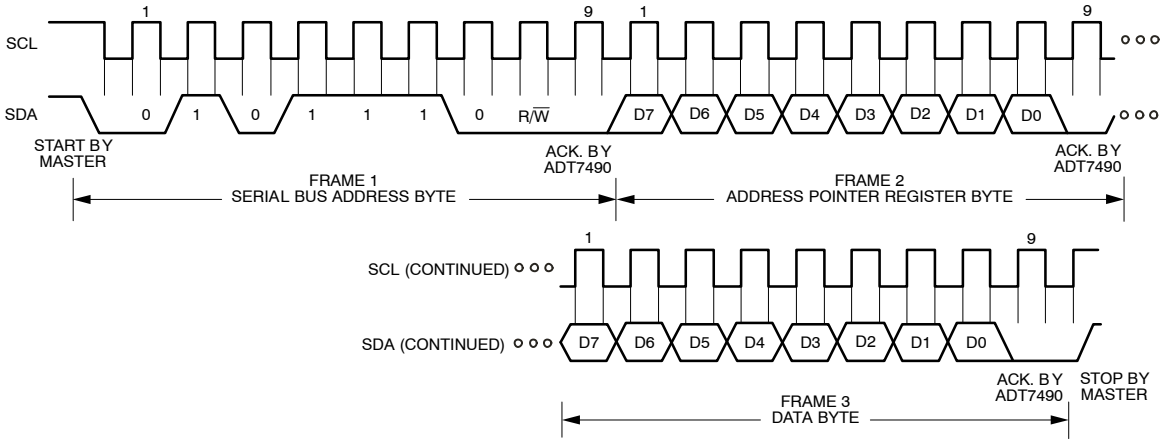

Figure 4. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

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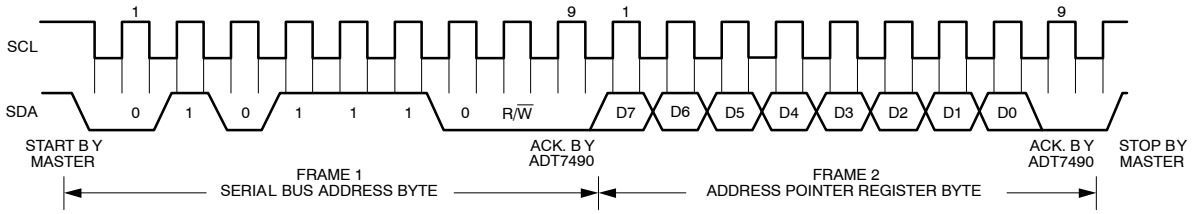

Figure 5. Writing to the Address Pointer Register Only

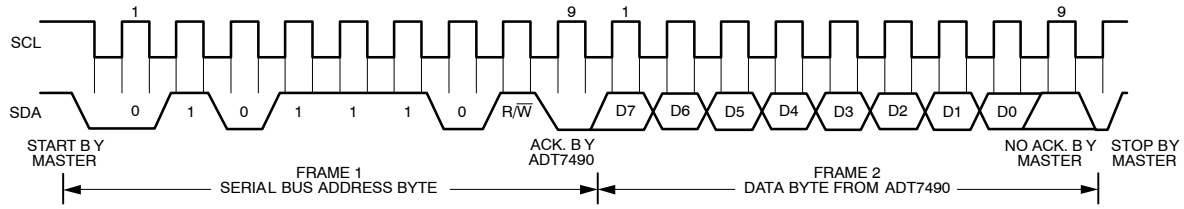

Figure 6. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the NCT7491 also supports the read byte protocol (see *System Management Bus Specifications Rev. 2* for more information; this document is available from the SMBus organization).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the NCT7491 are discussed here. The following abbreviations are used in the diagrams:

- S – Start
- P – Stop
- R – Read
- /$\overline{W}$ – Write
- A – Acknowledge
- /$\overline{A}$ – No acknowledge

The NCT7491 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NCT7491, the send byte protocol is used to write a register address to RAM for a subsequent single−byte read from the same address. This operation is illustrated in Figure 7.

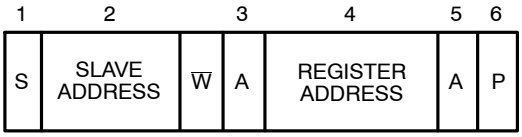

Figure 7. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single−byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

The byte write operation is illustrated in Figure 8.

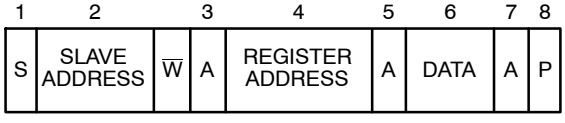

Figure 8. Single Byte Write to a Register

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Read Operations

The NCT7491 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must be previously set up. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the NCT7491, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 9.

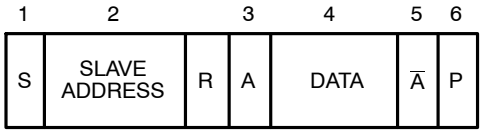

Figure 9. Single−Byte Read from a Register

ALERT RESPONSE ADDRESS

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The SMBALERT output can be used as either an interrupt output or an SMBALERT. One or more outputs can be connected to a common SMBALERT line connected to the master. If a device's SMBALERT line goes low, the following events occur:

1. SMBALERT is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose SMBALERT output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's SMBALERT output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the NCT7491 has responded to the alert response address, the master must read the status registers, and the SMBALERT is cleared only if the error condition is gone.

SMBus Timeout

The NCT7491 includes an SMBus timeout feature. If there is no SMBus activity for 25 ms, the NCT7491 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot work with the SMBus timeout feature, so it can be disabled.

Register 0x11 <4> TODIS = 0, SMBus timeout enabled (default). <4> TODIS = 1, SMBus timeout disabled.

Register Map Paging

The NCT7491 register map is organized into two pages:

- Page 1 contains register addresses 0x00 to 0xFF
- Page 2 contains register addresses 0x100 to 0x1FF

The default page on power up is page 1, so any SMBus read/writes to the NCT7491 will be to addresses in the range 0x00−0xFF.

To access page 2 of the register map, bit 0 (RGMP) of register 0xFF must be set to 1. Any subsequent read/writes after that bit is set will be to addresses in the range 0x100 to 0x1FF, e.g. reading from address 0x22 when RGMP is set will read from register 0x122. Bit 0 of register 0xFF is, in effect, the MSb of the address pointer. To return to page 1, bit 0 (RGMPCL) of register 0x1FF must be cleared to 0.

All register read/writes referenced in this document refer to registers on SMBus Page 1 unless stated otherwise.

ANALOG TEMPERATURE MEASUREMENT

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode connected transistor, measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the NCT7491 measures the change in V_{BE} when the device operates at four different currents.

Figure 10 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it can equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded but is linked to the base.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. C1 may be added as a noise filter (a recommended maximum value of 1000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section.

To measure ΔV_{BE}, the operating current through the sensor is switched among 4 currents, 2 x 2 related currents. As shown in Figure 10, N1 x I_1 is a multiple of I_1 and N2 x I_2 is a multiple of I_2. The currents through the temperature diode are switched between I and N1 x I, giving ΔV_{BE1}; and then between I and N2 x I, giving ΔV_{BE2}. The temperature is then calculated using the two ΔV_{BE} measurements. This method cancels the effect of any series resistance on the temperature measurement.

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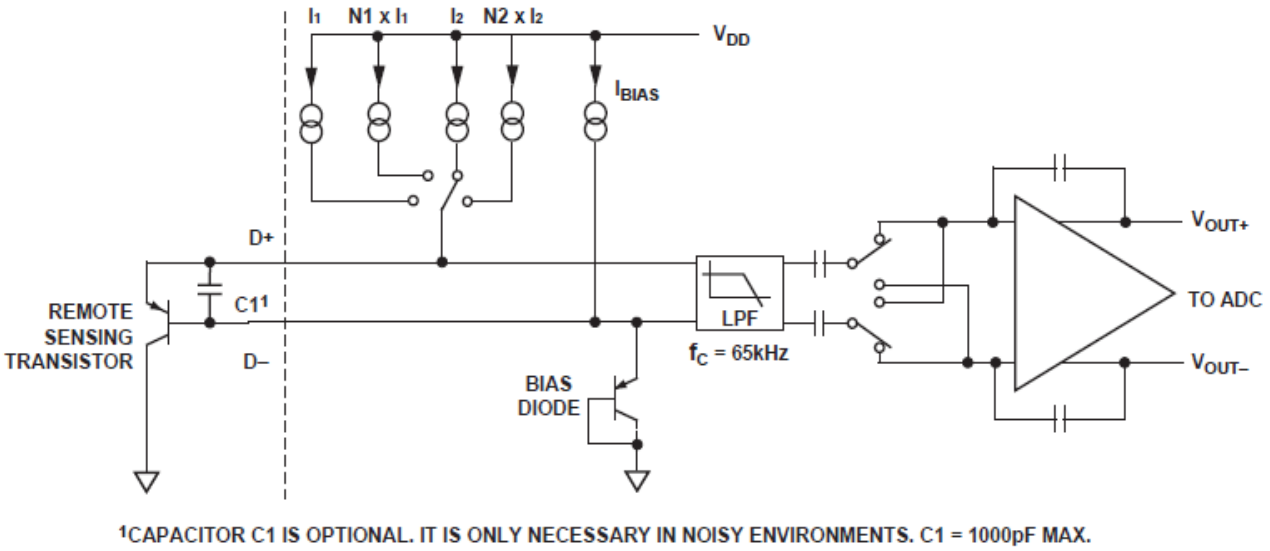

[1]CAPACITOR C1 IS OPTIONAL. IT IS ONLY NECESSARY IN NOISY ENVIRONMENTS. C1 = 1000pF MAX.

Figure 10. Analog Temperature Measurement Method

Series Resistance Cancellation

Parasitic resistance to the D+ and D− inputs to the NCT7491, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length and internal resistance in the CPU. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5 degree C offset per ohm of parasitic resistance in series with the remote diode.

The NCT7491 automatically cancels the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The NCT7491 is designed to automatically cancel typically up to 270 Ω of resistance in series with the thermal diode. By using an advanced temperature measurement method, this process is transparent to the user. This feature permits resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

Temperature Measurement Results

The results of the Local, Remote 1 and Remote 2 temperature measurements are stored in the local (0x26), remote 1 (0x25) and remote 2 (0x27) temperature value registers in two's complement format or Offset 64 format, depending on bit 0 if register 0x7C (1= 2's complement, 0 = Offset 64). These results are then compared with limits programmed into the local, remote 1 and remote 2 high and low limit registers. The high, low and THERM limits for the local, remote 1 and remote 2 channels must be in the same format as the temperature reading i.e. 2's complement or Offset 64.

All the temperature measurement data for each channel is stored in two registers, one for the MSB and one for the LSB. This gives the temperature measurement resolution of 0.25°C. When reading the full external temperature value, read the LSB first. This causes the MSB to be locked (that is, the ADC does not write to it) until it is read. This feature ensures that the results read back from the two registers come from the same measurement.

Theoretically, the temperature sensor and ADC can measure temperatures from −64°C to +127.5°C with a resolution of +0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the NCT7491 operating temperature range are not possible.

- Remote1 result registers: 0x25 (MSB), 0x77 bits <3:2> (2 LSb)
- Local result registers: 0x26 (MSB), 0x77 bits <5:4> (2 LSb)
- Remote1 result registers: 0x27 (MSB), 0x77 bits <7:6> (2 LSb)

Table 6. TWO'S COMPLEMENT FORMAT

Temperature	Digital Output (10−Bit)
−64°C	1100 0000 **00**
−55°C	1100 1001 **00**
−40°C	1101 1000 **00**
−10°C	1111 0110 **00**
−1°C	1111 1111 **00**
−0.25°C	1111 1111 **11**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25°C	0001 1001 **00**
125°C	0111 1101 **00**
127.5°C	0111 1111 **10**
Diode Fault – 127.75	0111 1111 **11**

NOTE: Bold numbers denote the LSB bits from extended resolution register 0x77.

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Offset 64 Format

In Offset 64 mode the range of values monitored is −64°C to 191.5°C (as opposed to −64°C to +127.5°C in 2's complement mode). To read the temperature in this format the user must subtract 64 from the value returned from the temperature register. Offset 64 mode is enabled by setting bit 0 if register 0x7C to zero.

Table 7. OFFSET64

Register Code	Temperature
0	−64°C
32	−32°C
64	0°C
100	36°C
255	191°C

Round Robin Temperature Measurement

The local and remote sensors are read in sequence in a continuous loop when monitoring is enabled (setting bit 0 of register 0x40). The user may decide which temperature channels are included in the monitoring loop using bits <2:0> in register 0x13.

- Setting <0> of register 0x13 includes the local channel in the monitoring loop.
- Setting <1> of register 0x13 includes the remote1 channel in the monitoring loop.
- Setting <2> of register 0x13 includes the remote2 channel in the monitoring loop.

Any channel not required in an application should be removed from the loop to reduce the overall monitoring time. Voltage channels may also be selected for the monitoring loop. See the Voltage Monitoring section for more information.

Temperature Averaging

The number of samples over which the temperature readings (and voltage readings) are averaged is set by bits <7:6> of register 0x40. The options are:

- 4 samples per averaged reading, <7:6> = <00>
- 8 samples per averaged reading, <7:6> = <01>
- 16 samples per averaged reading, <7:6> = <10>
- 32 samples per averaged reading, <7:6> = <11>

Averaging can be disabled for temperature readings by setting bit <4> of register 0x73.

Temperature Limits

Temperature limits can be set for each channel to detect an out of limit condition. These registers are programmed in the same format as the temperature reading, so if Offset64 mode is enabled then these registers must be programmed in that format, otherwise theay are programmed as 2's complement.

- Remote1 Low Limit register: 0x4E
- Remote1 High Limit register: 0x4F
- Local Low Limit register: 0x50
- Local High Limit register: 0x51
- Remote2 Low Limit register: 0x52
- Remote2 High Limit register: 0x53

Offset Registers

Offset errors can be introduced into the temperature measurements by clock noise or when the thermal diode is located away from the hot spot. To achieve the specified accuracy on this channel, these offsets must be removed.

The offset value is stored as an 8−bit, twos complement value. The value in the offset register is added to, or subtracted from, the measured value of the relevant temperature. The offset register has a default value of 0°C and has no effect unless the user writes a different value to it. The resolution of the value in the offset register is determined by bit 1 of register 0x7C. If the bit is 0 then the resolution is 0.5°C. If the bit is 1 then the resolution is 1°C.

- Remote1 Offset, register 0x70
- Local Offset, register 0x71
- Remote2 Offset, register 0x72

PUSH REGISTERS

The NCT7491 allows the user to program 4 temperatures into the device that can then be used for fan control and THERM/SMBALERT functions in the same way as other temperature sources. These temperatures can be written by the system SMBus master and should be programmed as 2's complement values.

- Push0, register 0xC8
- Push1, register 0xC9
- Push2, register 0xCA
- Push3, register 0xCB

Push Limit Registers

There are high, low and THERM limits associated with the Push channels. The same limits are applied to all 4 channels.

- Push Low Limit register, 0xCF
- Push High limit register, 0xCE
- Push THERM Limit register, 0xD0

Push Tmin/Trange Registers

The Push channels also have associated Tmin/Trange values for Automatic Fan Control. The hysteresis applied at the Tmin value can also be programmed.

- Push Tmin, 0xCC
- Push Trange, 0xCD bits <3:0>
- Push Hysteresis, 0xEB bits <3:0>

PECI 3.0 INTERFACE

The PECI 3.0 interface reads thermal data from the up to 4 CPUs located at PECI addresses between 0x30 and 0x37 (the first 4 addresses populated are used), and from 1 or 2 domains per CPU. The hottest reading from the domains for each CPU is stored in the PECI temperature registers. It can

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also write thermal data to the Package Configuration Space in the CPU. A PECI reading is a negative value, in degrees Celsius, which represents the offset from the thermal control circuit (T_{CC}) activation temperature. PECI information is returned as a 16−bit 2's complement value from which the 8−bit 2's complement value is derived. See the Platform Environment Control Interface (PECI) Specification from Intel for more details on the PECI data format. The PECI temperature stored for each CPU is an averaged value; the averaging window is user programmable.

The NCT7491 automatically detects the presence of a CPU at each of the supported addresses, and also detects the number of supported domains for each CPU. The presence of each CPU is indicated in the NCT7491 status registers.

On power up, the PECI interface will become active when the voltage measured on VTT is above 0.5 V and the voltage on Vccp is above 0.5 V. The returned CPU temperature will determine the behavior of the fans on power−up.

Thermal data that is collected by the NCT7491 (e.g. the DIMM temperatures) can be written to the CPU's Package Configuration Space (PCS) over the PECI 3.0 interface. This data can be used by the CPU to modify memory operations based on the DIMM temperature.

There are associated high and low limits for each PECI reading that can be programmed. The limit values take the same format as the PECI reading. Therefore, the programmed limits are not absolute temperatures but a relative offset in degrees Celcius from the TCC activation temperature. An out−of−limit event is recorded as follows:

- High Limit > comparison performed
- Low Limit ≤ comparison performed

An out−of−limit event is recorded in the associated status register and can be used to assert the SMBALERT pin.

A generic PECI 3.0 interface command structure is also available to allow an external master to issue any PECI 3.0 command in addition to the commands implemented by the NCT7491 monitoring loops.

PECI V_{TT} Input

The PECI V_{TT} voltage is used as the reference voltage for the PECI interface. This voltage must be connected to the NCT7491 in order for the PECI interface to be operational. The PECI V_{TT} input is also monitored by the NCT7491 and has associated high and low limits to allow out−of−limit detection on the V_{TT} channel. The valid operational voltage range for PECI V_{TT} is 0.85 V to 1.26 V.

PECI Startup Operation

On power up of the NCT7491 the PECI V_{TT} pin and the Vccp pin are monitored. If the voltage on both of these pins rises above 0.5 V then the NCT7491 will wait 5 ms and then automatically scan the PECI port to check for the presence of PECI 3.0 enabled processors. For any processors that are detected the PECI address, the domain count, the Tcontrol value and the Tjmax value will be read and stored in the NCT7491. The CPU count bits will be set (bits <7:6> of register 0x88). The PDET bit (bit <0> 0f register 0x37) will also be set to indicate that at least one CPU was detected. If any processors are detected then the PECI monitoring loop will automatically start.

The Vccp pin must be connected to an input voltage for the PECI interface to function correctly. If it is not connected to the CPU supply voltage then it should be connected to the NCT7491 supply voltage, Vcc. If the system processor does not support PECI 3.0 then the PECI monitoring loop will not automatically start. In that case the user can write to the PECI registers to manually configure the interface. The register descriptions are given below.

PECI Error Detection

The PECI 3.0 protocol includes FCS (Frame Check Sequence) bytes to guarantee data integrity. If there is a mismatch between the data and the FCS then a status bit indicates the communication failure (COMM status bit, register 0x43 bit <2>). PECI 3.0 also supports processor specific error codes to indicate error conditions relating to the temperature sensor within the processor (DATA status bit, register 0x43 bit <1>). These codes are shown in Table 8:

Table 8. DATA ERROR CODES

DATA code bits <6:4>, 0x43	DATA Error code	Description
<000>	0x8000	General Sensor Error
<001>	0x8002	Temperature below operational range
<010>	0x8003	Temperature above operational range

PECI Completion Code

Each read or write operation to the CPU Package Configuration Space returns a completion code to indicate the success or failure of the operation. The completion codes supported are shown in Table 9:

Table 9. COMPLETION CODES

Completion Code	Description
0x40	Command Passed, data is valid
0x80	Command timed out. Processor cannot generate required response in a timely fashion. Retry is appropriate.
0x81	Command timed out. Processor cannot allocate resources for the request. Retry is appropriate.
0x90	Unknown/Invalid/Illegal request
0x91	PECI Control hardware, firmware or associated logic error. The processor cannot process the request.

The completion code status bit in the NCT7491 (register 0x81 bit <0>) indicates the result of each read/write operation.

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PECI Registers

The registers relating to the operation of the PECI 3.0 interface are as follows:

Enabling the Interface:

- PECI Monitor, 0x40 bit 4

Setting PECI Monitor to 1 enables the PECI temperature monitoring loop. This will be automatically enabled on power up if the V_{TT} and V_{CCP} voltages have exceeded preset thresholds and any PECI 3.0 enabled processors have been automatically detected.

NOTE: The PDET bit (bit <0> 0x37) must also be set for correct operation.

Detected number of CPUs:

- CPU Count, 0x88 bits <7:6>
- PDET, 0x37 <0>

CPU Count indicates the number of populated CPUs. CPUs are automatically detected on power up by the NCT7491 and the number found is set here. The number can be overwritten by the user and sets the number of CPUs to be included in the temperature monitoring loop. The number of CPUs is 1 to 4, and the format is as shown in Table 10.

PDET is set if at least one PECI enabled processor is detected. If it is not automatically set then it must be set by the user.

Table 10. CPU COUNT

0x88 <7:6>	CPU Count
<00>	1
<01>	2
<10>	3
<11>	4

Domain Count bits:

- DOM0, 0x36 bit 3
- DOM1, 0x88 bit 5
- DOM2, 0x88 bit 4
- DOM3, 0x88 bit 3

These bits indicate the number of supported domains per CPU (0 = 1 domain, 1 = 2 domains). THE NCT7491 automatically detects these values on power up and sets the appropriate bits. They can be overwritten by the user.

PECI Interval:

- PECI Update Rate, 0x37 bits <5:4>

This determines the rate at which the PECI temperature registers are updated.

Table 11. UPDATE RATE

0x37 <5:4>	PECI Update Rate
<00>	1/sec
<01>	2/sec
<10>	5/sec
<11>	10/sec

PECI CPU Addresses:

- PECI0 CPU Address, 0x00
- PECI1 CPU Address, 0x01
- PECI2 CPU Address, 0x02
- PECI3 CPU Address, 0x03

These are the addresses used to access each CPU on the PECI interface and are automatically populated by the NCT7491 on power up. The values can be overwritten by the user.

PECI Temperature Values:

- PECI0 Temperature, 0x33
- PECI1 Temperature, 0x1A
- PECI2 Temperature, 0x1B
- PECI3 Temperature, 0x1C

These are the relative temperature values returned by the CPU. If a CPU is not populated then its associated temperature register can be written to by an external master. Data is tored in 2's complement format.

PECI Absolute Temperature Values:

- PECI0_Abs Temperature, 0x04
- PECI1_Abs Temperature, 0x05
- PECI2_Abs Temperature, 0x06
- PECI3_Abs Temperature, 0x07

These are the absolute CPU temperature values. They are automatically calculated by the NCT7491 from the relative temperature and the CPU T_{JMAX} value. See the **PECI T_{JMAX} Values** section. Data is stored in unsigned format.

Absolute PECI mode

The user can enable Absolute PECI mode by setting bit 2 of register 0x73 (ABS/REL) which will use the value stored in the PECI absolute temperature registers for fan control, THERM behaviour and SMBALERT behaviour rather than the relative PECI values.

PECI Averaging

The number of samples over which the PECI master will calculate an averaged temperature reading for each CPU can be set in register 0x36, bits <2:0>:

- <000> = No averaging
- <001> = Averaged over 2 samples
- <010> = Averaged over 4 samples
- <011> = Averaged over 8 samples
- <100> to <111> are reserved

PECI Offsets:

- PECI0 Offset, 0x94
- PECI1 Offset, 0x95
- PECI2 Offset, 0x96
- PECI3 Offset, 0x97

Offset values can be assigned to each temperature channel by programming these registers. The value programmed should be in 2's complement format. The resolution is 1°C.

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PECI Limits:

- PECI Low Limit, 0x34
- PECI High Limit, 0x35

These registers are used to set the allowable PECI temperature range. If the temperature is above the high limit or below the low limit then a status bit is set and pins configured as SMBALERT will assert. The high and low limit values are common to all PECI channels. The format depends on whether Absolute PECI mode is enabled. If it is then the limits are in unsigned format. If Absolute PECI mode is not enabled then the format is 2's complement.

PECI $T_{CONTROL}$ Values:

- PECI0 $T_{CONTROL}$, 0x3D
- PECI1 $T_{CONTROL}$, 0x08
- PECI2 $T_{CONTROL}$, 0x09
- PECI3 $T_{CONTROL}$, 0x0A

These values set the fail−safe fan assertion temperature. The response of the fans is determined by the THERM configuration registers and is described in the 'THERM Assertion' section of this document. These values can be read from the CPU via the PECI interface or programmed directly by the user.

The format depends on whether Absolute PECI mode is enabled. If it is then the limit is in unsigned format. If Absolute PECI mode is not enabled then the format is 2's complement.

PECI T_{JMAX} Values:

- PECI0 T_{JMAX} , 0x0B
- PECI1 T_{JMAX} , 0x0C
- PECI2 T_{JMAX} , 0x0D
- PECI3 T_{JMAX} , 0x0E

Each CPU has a maximum junction temperature T_{JMAX}. These values for the populated CPUs are read via the PECI 3.0 interface by the NCT7491. They can also be over−written by the user. They are used to determine the absolute PECI temperature. These values are stored as unsigned data.

PECI Fan Control:

- PECI Tmin, 0x3B
- PECI Trange, 0x3C bits <7:4>
- PWM1 Source1, 0x8A bits <6:3>
- PWM2 Source1, 0x8D bits <6:3>
- PWM3 Source1, 0x90 bits <6:3>

Tmin sets the turn−on temperature for any fan that is controlled by a PECI temperature.

Trange sets the range over which the PWM output will increase from PWMmin to PWMmax.

The PECI Tmin and PECI Trange values are common to all PECI channels.

The PWMX Source registers are used to assign temperature control to a fan. The PECI assignment is done with bits <6:3> in those registers.

The user can choose to use the relative or absolute PECI temperature values for fan control. If Absolute PECI mode is used then the maximum valid Tmin value is 175°C.

For full details on the Fan Control implementation see the 'Fan Control' section of this document

PECI Status Bits:

- PECI0 limit error, 0x43 bit 0
- PECI1 limit error, 0x81 bit 3
- PECI2 limit error, 0x81 bit 4
- PECI3 limit error, 0x81 bit 5
- DATA error, 0x43 bit 1
- COMM error, 0x43 bit 2
- DATA type, 0x43 bits <6:4>
- PECI completion code, 0x81 bit 0
- PECI0 $T_{CONTROL}$ exceeded, 0x89 bit 0
- PECI1 $T_{CONTROL}$ exceeded, 0x89 bit 1
- PECI2 $T_{CONTROL}$ exceeded, 0x89 bit 2
- PECI3 $T_{CONTROL}$ exceeded, 0x89 bit 3

The Data Type field indicates the returned code if a DATA error is generated. Status bits in 0x43 and 0x81 can be masked by setting the corresponding mask bits in registers 0x82 and 0x83.

Generic PECI Command Block

- CPU Address, 0xD1
- Data Write Length, 0xD2
- Data Read Length, 0xD3
- Data Write Buffer, 0xD4 to 0xE0
- Data Read Buffer, 0xE1 to 0xE9
- Generic PECI Configuration, 0xEA

These registers define the generic PECI interface. An external master can populate these registers in order to execute any supported PECI 3.0 commands.

The byte definitions for this block are as follows:

CPU Address sets the target address of the PECI client that is to be accessed.

Data Write Length sets the number of bytes to be transferred to the PECI client. This byte should include the AW FCS byte in its count. The AW FCS byte is automatically calculated and appended by the NCT7491.

Data Read Length sets the number of bytes to be returned from the PECI client.

Data Write Buffer is a 13 byte buffer that holds the data to be transferred to the client. The first byte of this buffer is the command code that defines the command to be executed.

Data Read Buffer is a 9 byte buffer that will hold the data returned from the client.

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The PECI Configuration 5 register (address 0xEA) enables the generic block and allows the command to be executed. The configuration bits are:

- AW, bit 1
- PEX, bit 2

Setting **AW** to 1 indicates that the transfer is an Assured Write transaction.

Setting **PEX** to 1 causes the NCT7491 to execute the command that has been set up in the generic command block. This bit will automatically clear when the transaction has completed.

If a communication error occurs when a Generic PECI command is sent then the GCOMM status bit is set. This bit can be masked.

- GCOMM, register 0x81 <2>
- GCOMM mask, register 0x83 <2>

SMBUS COMPATIBLE MASTER PORT

Thermal data is gathered from temperature monitoring devices attached to the SMBus Master port on the NCT7491. This port is used to automatically read temperature data from DIMM sensors, the PCH chipset sensor, graphics thermal sensors, or any thermal sensor with an SMBus interface. Up to 8 thermal slave devices are supported on the SMBus master port. The SMBus slave address for each device is user programmable. The register address of the thermal data within the slave device is also user programmable. This is assumed to be a 1−byte address so devices with a register address range of 0x00 to 0xFF are suitable. Each slave device has associated programmable configuration bits to indicate the protocol required to communicate over the SMBus and the temperature data format returned by the slave device. Status bits will indicate if any checksum errors arise from communicating with the slave devices.

The NCT7491 can be connected to the SMLINK1 port of the PCH to allow the PCH thermal data to be read. Data is automatically read from the PCH using the SMBus Block Read protocol. The device can be configured to read the DIMM temperature registers from the PCH.

The SMBus master and slave ports on the NCT7491 can be connected together if required.

Temperature readings returned from the thermal devices on the SMBus master port are available for use in the Automatic Fan Control algorithm.

The SMBus thermal devices have associated high and low temperature limit registers to allow out−of−limit conditions to be detected. If the SMBus Master interface is disabled then the SMBus master is internally connected to the slave interface, if the pins have not been assigned to GPIO functions. Enabling the SMBus master port overrides any GPIO1/GPIO2 configuration settings.

SMBus Compatible Master Registers

The registers relating to the control of the SMBus compatible master interface are as follows:

Enabling the SMBus Master port:

- SMBus Master Enable, 0xB5 bit 0

Setting this bit configures pins 5 and 6 on the QSOP package, or pins 2 and 3 on the QFN package as the SMBus Master Port. It also enables the Thermal slave temperature monitoring loop which will gather data from the devices configured in the SMBus Master Addressing table.

When this bit is 0 and pins 5 and 6 on the QSOP package, or pins 2 and 3 on the QFN package are not configured as GPIOs then the SMBus slave port is internally connected to the SMBus master port. This allows the master connected to the NCT7491 to communicate directly with devices that are on the NCT7491 master port.

Temperature Addressing Table:

- Device0 Address, 0x98
- Device0 Pointer, 0x99
- Device1 Address, 0x9A
- Device1 Pointer, 0x9B
- Device2 Address, 0x9C
- Device2 Pointer, 0x9D
- Device3 Address, 0x9E
- Device3 Pointer, 0x9F
- Device4 Address, 0xA0
- Device4 Pointer, 0xA1
- Device5 Address, 0xA2
- Device5 Pointer, 0xA3
- Device6 Address, 0xA4
- Device6 Pointer, 0xA5
- Device7 Address, 0xA6
- Device7 Pointer, 0xA7

The DeviceX Address register sets the 7−bit (R/W bit not included) SMBus address of the thermal sensor.

The DeviceX Pointer register sets the register address of the temperature data in the thermal slave device.

Device0 can be used for SMBus Block Read commands. In that case the block read command code should be written to the Device0 Pointer register. If the NCT7491 Master port is connected to the SMLINK1 port of the Intel PCH then the PCH temperature (and possibly the DIMM temperatures) can be read from this port. In that case Device0 should be reserved for the PCH temperature and Device1 to Device 4 reserved for DIMM0 to DIMM3.

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The NCT7491 will not attempt to read from a device that has a Device Address byte that is set to 0.

Temperature Values:

- Device0 (PCH), 0xA8
- Device1 (DIMM0), 0xA9
- Device2 (DIMM1), 0xAA
- Device3 (DIMM2), 0xAB
- Device4 (DIMM3), 0xAC
- Device5, 0xAD
- Device6, 0xAE
- Device7, 0xAF

The results of the readings from each of the thermal slave devices are stored here.

Thermal Slave Data Formats

It is necessary for the NCT7491 to be configured so that the data format for each SMBus client device is known, e.g. if the data is 2's Complement or unsigned data, or if a JEDEC standard SPD device is used so that the data can be correctly read from the device. Each SMBus device has a bit field to determine the data format for that device. The format selected for the device determines its behaviour for out−of−limit comparisons, THERM assertions and fan control operation. For Device0, if the format is set to PCH Block Read then the resulting data is stored as unsigned binary. The VR12 literal mode can be selected to allow temperature or power data be read from a VR12 controller via the PMBus.

Table 12. Device0 FORMATS

0xB2 <1:0>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	PCH block reads

Table 13. Device1 FORMATS

0xB2 <3:2>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 14. Device2 FORMATS

0xB2 <5:4>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 15. Device3 FORMATS

0xB2 <7:6>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 16. Device4 FORMATS

0xB3 <1:0>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 17. Device5 FORMATS

0xB3 <3:2>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	VR12 Literal

Table 18. Device6 FORMATS

0xB3 <5:4>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	VR12 Literal

Table 19. Device7 FORMATS

0xB3 <7:6>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	VR12 Literal

SMBus Master Update Rate

The interval between successive reads from an SMBus client device is determined by register 0xC7 bits <7:6>:

Table 20. SMBus UPDATE

0xC7 bits <7:6>	SMBus Update Rate
00	250 ms
01	500 ms
10	750 ms
11	1 sec

Thermal Slave Limits:

- SMB Slave High Limit, 0xC1
- SMB Slave Low Limit, 0xC2

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These registers are used to set the allowable Thermal slave temperature range. If the temperature is above the high limit or below the low limit then a status bit is set and pins configured as SMBALERT will assert. The high and low limit values are common to all SMBus Thermal slave readings. The low limit is programmed as a 2's Complement value. The high limit is programmed as an unsigned value. The difference between the two formats is necessary to cover the alternate formats available for the SMBus slave devices.

Thermal Slave THERM Value:

- SMBus THERM Limit, 0xC3

This value sets the fail−safe THERM assertion temperature. The response of the fans is determined by the THERM configuration registers and is described in the 'THERM Assertion' section of this document. This value is programmed as an 8−bit unsigned value.

Thermal Slave Fan Control:

- SMB Device Tmin, 0xC6
- SMB Device Trange, 0xC7 bits <3:0>
- PWM1 Source2, 0x8B
- PWM2 Source2, 0x8E
- PWM3 Source2, 0x91

Tmin sets the turn−on temperature for any fan that is controlled by a Thermal slave device. Trange sets the temperature range over which the PWM output will increase from PWMmin to PWMmax. The Tmin and Trange values apply to all Thermal slave devices. SMB Tmin is programmed as an 8−bit unsigned value. The maximum valid SMBus Tmin value is 175°C.

The PWMX Source registers are used to assign temperature control to a fan.

For full details on the Fan Control implementation see the 'Fan Control' section of this document.

SMBus Master Communication Settings

- Repeated Start Enable, 0xB0 bits <7:0>
- PEC Supported, 0xB1 bits <7:0>

The Repeated Start bits enable/disable the repeated start protocol for each device.

The PEC Supported bits can be set if an SMBus client device supports CRC−8 PEC. If this bit is set for a client device then the NCT7491 will read the PEC byte after the data and set the corresponding bit in the PEC status register (0xB7) if the PEC byte is incorrect.

DIMM Temperatures from PCH

- Read DIMM from PCH, 0xB5 bit 7

If this bit is set to 1 then the SMBus master port will read the DIMM registers from the SMLINK1 port of the PCH and store the results in registers 0xA9 to 0xAC. If it is 0 then it will read DIMM temperatures from SMBus slave devices.

DIMM Temperatures from Remote Sensors

- DIMM 0/1 from Remote1, 0xB5 bit 5
- DIMM 2/3 from Remote2, 0xB5 bit 6

If 0xB5 <5> is 1 then registers 0xA9 and 0xAA are overwritten by the Remote1 temperature reading.

If 0xB5 <6> is 1 then registers 0xAB and 0xAC are overwritten by the Remote2 temperature reading.

If bit 7 of 0xB5 (DIMM from PCH) is set then bits 5 and 6 have no effect.

Writing DIMM temperatures to the CPUs

The DIMM temperatures collected from SPD devices, from the PCH or from the analog thermal sensors can be automatically written to the CPU via PECI. To enable this function set the PWEN bit, register 0x37 <7>. The temperatures written will be the maximum DIMM temperature for each CPU.

DIMM CPU assignments:

- DIMM0 CPU, 0x0F bits <1:0>
- DIMM1 CPU, 0x0F bits <3:2>
- DIMM2 CPU, 0x0F bits <5:4>
- DIMM3 CPU, 0x0F bits <7:6>

These bits set the CPU associated with each DIMM. This information is necessary in order for the PECI loop to program the maximum DIMM temperature for each CPU.

Selecting DIMMs To Be Written

Each DIMM register can be enabled to be written to the CPU individually. This is done in register 0x87 bits <7:4>. If a DIMM is not populated then the corresponding bit in this register should be set to zero:

Setting 0x87 bit <4> to 1 includes DIMM0 in the PECI write

Setting 0x87 bit <5> to 1 includes DIMM1 in the PECI write

Setting 0x87 bit <6> to 1 includes DIMM2 in the PECI write

Setting 0x87 bit <7> to 1 includes DIMM3 in the PECI write

SMBus Thermal Slave Error Response

How the NCT7491 responds to errors on the SMBus master port can be configured in the following ways:

- SMBus Retry Interval, 0x10 bits <4:3>
- PWM1 Response, 0x11 bit 5
- PWM2 Response, 0x11 bit 6
- PWM3 Response, 0x11 bit 7

SMBus Retry Interval: If an error is encountered when communicating with a Thermal slave device then the NCT7491 will attempt to carry out the command up to 3 times. These bits set the interval between the retry attempts.

Table 21. SMBUS ERROR RETRY TIMES

0x10 bits <4:3>	SMBus Retry Interval
00	1 ms
01	2 ms
10	4 ms
11	8 ms

If the device fails 3 consecutive read attempts then the PWMx Response bits determine the fan behaviour.

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- If bit 5 of 0x11 is 1 then PWM1 will go to 100% duty or Max duty. If bit 5 is 0 then the error is ignored.
- If bit 6 of 0x11 is 1 then PWM2 will go to 100% duty or Max duty. If bit 6 is 0 then the error is ignored.
- If bit 7 of 0x11 is 1 then PWM3 will go to 100% duty or Max duty. If bit 7 is 0 then the error is ignored.

Whether the PWM outputs go to 100% or Max duty is determined by bits <4:2> of register 0x16. See the **THERM ASSERTION** section of this document for more details.

SMBus Master Status Registers

- Bad Block read byte count, 0x81 bit 6
- NACK bits, 0xB6 bits <7:0>
- PEC error bits, 0xB7 bits <7:0>
- SMBus Timeout bits, 0xB8 bits <7:0>
- High/Low Limit exceeded bits, 0xB9 bits <7:0>
- PCH Data Invalid, 0xBA bits <4:0>
- THERM Limit exceeded, 0xBB bits <7:0>

Bad Block Read Count will assert if the byte count returned by the block read command is insufficient to read the required temperatures.

NACK bits will assert if a device does not acknowledge its SMBus address.

PEC error bits will assert if the PEC byte is incorrect.

SMBus Timeout bits will assert if the bus is locked.

High/Low Limit bits will assert if the temperature returned is at or below the programmed low limit value.

PCH Data Invalid bits will assert if the PCH returns reserved temperature codes

THERM Limit bits will assert if the returned temperature is greater than the programmed THERM limit

The status bits ((except THERM status) will hold their value until the registers are read through the SMBus slave port. Status bits (except THERM status) can be masked by setting the corresponding bits in registers 0xBB to 0xBF. THERM Limit status bits will automatically clear when the temperature is below the SMBus THERM limit, unless THERM hysteresis is enabled (setting bit 0 of register 0x11) in which case the temperature must drop below THERM limit – Hysteresis.

AUTOMATIC FAN CONTROL

There are two automatic fan control methods that can be selected in the NCT7491. Each PWM channel can be set to use the Tmin/Trange control method or to use an 8 point PWM Look–Up Table. In both cases one or more temperature channels can be assigned to control each PWM output.

Assigning Temperature Zones for Automatic Fan Control

These registers allow the temperature zone to be assigned to a PWM channel by setting the appropriate bit. Any combination of temperature zones can be assigned to control any fan. If more than one zone is selected then a PWM value will be calculated for each temperature and the highest calculated PWM value will be output. If no temperature sources are selected then the associated PWM channel defaults to manual mode.

Registers for assigning zones to PWM1:

- Local/Remote1/Remote2 Control, 0x8A bits <2:0>
- PECI Control, 0x8A, bits <6:3>
- SMBus Thermal Slave Control, 0x8B bits <7:0>
- Push Temperature Control, 0x8C bits <3:0>

Registers for assigning zones to PWM2:

- Local/Remote1/Remote2 Control, 0x8D bits <2:0>
- PECI Control, 0x8D, bits <6:3>
- SMBus Thermal Slave Control, 0x8E bits <7:0>
- Push Temperature Control, 0x8F bits <3:0>

Registers for assigning zones to PWM3:

- Local/Remote1/Remote2 Control, 0x90 bits <2:0>
- PECI Control, 0x90, bits <6:3>
- SMBus Thermal Slave Control, 0x91 bits <7:0>
- Push Temperature Control, 0x92 bits <3:0>

For example if the user wants to control PWM1 from the hottest of the CPU temperature, PCH temperature and the Remote1 sensor then the Control Source registers would be programmed as:

- 0x8A <3> = 1 (PECI0)
- 0x8A <1> = 1 (Remote1)
- 0x8B <0> = 1 (SMBus Device 0, PCH)

Tmin/Trange Automatic Fan Control

The PWM channels can be put into Tmin/Trange in the following way:

- Setting bit <0> of register 0x10 to 0 puts PWM1 in Tmin/Trange mode
- Setting bit <1> of register 0x10 to 0 puts PWM2 in Tmin/Trange mode
- Setting bit <2> of register 0x10 to 0 puts PWM3 in Tmin/Trange mode

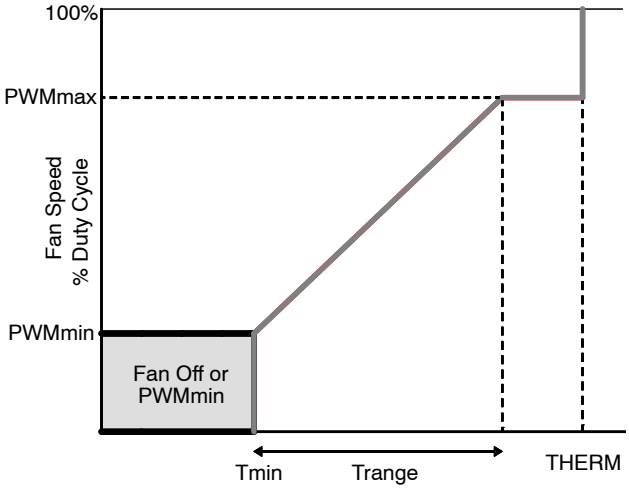

Figure 11. PWM Control Curve in Tmin/Trange Mode

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The control loop behaviour in Tmin/Trange mode is determined by the Tmin, PWMmin, Trange and PWMmax values. Tmin sets the temperature at which the fan turns on and PWMmin is the PWM value at Tmin. Trange sets the temperature range over which the PWM output increases from PWMmin to PWMmax. These settings set the slope of the curve. Each temperature source has its own associated Tmin/Trange values. The THERM limit associated with the temperature channel can override the fan control curve if a THERM event occurs.

Minimum PWM values:

- PWM1 Minimum Duty, 0x64
- PWM2 Minimum Duty, 0x65
- PWM3 Minimum Duty, 0x66

These set the lowest PWM at which the fan will run. One Lsb equals 0.39% duty cycle. Minimum PWM values only apply in Tmin/Trange mode.

Maximum PWM values:

- PWM1 Maximum Duty, 0x38
- PWM2 Maximum Duty, 0x39
- PWM3 Maximum Duty, 0x3A

These set the maximum duty at which the fans will run. THERM assertions can be configured to over−ride this to allow the fans to go to 100% duty on a THERM event. See the **THERM ASSERTION** section for more details.

PWM duty cycle registers:

- PWM1 Duty, 0x30
- PWM2 Duty, 0x31
- PWM3 Duty, 0x32

The current duty cycle calculated by the control loop can be read in these registers. If the PWM channel is not associated with a temperature zone then that channel's duty cycle register will become writeable (manual mode).

Tmin/Trange values for all Temperature Sources:

- PECI Tmin. 0x3B
- PECI Trange, 0x3C bits <7:4>
- Remote1 Tmin, 0x67
- Remote1 Trange, 0x5F bits <7:4>
- Local Tmin, 0x68
- Local Trange, 0x60 bits <7:4>
- Remote2 Tmin, 0x69
- Remote2 Trange, 0x61 bits <7:4>
- SMBus slave Tmin, 0xC6
- SMBus slave Trange, 0xC7 bits <3:0>
- Push temperature Tmin, 0xCC
- Push temperature Trange, 0xCD bits <3:0>

PECI Tmin

PECI Tmin values must be programmed in the same format selected for PECI fan control (selected by bit 2 of register 0x73). If relative mode is selected then Tmin is programmed in 2's Complement format. If absolute mode is selected then Tmin is programmed as an unsigned value. If Absolute PECI mode is used then the maximum valid Tmin value is 175°C.

Analog Sensor Tmin

The Tmin value for the analog sensors (Remote1/ Remote2/Local) must be written in the same format as the measurement registers, i.e. if they are in Offset 64 format then the Tmin value for these channels must also be written in Offset 64 format. If they are in 2's Complement format then Tmin must be written in the range 0°C to 127°C.

SMBus Tmin

The SMBus Tmin value should be programmed as an unsigned 8−bit value in the range 0°C to 175°C.

Push Tmin

The Push register Tmin value should be programmed as a value in the range 0°C to 127°C.

Tmin Hysteresis

Hysteresis can be applied to the Tmin temperature to prevent the fan from turning on and off rapidly around Tmin. Each temperature has its own hysteresis value that can be applied. The range of possible values is 0°C to 15°C.

Table 22. HYSTERESIS REGISTERS

Temperature	Hystersis
Remote1	Register 0x6D <7:4>
Local	Register 0x6D <3:0>
Remote2	Register 0x6E <7:4>
PECI	Register 0x6E <3:0>
SMBus slave	Register 0xB5 <4:1>
Push registers	Register 0xEB <3:0>

PWM Behaviour below Tmin:

- PWM1 on below Tmin, 0x62 bit 5
- PWM2 on below Tmin, 0x62 bit 6
- PWM3 on below Tmin, 0x62 bit 7

Setting these bits to 1 will cause the associated PWM output to remain at the minimum PWM value rather than shut off when the control temperature is below its Tmin value minus hysteresis. This setting applies to both Tmin/Trange mode and to Look−Up Table mode.

Trange Values

The Trange values determine the temperature range over which the fan control curve will increase from the PWM minimum value to the PWM maximum value associated with the PWM output.

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The 4−bit Trange values that can be assigned for each channel are shown in the following table:

Table 23. TRANGE OPTIONS

Trange Bit Field	Trange Value
0000	2°C
0001	2.5°C
0010	3.33°C
0011	4°C
0100	5°C
0101	6.67°C
0110	8°C
0111	10°C
1000	13.33°C
1001	16°C
1010	20°C
1011	26.67°C
1100	32°C
1101	40°C
1110	53.33°C
1111	80°C

Enabling Enhanced Acoustics on the PWM Outputs:

- PWM1 Max Ramp Rate, 0x62 bits <2:0>
- PWM1 enable acoustics, 0x62 bit 3
- PWM2 Max Ramp Rate, 0x63 bits <6:4>
- PWM2 enable acoustics, 0x63 bit 7
- PWM3 Max Ramp Rate, 0x63 bits <2:0>
- PWM3 enable acoustics, 0x63 bit 3

These settings allow the user to limit the rate at which the PWM output changes whenever the fan control loop calculates a new value. As this prevents instant changes in PWM the acoustic response of the system is improved. These settings apply to both Tmin/Trange mode and to Look−Up Table mode.

Table 24. ENHANCED ACOUSTICS TIMES

Ramp Rate code	Settling time
000	31.75 sec
001	15.7 sec
010	10.5 sec
011	6.33 sec
100	4 sec
101	2.66 sec
110	1.28 sec
111	0.75 sec

Setting the PWM Frequency

Each PWM output can be set to high frequency PWM mode or low frequency PWM mode. In high frequency mode the output will run at 22 kHz. In low frequency mode the frequency can be selected for each PWM output.

Setting bit <3> of register 0x5F to 1 enables high frequency for PWM1

Setting bit <3> of register 0x60 to 1 enables high frequency for PWM2

Setting bit <3> of register 0x61 to 1 enables high frequency for PWM3

If low frequency is enabled (if bit <3> in 0x5F, 0x60 or 0x61 is 0) then the frequency is set as follows:

Table 25. LOW FREQUENCY PWM SELECTION

0x5F, 0x60 or 0x61 bits <2:0>	Frequency
000	11.0 Hz
001	14.7 Hz
010	22.1 Hz
011	29.4 Hz
100	35.3 Hz
101	44.1 Hz
110	58.8 Hz
111	88.2 Hz

Look−Up Table Automatic Fan Control

In this mode the selected PWM output is controlled by an 8−point look−up table, where a temperature and PWM value is programmed for each point. Each channel has its own control table. Any combination of temperature sources can be assigned to control the PWM output. When more than one channel is assigned to control a PWM output in this mode the channel that is the hottest will control the output. The exception to this is if PECI relative temperatures are assigned to contol a channel. Since PECI relative values are always negative they cannot be combined with other channels, since the other channels would always dominate due to the fact that they are positive values. To allow PECI readings to be combined with other readings the user can set bit 2 of register 0x73 (ABS/REL). This will cause the absolute PECI readings to be used for fan control, rather than the relative readings.

- If relative PECI readings are assigned for fan control then the control temperature values for that PWM channel must be programmed in negative 2's complement format (−128°C to 127°C).
- If any temperature source other than relative PECI is assigned for fan control (including absolute PECI readings) then the control temperatures for that PWM channel must be programmed in unsigned format (0°C to 255°C).

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- PWM values are programmed in the range 0x00 to 0xFF. The resolution for this register is 1 lsb = 0.392%.

The NCT7491 linearly interpolates between the programmed points. It is not necessary to program all 8 points. If fewer than 8 points are required then the user should program from the lowest to the highest required control temperature and set the unused control temperatures to the maximum value (0x00 if relative PECI is assigned, 0xFF if the PWM channel is controlled by any other temperature source).

- Setting bit <0> of register 0x10 to 1 puts PWM1 in Look−up Table mode
- Setting bit <1> of register 0x10 to 1 puts PWM2 in Look−up Table mode
- Setting bit <2> of register 0x10 to 1 puts PWM3 in Look−up Table mode

The registers used for setting the control temperatures and PWMs for each channel are on page 2 of the register map. To access these registers the user must first set bit 0 of register 0xFF to 1. This will set the register page to page 2. When programming the table is complete the user should clear bit 0 of register 0xFF to zero to return to page 1 of the register map.

Table 26. PWM1 LOOK−UP TABLE VALUES

PWM1 Control Points	Temperature Address	PWM Address
PWM1 Control Point 1	0x00 (0x100)	0x01 (0x101)
PWM1 Control Point 2	0x02 (0x102)	0x03 (0x103)
PWM1 Control Point 3	0x04 (0x104)	0x05 (0x105)
PWM1 Control Point 4	0x06 (0x106)	0x07 (0x107)
PWM1 Control Point 5	0x08 (0x108)	0x09 (0x109)
PWM1 Control Point 6	0x0A (0x10A)	0x0B (0x10B)
PWM1 Control Point 7	0x0C (0x10C)	0x0D (0x10D)
PWM1 Control Point 8	0x0E (0x10E)	0x0F (0x10F)

Table 27. PWM2 LOOK−UP TABLE VALUES

PWM2 Control Points	Temperature Address	PWM Address
PWM2 Control Point 1	0x10 (0x110)	0x11 (0x111)
PWM2 Control Point 2	0x12 (0x112)	0x13 (0x113)
PWM2 Control Point 3	0x14 (0x114)	0x15 (0x115)
PWM2 Control Point 4	0x16 (0x116)	0x17 (0x117)
PWM2 Control Point 5	0x18 (0x118)	0x19 (0x119)
PWM2 Control Point 6	0x1A (0x11A)	0x1B (0x11B)
PWM2 Control Point 7	0x1C (0x11C)	0x1D (0x11D)
PWM2 Control Point 8	0x1E (0x11E)	0x1F (0x11F)

Table 28. PWM3 LOOK−UP TABLE VALUES

PWM3 Control Points	Temperature Address	PWM Address
PWM3 Control Point 1	0x20 (0x120)	0x21 (0x121)
PWM3 Control Point 2	0x22 (0x122)	0x23 (0x123)
PWM3 Control Point 3	0x24 (0x124)	0x25 (0x125)
PWM3 Control Point 4	0x26 (0x126)	0x27 (0x127)
PWM3 Control Point 5	0x28 (0x128)	0x29 (0x129)
PWM3 Control Point 6	0x2A (0x12A)	0x2B (0x12B)
PWM3 Control Point 7	0x2C (0x12C)	0x2D (0x12D)
PWM3 Control Point 8	0x2E (0x12E)	0x2F (0x12F)

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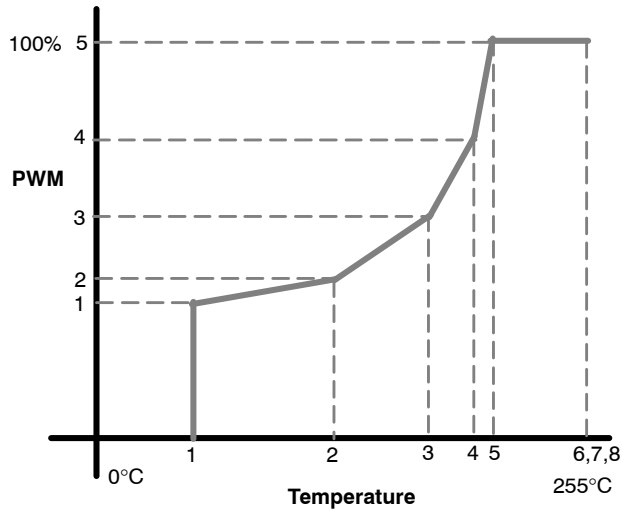

Figure 12.

Figure 12 shows a typical look−up table curve. The temperatures are programmed as unsigned data. In this example 5 of the 8 control points are used and the remaining 3 are set to the maximum value of 255°C. This curve applies if relative PECI values are not assigned to control the PWM channel.

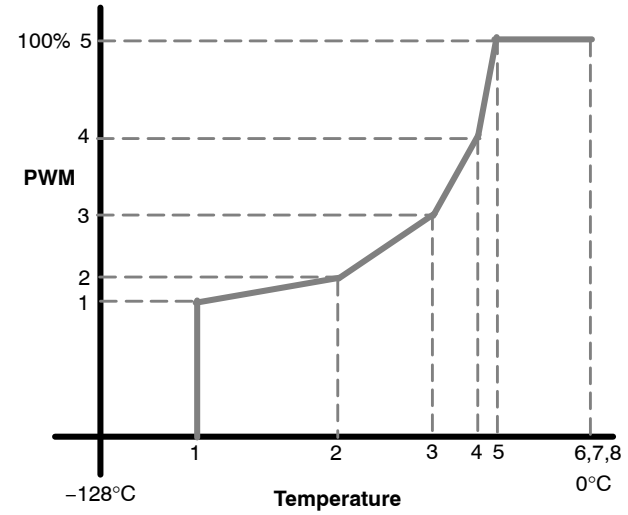

Figure 13.

Figure 13 shows a typical look−up table curve that applies when relative PECI values are assigned to control the PWM channel. The temperatures are programmed as negative 2's complement values. In this example 5 of the 8 control points are used and the remaining 3 are set to the maximum value of 0°C, as this is the maximum value for relative PECI values.

FAN OVERRIDE SETTINGS

There are bits in the NCT7491 that allow the PWM outputs to be overdriven so that the outputs go to maximum speed (as programmed in the maximum PWM registers), to go to full speed (100% duty) or to be shut off. These bits will override all other fan control settings.

- Setting bit 1 of register 0x11 to 1 runs the fans at the maximum programmed PWM duty cycle
- Setting bit 3 of register 0x40 to 1 runs the fans at 100% duty cycle. This bit has precedence over all others.
- Setting bit 0 of register 0x87 to 1 turns off PWM1
- Setting bit 1 of register 0x87 to 1 turns off PWM2
- Setting bit 2 of register 0x87 to 1 turns off PWM3

THERM Override

Setting bit 5 of register 0x40 will allow assertions on any pin configured as a THERM pin to drive the fans to 100% duty cycle or Max PWM, deending on bits <4:2> of register 0x16. This will override all other fan settings. This allows an external device to bypass the register settings of the NCT7491 for fail safe operation.

FAN DRIVE

The NCT7491 uses pulse width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4−wire fans, the PWM drive may need only a pullup resistor. In many cases the 4−wire fan PWM input has an internal pullup resistor. The NCT7491 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are used for 3−wire fans, while the high frequency option is usually used with 4−wire fans. For 3−wire fans, a single N−channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven and the input capacitance of the FET. Because a 10 k (or greater) resistor must be used as a PWM pullup, an FET with large input capacitance can cause the PWM output to become distorted and adversely affect the fan control range. This is a requirement only when using high frequency PWM mode. Typical notebook fans draw a nominal 170 mA, therefore, SOT devices can be used where board space is a concern. In desktops, fans typically draw 250 mA to 300 mA each. If several fans are driven in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, VGS < 3.3 V, for direct interfacing to the PWM output pin.

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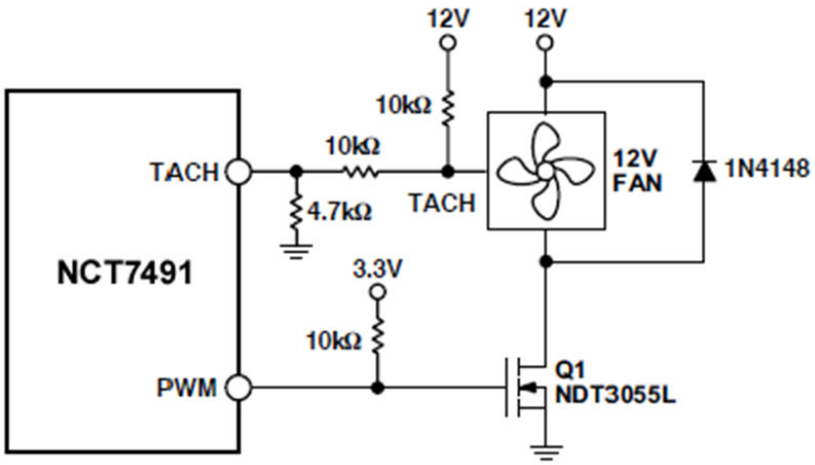

Figure 14. Driving a 3−Wire Fan Using an N−Channel MOSFET

Figure 14 uses a 10 k pullup resistor for the TACH signal. This assumes that the TACH signal is an open−collector from the fan. In all cases, the TACH signal from the fan must be kept below 3.6 V maximum to prevent damaging the NCT7491.

Figure 15 shows a fan drive circuit using an NPN transistor such as a general purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements. Ensure that the base resistor is chosen so that the transistor is saturated when the fan is powered on.

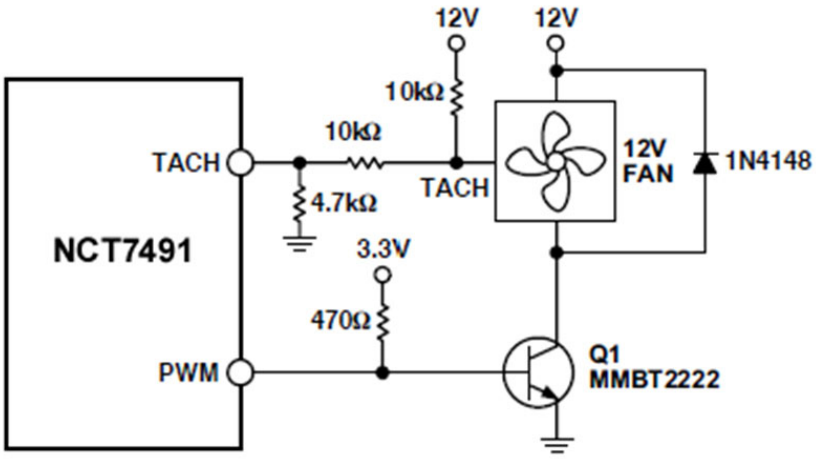

Figure 15. Driving a 3−Wire Fan Using an NPN Transistor

Because the fan drive circuitry in 4−wire fans is not switched on or off, as with previous PWM driven/powered fans, the internal drive circuit is always on and uses the PWM input as a signal instead of a power supply. This enables the internal fan drive circuit to perform better than 3−wire fans, especially for high frequency applications. Figure 16 shows a typical drive circuit for 4−wire fans.

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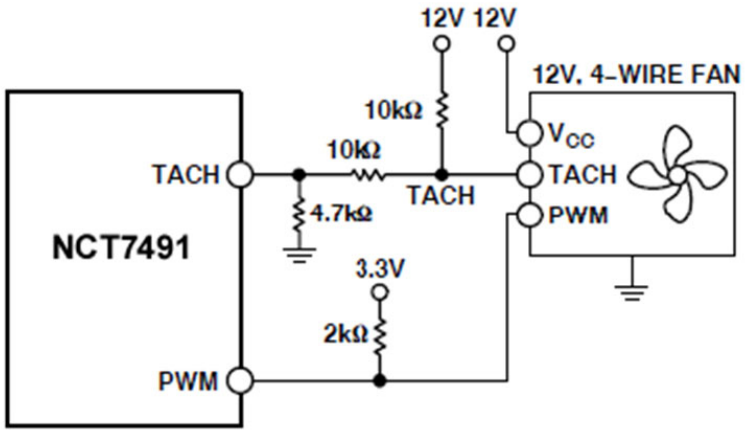

Figure 16. Driving a 4−Wire Fan

Driving Two Fans from PWM3

The NCT7491 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 17 shows how to drive two fans in parallel using a MOSFET. Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure the PWM outputs are not required to source current, and that they sink less than the 5 mA maximum current specified in the data sheet.

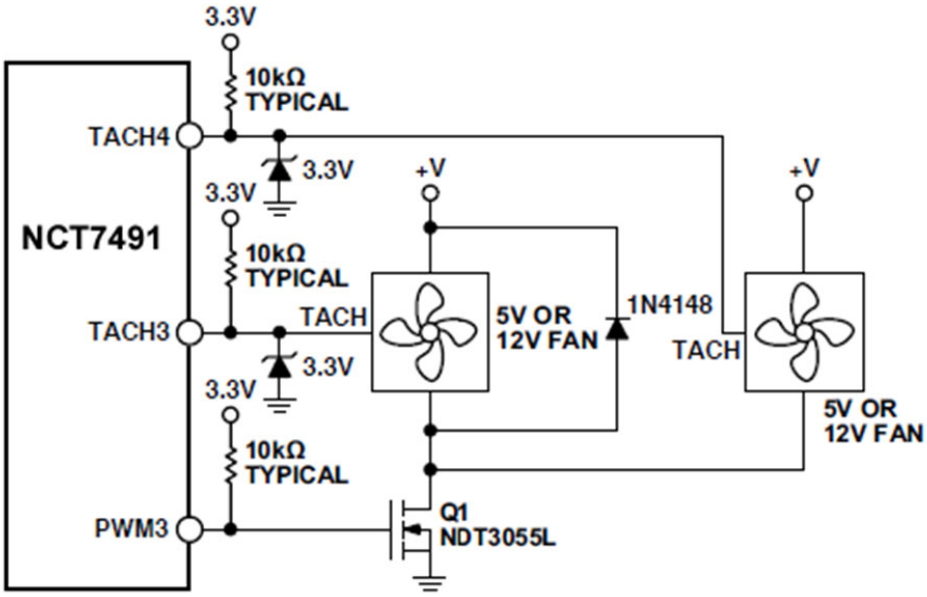

Figure 17. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N−Channel MOSFET

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3, so PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry looks the same, as shown in Figure 17. The SYNC bit in Register 0x62 enables this function. Synchronization is not required in high frequency mode when used with 4−wire fans.

Setting bit 4 of register 0x62 (SYNC) to 1 synchronizes TACH2, TACH3, and TACH4 to PWM3.

TACH Inputs

Pins 9, 11, 12 and 14 on the QSOP package or pins 6, 8, 9 and 11 on the QFN package (when configured as TACH inputs) are high impedance inputs intended for fan speed measurement. Signal conditioning in the NCT7491

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accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 3.6 V, even though VCC is 3.3 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 3.6 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range. Figure 18 to Figure 20 show circuits for the most common fan TACH outputs. If the fan TACH output has a resistive pullup to VCC, it can be connected directly to the fan input, as shown in Figure 18.

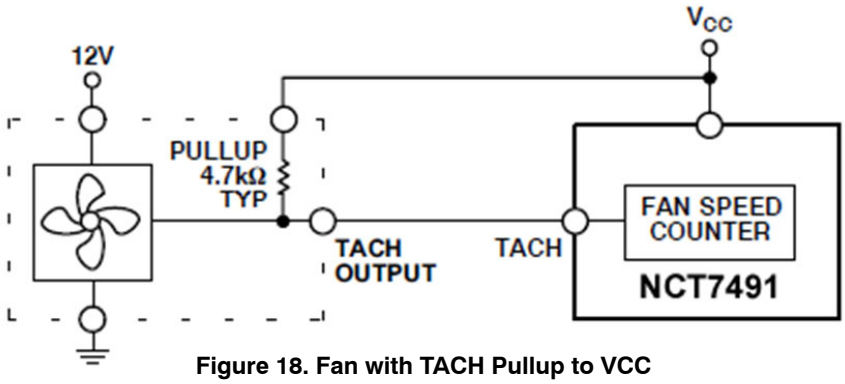

Figure 18. Fan with TACH Pullup to VCC

If the fan output has a resistive pullup to 12 V, or other voltage greater than 3.6 V, the fan output can be clamped with a zener diode, as shown in Figure 19. The zener diode voltage should be chosen so that it is greater than VIH of the TACH input but less than 3.6 V, allowing for the voltage tolerance of the zener. A value of between 3.0 V and 3.6 V is suitable.

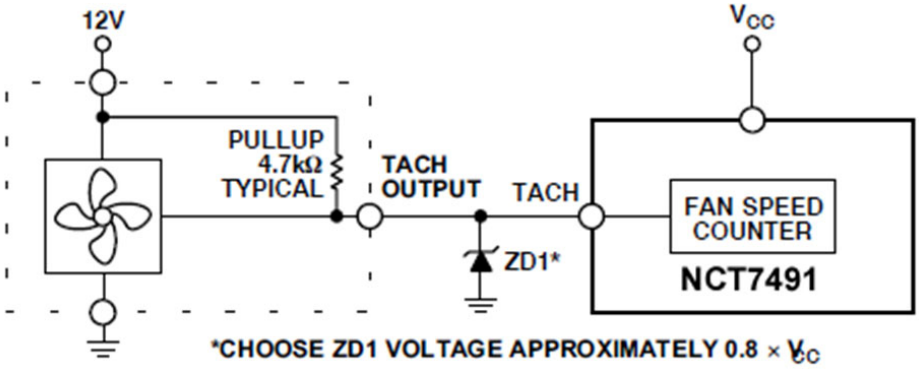

Figure 19. Fan with TACH Pullup to Voltage > 3.6 V, for Example, 12 V Clamped with Zener Diode

If the fan has a strong pullup (less than 1 k_) to 12 V or a totem−pole output, a series resistor can be added to limit the zener current, as shown in Figure 20.

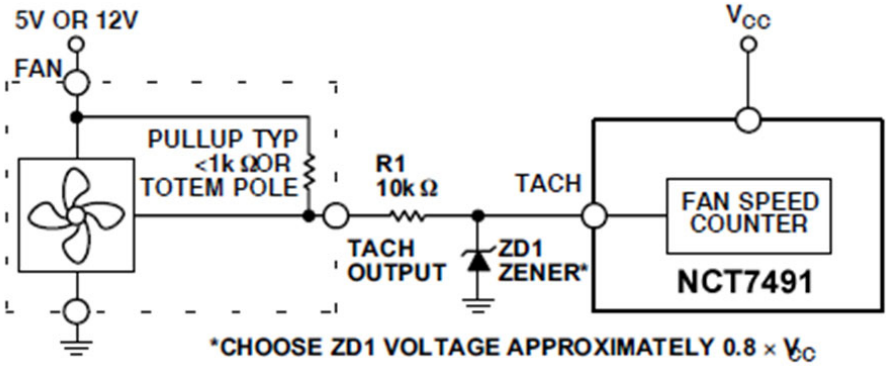

Figure 20. Fan with Strong TACH Pullup to >VCC or Totem−Pole Output, Clamped with Zener Diode and Resistor

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TACH Measurement Overview

The fan counter does not count the fan TACH output pulses directly because the fan speed could be less than 1000 RPM, and it takes several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on−chip 78 kHz oscillator into the input of a 16−bit counter for N periods of the fan TACH output (see Figure 21) so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed. N, the number of pulses counted, is determined by the settings of the TACH pulses per revolution register (0x7B). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

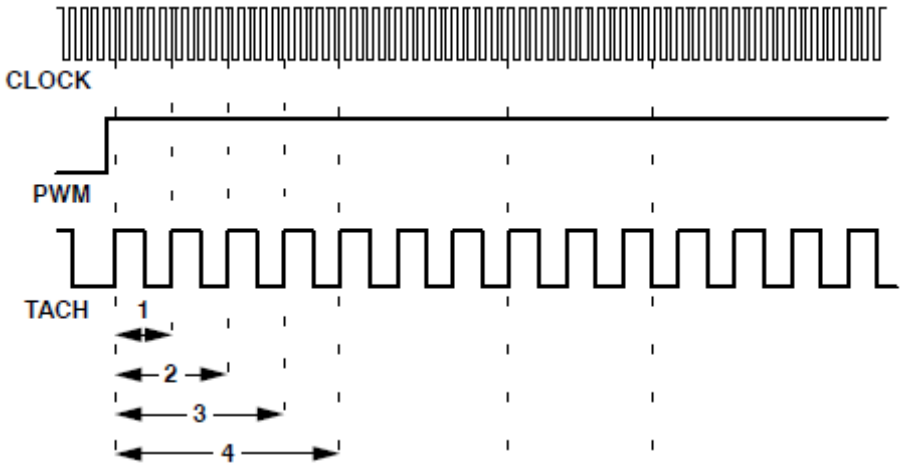

Figure 21. Fan Speed Measurement

Fan Speed Measurement Registers

The fan tachometer registers are 16−bit values consisting of a 2−byte read from the NCT7491.

- Register 0x28, TACH1 Low Byte
- Register 0x29, TACH1 High Byte
- Register 0x2A, TACH2 Low Byte
- Register 0x2B, TACH2 High Byte
- Register 0x2C, TACH3 Low Byte
- Register 0x2D, TACH3 High Byte
- Register 0x2E, TACH4 Low Byte
- Register 0x2F, TACH4 High Byte

Reading Fan Speed from the NCT7491

The measurement of fan speeds involves a 2−register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 12.82 us period clocks (78 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16−bit fan tachometer reading of 0xFFFF indicates that either the fan has stalled or is running very slowly (<100 RPM).

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an SMBALERT

Fan TACH Limit Registers

The fan TACH limit registers are 16−bit values consisting of two bytes.

- Register 0x54, TACH1 Minimum Low Byte = 0xFF default
- Register 0x55, TACH1 Minimum High Byte = 0xFF default
- Register 0x56, TACH2 Minimum Low Byte = 0xFF default
- Register 0x57, TACH2 Minimum High Byte = 0xFF default
- Register 0x58, TACH3 Minimum Low Byte = 0xFF default
- Register 0x59, TACH3 Minimum High Byte = 0xFF default
- Register 0x5A, TACH4 Minimum Low Byte = 0xFF default
- Register 0x5B, TACH4 Minimum High Byte = 0xFF default

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second. When set, the FAST bit (Bit 3) of Configuration Register 3 (0x78), updates the fan TACH readings every 250 ms.

DC Bits

If any of the fans are not being driven by a PWM channel but are powered directly from 5.0 V or 12 V, their associated dc bit in Configuration Register 3 (0x78) should be set. This

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allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For 4−wire fans, once high frequency mode is enabled, the dc bits do not need to be set because this is automatically done internally.

If any tach channels are not connected then the associated DC bit should be set for that fan.

Calculating Fan Speed From Register Values

Assuming a fan with a two pulses per revolution, and with the NCT7491 programmed to measure two pulses per revolution, fan speed is calculated by Fan Speed (RPM) = (78,000 x 60)/Fan TACH Reading where Fan TACH Reading is the 16−bit fan tachometer reading.

Example:

TACH1 High Byte (Register 0x29) = 0x17
TACH1 Low Byte (Register 0x28) = 0xFF
What is Fan 1 speed in RPM?
Fan 1 TACH Reading = 0x17FF = 6143 (decimal)
RPM = (f x 60)/Fan 1 TACH Reading
RPM = (78000 x 60)/6143
Fan Speed = 762 RPM

Fan Pulses per Revolution

Different fan models can output one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the TACH pulses per revolution register (0x7B) for each fan. Alternatively, this register can be used to determine the number or pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

TACH Pulses per Revolution Register 0x7B

- Bits [1:0], FAN1 default = 2 pulses per revolution
- Bits [3:2], FAN2 default = 2 pulses per revolution
- Bits [5:4], FAN3 default = 2 pulses per revolution
- Bits [7:6], FAN4 default = 2 pulses per revolution
- 00 = 1 pulse per revolution
- 01 = 2 pulses per revolution
- 10 = 3 pulses per revolution
- 11 = 4 pulses per revolution

Fan Spin−Up

The NCT7491 has a unique fan spin−up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. When two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage of this is that fans have different spin−up characteristics and take different times to overcome inertia. The NCT7491 runs the fans just fast enough to overcome inertia and is quieter on spin−up than fans programmed to spin up for a given spin−up time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up, because the fan is below running speed, the NCT7491 includes a fan startup timeout function. During this time, the NCT7491 looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated. Fan startup timeout can be disabled by setting Bit 3 (FSPDIS) of Configuration Register 7 (0x11).

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THERM ASSERTION

Pins 14, 19 and 22 on the QSOP package, or pins 11, 16 and 19 on the QFN package can be configured as THERM I/O pins. These are open−drain active low pins used to signal that a critical temperature limit has been exceeded. If a temperature measurement exceeds its associated THERM limit (or Tcontrol limit for PECI) then the THERM pin will assert low. THERM assertion can be enabled or disabled for each thermal measurement channel. PWM outputs can be configured to respond to THERM assertions. By default THERM assertion will cause the PWM outputs to go to 100% duty cycle for fail safe cooling. This can be individually disabled for each PWM output. THERM assertion behavior can be modified so that the outputs do not immediately go to 100% when THERM asserts. If this function is enabled then an associated temperature step register is used to increase the PWM duty in steps. For example, if the step register is set to 4 degrees then the PWM output will go to PWMStep1 at the THERM limit, to PWMStep2 at THERM+4 and 100% at THERM+2x4, where PWMStep1 and PWMStep2 are programmable PWM levels.

THERM Pin Configuration

Configuring Pin 14 (QSOP), Pin 11 (QFN) as a THERM pin:

Setting bits <1:0> of register 0x7D to <01> sets pin 14 on the QSOP package or pin 11 on the QFN package as a THERM pin.

Configuring Pin 19 (QSOP), Pin 16 (QFN) as a THERM pin:

Setting bits <3:2> of register 0x7C to <01> sets pin 19 on the QSOP package or pin 16 on the QFN package as a THERM pin.

Configuring Pin 22 (QSOP), Pin 19 (QFN) as a THERM pin:

Setting bit 1 of register 0x78 to 1 enables pin 22 on the QSOP package or pin 19 on the QFN package as a THERM pin.

THERM/Tcontrol Limit Registers

- Remote1 THERM Limit, 0x6A
- Local THERM Limit, 0x6B
- Remote2 THERM Limit, 0x6C
- PECI0 Tcontrol Limit, 0x3D
- PECI1 Tcontrol Limit, 0x08
- PECI2 Tcontrol Limit, 0x09
- PECI3 Tcontrol Limit, 0x0A
- SMBus Device THERM Limit, 0xC3 (applies to all SMBus devices)
- Push temperature THERM Limit, 0xD0 (applies to all Push channels)

If any temperature channel exceeds its associated THERM limit then a status bit will be set to indicate the condition. If that channel is enabled for pin assertions and a THERM pin has been configured then the pin will assert. If the temperature value goes below its THERM limit then the status bit will automatically clear and the pin will de−assert.

- If Offset64 mode is enabled then Remote1/Local/Remote2 THERM limits should be programmed in that format. Otherwise those limits should be programmed as 2's complement values.
- If PECI Absolute mode is enabled than PECI Tcontrol limits should be programmed as unsigned values, otherwise they should be programmed as 2's complement values.
- SMBus THERM limit should be programmed as an unsigned value.
- Push THERM limit should be programmed as a 2's complement value.

THERM Status Bits

- PECI Tcontrol status bits = 0x89 <3:0>
- Remote1 THERM status bit = 0x89 <4>
- Local THERM status bit = 0x89 <5>
- Remote2 THERM status bit = 0x89 <6>
- SMBus slave THERM status bits = 0xBB <7:0>
- Push THERM status bits = 0x7E <7:4>

Enabling THERM/Tcontrol Assertions for the Temperature Channels

- Set 0x7C bit 4 to 1 to enable PECI $T_{CONTROL}$ pin assertions
- Set 0x7C bit 5 to 1 to enable Remote1 THERM pin assertions,
- Set 0x7C bit 6 to 1 to enable Local THERM pin assertions,
- Set 0x7C bit 7 to 1 to enable Remote2 THERM pin assertions,
- Set 0x16 bit 5 to 1 to enable Push temperature THERM pin assertions,
- Set 0x16 bit 6 to 1 to enable SMBus slave THERM pin assertions

PECI $T_{CONTROL}$ enable bit applies to all PECI channels

Push temperature THERM enable applies to all Push channels

SMBus slave enable bit applies to all SMBus channels

The user should also ensure that the THERM Disable bit, 0x7D <2>, is 0. This is the THERM disable bit and when set to 1 will disable all THERM pin assertions.

Enabling the PWM Response to THERM Assertions

- PWM1 responds to THERM, 0x17 bit 0
- PWM2 responds to THERM, 0x17 bit 1
- PWM3 responds to THERM, 0x17 bit 2

If these bits are set to 1 then the associated PWM output will be affected by a THERM assertion. There are 3 possible responses: go to 100%, go to Maximum PWM or implement the THERM Stepping function.

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Setting the PWM Level for THERM Events

- PWM1 Max/Full, 0x16, bit 2
- PWM2 Max/Full, 0x16, bit 3
- PWM3 Max/Full, 0x16, bit 4

If these bits are set to 1 then the fans will go to 100% on THERM assertion. If they are 0 then they will go to the Maximum PWM value.

These bits are ignored if the THERM stepping function is enabled.

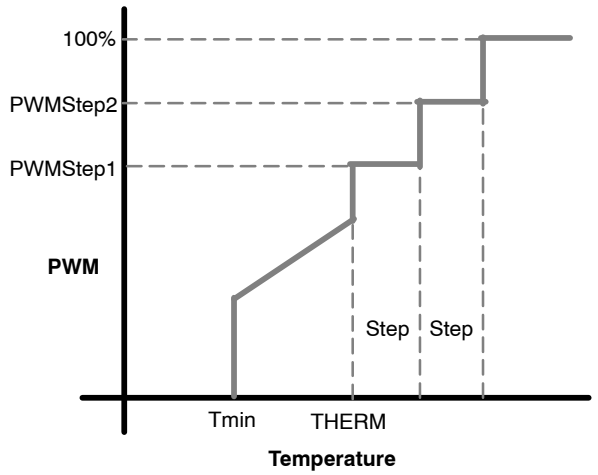

Figure 22. THERM Stepping Function

THERM Stepping Function

If the THERM Stepping function is enabled then the associated PWM output goes to PWMStep1 when the temperature is higher than THERM. The PWM output goes to PWMStep2 when the temperature is higher than THERM+Step and goes to 100% if the temperature reaches THERM+2xStep. THERM stepping does not apply to PWM channels in look−up table mode.

THERM Stepping is enabled by writing a value greater than 0°C to the THERM Step Size registers

Setting the THERM Step Size

- SMBus slave THERM Step, 0x18, bits <3:0>
- PECI THERM Step, 0x18 bits <7:4>
- Remote1/Local/Remote2 THERM Step, 0x19 bits <3:0>
- Push temperature THERM Step, 0x19 bits <7:4>

The range of temperature values that can be programmed for the Step size is 0 to 15°C. If set to 0 then the stepping function is disabled.

Setting the PWM Levels for THERM Stepping

- PWMStep1 Value, 0x14
- PWMStep2 Value, 0x15

PWMStep1 sets the PWM level that is output when a temperature exceeds its THERM limit (and Stepping is enabled). PWMStep2 sets the PWM level if the temperature exceeds THERM Limit + Step, where Step is the programmed step size for the temperature channel.

PWMStep1 and PWMStep2 are absolute PWM values and have a resolution of 1 lsb = 0.392%.

NOTE: If stepping is enabled for a temperature channel controlling a PWM output, then that PWM output will only respond to THERM events generated by its own temperature control sources and will not respond to THERM events from other temperature sources.

THERM TIMER

The NCT7491 has an internal timer to measure THERM assertion time. For example, the THERM input can be connected to the PROCHOT output of a CPU to measure system performance. The THERM input can also be connected to the output of a trip point temperature sensor. The timer is started on the assertion of the NCT7491 THERM input and stopped when THERM is deasserted. The timer counts THERM times cumulatively, that is, the timer resumes counting on the next THERM assertion. The THERM timer continues to accumulate THERM assertion times until the timer is read (it is cleared on read), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8−bit THERM timer value register (0x79) is designed so that Bit 0 is set to 1 on the first THERM assertion. Once the cumulative THERM assertion time has exceeded 45.52 ms, Bit 1 of the THERM timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 23).

After a pin has been configured as a THERM pin the timer function can be enabled on the pin using bits <1:0> of register 0x16:

- <00> = Timer disabled
- <01> = Timer enabled on pin 14 (QSOP), pin 11 (QFN)
- <10> = Timer enabled on pin 19 (QSOP), pin 16 (QFN)
- <11> = Timer enabled on pin 22 (QSOP), pin 19 (QFN)

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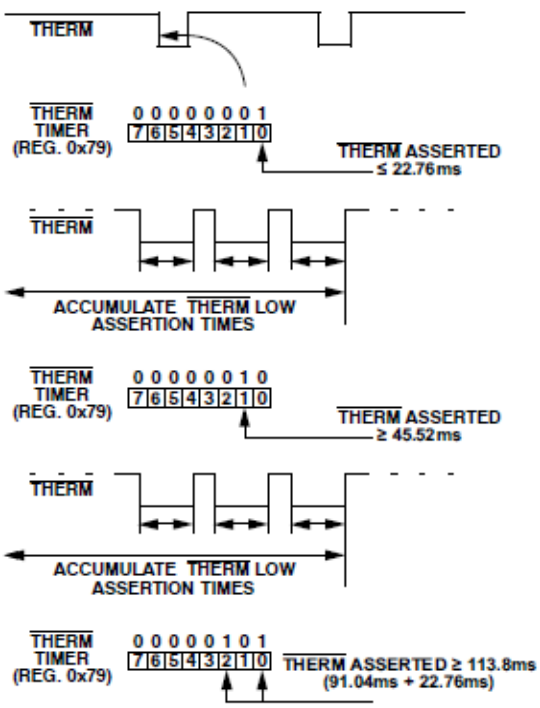

Figure 23. THERM Timer

THERM Timer Limit

The THERM Timer limit register can be used to assert an SMBALERT output when the timer measurement exceeds the programmed limit value. If the value N is programmed to the limit register then the limit time will be (N + 1) x 22.76 ms.

SMBALERT FUNCTIONS

All of the measured temperatures, voltages and fan speeds have associated limit registers to detect when an out of limit condition occurs on any channel. Each of these channels has an associated status bit that can be read over the SMBus to determine the limit. There are also status bits to indicate the success or failure of various functions, such as the PECI interface or the SMBus Master Port interface. If a pin is configured as an SMBALERT pin then any of the status bits can assert the pin when they are set by the NCT7491. Most of the status bits can be masked, allowing the user to prevent assertion of the SMBALERT pins by functions that are not required in an application. Descriptions of the limit registers for each temperature, voltage or fan channel are described in their relevant sections of this document.

Enabling Pins as SMBALERT Pins

- Setting bit 0 of register 0x78 sets pin 10 on the QSOP package, or pin 7 on the QFN package as an SMBALERT pin.
- Setting bits <1:0> of register 0x7D to <10> sets pin 14 on the QSOP package or pin 11 on the QFN package as an SMBALERT pin.
- Setting bits <3:2> of register 0x7C to <00> sets pin 19 on the QSOP package or pin 16 on the QFN package as an SMBALERT pin.

NCT7491 Status Bits

When a status bit is set and the SMBALERT output asserts it may be necessary to read the status registers to determine the source of the assertion. To minimize to number of register reads required the NCT7491 uses Out Of Limit bits (OOL bits) to indicate in which registers an assertion has occurred.

By first reading Status OOL register address 0x12 it can be determined which other status registers are active. Once set, a status bit will remain set until the register that it is contained in is read over the SMBus interface, even if the fault that caused the assertion is no longer present.

OOL register 0x12 Definitions:

- Bit 0 of 0x12 = 1 indicates an assertion in register 0x41 (Analog temperature and Voltage limit errors)
- Bit 1 of 0x12 = 1 indicates an assertion in register 0x7E (Push register limit errors)
- Bit 2 of 0x12 = 1 indicates an assertion in register 0xB6 (SMBus Master NACK errors)
- Bit 3 of 0x12 = 1 indicates an assertion in register 0xB7 (SMBus Master PEC errors)
- Bit 4 of 0x12 = 1 indicates an assertion in register 0xB8 (SMBus Master Timeout errors)
- Bit 5 of 0x12 = 1 indicates an assertion in register 0xB9 (SMBus Master limit errors)
- Bit 6 of 0x12 = 1 indicates an assertion in register 0xBA (SMBus Master Data Invalid errors)
- Bit 7 of 0x12 = 1 indicates an assertion in register 0x89 (Tcontrol/THERM assertions). This bit relates to THERM function and does not affect the SMBALERT pins.

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List of Status Registers

The complete list of status registers is given below along with their associated mask registers. The definitions for the status bits for each of the registers can be found in the register tables at the end of this document. OOL bits in any register do not require to be masked as they do not assert the SMBALERT pin.

Table 29. STATUS REGISTERS

Status Bits	Status Register Address	Mask Register Address
Indicates status assertions in registers 0x41, 0x7E, 0xB6, 0xB7, 0xB8, 0xB9, 0xBA and 0x89.	0x12	Not applicable
Voltage & Analog temperature out of limit bits. OOL bit for register 0x42.	0x41	0x74
Voltage, Fans, Diode Faults. OOL bit for register 0x43.	0x42	0x75
PECI0 out of limit, PECI COMM/ DATA error, THERM assertion, DATA error code. OOL bit for register 0x81.	0x43	0x82
PECI completion code error, THERM timer error, Generic COMM error, PECI1−3 out of limit bits, PCH byte count error, V_{TT} out of limit bit.	0x81	0x83
Push register out of limit bits	0x7E	0x7F
SMBus Master NACK errors	0xB6	0xBC
SMBus Master PEC errors	0xB7	0xBD
SMBus Master Timeout errors	0xB8	0xBE
SMBus Master out of limit bits	0xB9	0xBF
SMBus Master Data Invalid errors	0xBA	0xC0

VOLTAGE MONITORING

The NCT7491 has 5 external voltage measurement channels. It can also measure its own supply voltage, V_{CC}. The NCT7491 can measure 5 V, 12 V, and 2.5 V supplies, and the processor core voltage V_{CCP} (0 V to 3 V input). The 2.5 V input can be used to monitor a chipset supply voltage in computer systems. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin. The PECI V_{TT} voltage is also measured and is the dedicated reference voltage for the PECI circuitry.

Analog−to−Digital Converter

All analog inputs are multiplexed into the on−chip, successive− approximation, analog−to−digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2 V, but the inputs have built−in attenuators to allow measurement of 2.5 V, 3.3 V, 5 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 dec or 300 hex) for the nominal input voltage, and so has adequate headroom to cope with overvoltages.

Voltage Input Circuitry

The internal structure for the analog inputs is shown in Figure 24. The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first−order low−pass filter that gives input immunity to high frequency noise. The attenuators can be disabled for the voltage channels, except for the Vcc channel.

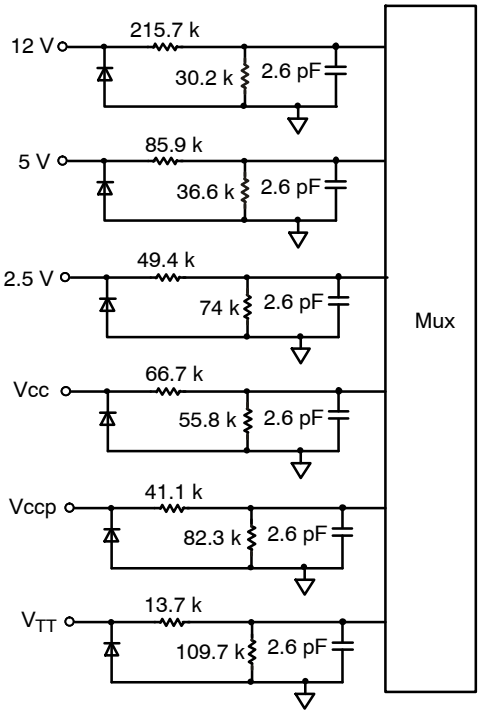

Figure 24. Voltage Input Structures

Voltage Measurement Registers

- Reg. 0x1E, V_{TT} Reading = 0x00 default
- Reg. 0x20, 2.5 V Reading = 0x00 default
- Reg. 0x21, V_{CCP} Reading = 0x00 default
- Reg. 0x22, V_{CC} Reading = 0x00 default
- Reg. 0x23, 5 V Reading = 0x00 default
- Reg. 0x24, 12 V Reading = 0x00 default

Extended Resolution Registers

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x1F, 0x76 and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers (0x1E, 0x20 to 0x24) is locked until their data is read. That is, if extended resolution is required, the extended resolution register must be read first immediately followed by the appropriate voltage measurement register.

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Voltage Measurement Selection

The user can select which voltage channels to include in the monitoring loop. By only including the channels that are required the loop monitoring time can be reduced.

- Setting <2> of register 0x11 includes the V_{TT} channel in the monitoring loop.
- Setting <3> of register 0x13 includes the 12V channel in the monitoring loop.
- Setting <4> of register 0x13 includes the 5 V channel in the monitoring loop.
- Setting <5> of register 0x13 includes the Vccp channel in the monitoring loop.
- Setting <6> of register 0x13 includes the 2.5 V channel in the monitoring loop.
- Setting <7> of register 0x13 includes the Vcc channel in the monitoring loop.

Voltage Measurement Resolution

The NCT7491 uses a reference voltage of 2 V. The ADC is 10−bit giving a resolution of 1.953 mV per lsb. This is the resolution that applies when the attenuators are disabled. With attenuators enabled the resolution for each channel is as follows:

- 12 V resolution = 15.92 mV per lsb
- 5 V resolution = 6.54 mV per lsb
- 2.5 V resolution = 3.26 mV per lsb
- Vccp resolution = 2.93 mV per lsb
- Vcc resolution = 4.29 mV per lsb
- V_{TT} resolution = 2.2 mV per lsb

Voltage Limit Registers

Associated with each voltage measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate SMBALERT interrupts.

- Reg. 0x84, V_{TT} Low Limit
- Reg. 0x86, V_{TT} High Limit
- Reg. 0x44, 2.5 V Low Limit
- Reg. 0x45, 2.5 V High Limit
- Reg. 0x46, V_{CCP} Low Limit
- Reg. 0x47, V_{CCP} High Limit
- Reg. 0x48, V_{CC} Low Limit
- Reg. 0x49, V_{CC} High Limit
- Reg. 0x4A, 5 V Low Limit
- Reg. 0x4B, 5 V High Limit
- Reg. 0x4C, 12 V Low Limit
- Reg. 0x4D, 12 V High Limit

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the NCT7491 to offer the system designer increased flexibility. The functions described below are enabled by setting the appropriate bit in configuration register 2 (0x73).

Turn−Off Voltage Averaging

The averager length that is applied to the temperature readings is also applied to the voltage readings. The averager length is programmable as 4, 8, 16 or 32 samples. These values can be selected in register 0x40 bits <7:6>.

When faster conversions are needed, setting Bit 3 of Configuration Register 2 (Reg. 0x73) turns voltage averaging off. This gives a faster reading, but the reading can be noisier. The default round−robin cycle time takes **TBD** ms.

Bypass Individual Voltage Input Attenuators

Bits <7:3> of Configuration Register 4 (0x7D) can be used to bypass individual voltage channel attenuators.

Table 30. BYPASSING VOLTAGE ATTENUATORS

Configuration Register 4 (0x7D)	
Bit	**Channel Attenuated**
3	Bypass V_{TT} attenuator
4	Bypass 2.5 V attenuator
5	Bypass V_{CCP} attenuator
6	Bypass 5 V attenuator
7	Bypass 12 V attenuator

The input range of the ADC without the attenuators is 0 V to 2 V.

GPIO FUNCTIONS

There are up to 3 pins that can be configured as open−drain general purpose digital I/O pins. These are pins 5 (GPIO1), 6 (GPIO2) and 19 (GPIO3) on the QSOP package and pins 2 (GPIO1), 3 (GPIO2) and 16 (GPIO3) on the QFN package. GPIO1 and GPIO2 are shared with the SMBus Master Port pins SCL_M and SDA_M. GPIO3 is shared with THERM and SMBALERT functions.

There are 2 bits that must be programmed to enable the GPIO1 and GPIO2 functions:

- Setting bit 1 of register 0x80 to 1 enables GPIO1 and GPIO2
- Clearing bit 0 of register 0xB5 to 0 disables the SMBus Master Port. This bit has priority over the GPIO enable bit so must be cleared for GPIOs to function.

GPIO3 is enabled by setting bits <3:2> of register 0x7C to <10>.

Each GPIO pin has associated direction, polarity and data bits.

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GPIO1

- Bit 7 of register 0x80 sets GPIO1 direction. 1=Input, 0=Output
- Bit 5 of register 0x80 sets GPIO1 polarity. 1=active high, 0=active low
- Bit 3 of register 0x80 is GPIO1 data. If GPIO1 is an input this bit shows the pin state. If it is an output then this bit sets the output state.

GPIO2

- Bit 6 of register 0x80 sets GPIO2 direction. 1=Input, 0=Output
- Bit 4 of register 0x80 sets GPIO2 polarity. 1=active high, 0=active low
- Bit 2 of register 0x80 is GPIO2 data. If GPIO2 is an input this bit shows the pin state. If it is an output then this bit sets the output state.

GPIO3

- Bit 7 of register 0x85 sets GPIO3 direction. 1=Input, 0=Output
- Bit 6 of register 0x85 sets GPIO3 polarity. 1=active high, 0=active low
- Bit 5 of register 0x85 is GPIO3 data. If GPIO3 is an input this bit shows the pin state. If it is an output then this bit sets the output state.

When writing to a GPIO pin that is configured as an output the polarity must be taken into account. For example, if the pin is set as active low then writing a 1 to the data bit will pull the GPIO pin low.

When GPIOs are configured as inputs the data bit always shows the actual pin state.

VCCP LOW DETECTION

If the processor core voltage is being monitored on the Vccp channel and the NCT7491 is run from the auxiliary rail, then the user can enable a function to suspend various functions in the NCT7491 when the core voltage falls below a programmable threshold.

Setting bit 6 of register 0x10 enables the Vccp Low function. In this mode, if the Vccp voltage falls below the value in the Vccp Low Limit register (0x46) then the Vccp status bit is set, the THERM timer function is disabled, PECI errors are cleared, SMBus Master errors are cleared and all PWM outputs shut down. When the Vccp voltage increases above the Vccp Low Limit then any of the above functions that were previously enabled will become active again.

XNOR TREE TEST MODE

The NCT7491 includes an XNOR tree test mode. This mode is useful for in−circuit test equipment at board−level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens, or shorts, on the system board.

The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR Tree Test Enable register (Register 0x6F). Figure 25 shows the signals that are exercised in the XNOR tree test mode.

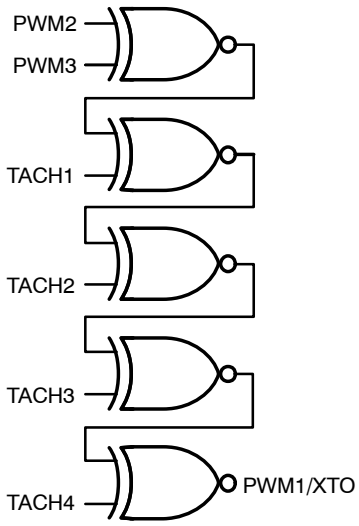

Figure 25. XNOR Tree Test

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R/W	PECI0 Address	7	6	5	4	3	2	1	0
0x01	R/W	PECI1 Address	7	6	5	4	3	2	1	0
0x02	R/W	PECI2 Address	7	6	5	4	3	2	1	0
0x03	R/W	PECI3 Address	7	6	5	4	3	2	1	0
0x04	R	PECI0_Abs	7	6	5	4	3	2	1	0
0x05	R	PECI1_Abs	7	6	5	4	3	2	1	0
0x06	R	PECI2_Abs	7	6	5	4	3	2	1	0
0x07	R	PECI3_Abs	7	6	5	4	3	2	1	0
0x08	R/W	PECI1 Tcontrol	7	6	5	4	3	2	1	0
0x09	R/W	PECI2 Tcontrol	7	6	5	4	3	2	1	0
0x0A	R/W	PECI3 Tcontrol	7	6	5	4	3	2	1	0
0x0B	R	PECI0 Tjmax	7	6	5	4	3	2	1	0
0x0C	R	PECI1 Tjmax	7	6	5	4	3	2	1	0
0x0D	R	PECI2 Tjmax	7	6	5	4	3	2	1	0
0x0E	R	PECI3 Tjmax	7	6	5	4	3	2	1	0
0x0F	R/W	PECI Config 4	DM3CPU	DM3CPU	DM2CPU	DM2CPU	DM1CPU	DM1CPU	DM0CPU	DM0CPU
0x10	R/W	Config. 6		V_{CCP} Low	IFT	SMBRT1	SMBRT0	PWM3 Mode	PWM2 Mode	PWM1 Mode
0x11	R/W	Config. 7	SMBFS3	SMBFS2	SMBFS1	TODIS	FSPDIS	VTT	FSPD	THERMHys
0x12	R	Interrupt Status 6	OOL10	OOL9	OOL8	OOL7	OOL6	OOL5	OOL4	OOL0
0x13		Config. 8	Vcc	2.5V	Vccp	5V	12V	Rem2	Rem1	Local
0x14	R/W	PWMStep1	7	6	5	4	3	2	1	0
0x15	R/W	PWMStep2	7	6	5	4	3	2	1	0
0x16	R/W	THERM Config1		SMBus THERM	Push THERM	Max/Full 3	Max/Full 2	Max/Full 1	TMRP1	TMRP0
0x17	R/W	THERM Config2						P3TH	P2TH	P1TH
0x18	R/W	THERM Config3	PECSTEP	PECSTEP	PECSTEP	PECSTEP	SMBSTEP	SMBSTEP	SMBSTEP	SMBSTEP
0x19	R/W	THERM Config4	PSHSTEP	PSHSTEP	PSHSTEP	PSHSTEP	SNRSTEP	SNRSTEP	SNRSTEP	SNRSTEP
0x1A	R	PECI1	7	6	5	4	3	2	1	0
0x1B	R	PECI2	7	6	5	4	3	2	1	0
0x1C	R	PECI3	7	6	5	4	3	2	1	0
0x1D	R	Device ID	7	6	5	4	3	2	1	0
0x1E	R	Vtt measurement	9	8	7	6	5	4	3	2
0x1F	R	Extended resolution 3			Vtt	Vtt				
0x20	R	2.5 V Measurement	9	8	7	6	5	4	3	2
0x21	R	V_{CCP} Measurement	9	8	7	6	5	4	3	2
0x22	R	V_{CC} Measurement	9	8	7	6	5	4	3	2
0x23	R	5 V Measurement	9	8	7	6	5	4	3	2
0x24	R	12 V Measurement	9	8	7	6	5	4	3	2
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2
0x26	R	Local Temperature	9	8	7	6	5	4	3	2
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2
0x28	R	TACH 1 Low Byte	7	6	5	4	3	2	1	0
0x29	R	TACH 1 High Byte	15	14	13	12	11	10	9	8
0x2A	R	TACH 2 Low Byte	7	6	5	4	3	2	1	0
0x2B	R	TACH 2 High Byte	15	14	13	12	11	10	9	8

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2C	R	TACH 3 Low Byte	7	6	5	4	3	2	1	0
0x2D	R	TACH 3 High Byte	15	14	13	12	11	10	9	8
0x2E	R	TACH 4 Low Byte	7	6	5	4	3	2	1	0
0x2F	R	TACH 4 High Byte	15	14	13	12	11	10	9	8
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0
0x33	R	PECI0	7	6	5	4	3	2	1	0
0x34	R/W	PECI Low Limit	7	6	5	4	3	2	1	0
0x35	R/W	PECI High Limit	7	6	5	4	3	2	1	0
0x36	R/W	PECI configuration Register 1					DOM0	AVG2	AVG1	AVG0
0x37	R/W	PECI Config 3	PWEN		Rate1	Rate0			RTYDIS	PDET
0x38	R/W	Max PWM 1 Duty Cycle	7	6	5	4	3	2	1	0
0x39	R/W	Max PWM 2 Duty Cycle	7	6	5	4	3	2	1	0
0x3A	R/W	Max PWM 3 Duty Cycle	7	6	5	4	3	2	1	0
0x3B	R/W	PECI T_{MIN}	7	6	5	4	3	2	1	0
0x3C	R/W	PECI T_{RANGE}	RANGE	RANGE	RANGE	RANGE				
0x3D	R/W	PECI0 $T_{CONTROL}$	7	6	5	4	3	2	1	0
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0
0x3F	R	Version/Revision	Ver3	Ver2	Ver1	Ver0	4−wire	PECI	REV1	REV0
0x40	R/W	Configuration 1	AVELN1	AVELN0	THERM Override	PECI Monitor	Fan Boost	RDY	LOCK	STRT
0x41	R	Interrupt Status 1	OOL	R2T	LT	R1T	5 V	V_{CC}	V_{CCP}	2.5 V
0x42	R	Interrupt Status 2	D2 FAULT	D1 FAULT	FAN4	FAN3	FAN2	FAN1	OOL	12 V
0x43	R	Interrupt Status 3	OOL3	DAT2	DAT1	DAT0	OVT ($\overline{\text{THERM}}$ Temp Limit)	COMM	DATA	PECI0
0x44	R/W	2.5 V Low Limit	7	6	5	4	3	2	1	0
0x45	R/W	2.5 V High Limit	7	6	5	4	3	2	1	0
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0
0x4A	R/W	5 V Low Limit	7	6	5	4	3	2	1	0
0x4B	R/W	5 V High Limit	7	6	5	4	3	2	1	0
0x4C	R/W	12 V Low Limit	7	6	5	4	3	2	1	0
0x4D	R/W	12 V High Limit	7	6	5	4	3	2	1	0
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0
0x55	R/W	TACH1 Minimum High Byte	15	14	13	12	11	10	9	8

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0
0x57	R/W	TACH2 Minimum High Byte	15	14	13	12	11	10	9	8
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10	9	8
0x5C	R/W	PWM1 Configuration Register				INV		SPIN	SPIN	SPIN
0x5D	R/W	PWM2 Configuration Register				INV		SPIN	SPIN	SPIN
0x5E	R/W	PWM3 Configuration Register				INV		SPIN	SPIN	SPIN
0x5F	R/W	Remote 1 T_{RANGE}/PWM 1 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ
0x60	R/W	Local T_{RANGE}/PWM 2 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ
0x61	R/W	Remote 2 T_{RANGE}/PWM3 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ
0x62	R/W	Enhance Acoustics Reg. 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU1	ACOU1	ACOU1
0x63	R/W	Enhance Acoustics Reg. 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0
0x6B	R/W	Local $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0
0x6D	R/W	Remote 1 and Local Temp/T_{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL
0x6E	R/W	Remote 2 and PECI Temp/T_{MIN} Hysteresis	HYSR2	HYSR2	HYSR2	HYRS	HYSP	HYSP	HYSP	HYSP
0x6F	R/W	XNOR Tree Test Enable								XEN
0x70	R/W	Remote 1 Temperature Offset	7	6	5	4	3	2	1	0
0x71	R/W	Local Temperature Offset	7	6	5	4	3	2	1	0
0x72	R/W	Remote 2 Temperature Offset	7	6	5	4	3	2	1	0
0x73	R/W	Configuration Register 2	Shutdown	FQ1	FQ0	TAVG	VAVG	ABS/REL		
0x74	R/W	Interrupt Mask 1 Register		R2T	LT	RIT	5 V	V_{CC}	V_{CCP}	2.5 V
0x75	R/W	Interrupt Mask 2 Register	D2	D1	FAN4	FAN3	FAN2	FAN1		12 V
0x76	R	Extended Resolution 1	5 V	5 V	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	2.5 V	2.5 V
0x77	R	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	12 V	12 V
0x78	R/W	Config. 3	DC4	DC3	DC2	DC1	FAST		THERM/2.5V	ALERT Enable
0x79	R	$\overline{\text{THERM}}$ Timer Value	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/TMRO
0x7A	R/W	$\overline{\text{THERM}}$ Timer Limit	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1
0x7C	R/W	Configuration Register 5	R2 THERM O/P	Local THERM O/P	R1 THERM O/P	PECI THERM O/P	PIN19 Func	PIN19 Func	Temp Offset	TWOS COMPL
0x7D	R/W	Configuration Register 4	BpAtt 12 V	BpAtt 5 V	BpAtt V_{CCP}	BpAtt 2.5 V	BpAtt Vtt	$\overline{\text{THERM}}$ Disable	Pin 14 Func	Pin 14 Func
0x7E	R	Interrupt Status 5	OVT_P3	OVT_P2	OVT_P1	OVT_P0	PUSH3	PUSH2	PUSH1	PUSH0
0x7F	R/W	Interrupt Mask 5					PUSH3	PUSH2	PUSH1	PUSH0
0x80	R/W	GPIO Configuration register	GPIO1 DIR	GPIO2 DIR	GPIO1 POL	GPIO2 POL	GPIO1	GPIO2	GPEN	
0x81	R	Interrupt Status 4	V_{TT}	SMBCNT	PECI3	PECI2	PECI1	GCOMM	TTS	PCC
0x82	R/W	Interrupt Mask 3					OVT $\overline{\text{THERM}}$ Temp Limit	COMM	DATA	PECI0
0x83	R/W	Interrupt Mask 4	V_{TT}	SMBCNT	PECI3	PECI2	PECI1	GCOMM	TTS	PCC
0x84	R/W	V_{TT} Low Limit	7	6	5	4	3	2	1	0
0x85	R/W	GPIO Config 2	GPIO3 DIR	GPIO3 POL	GPIO3					
0x86	R/W	V_{TT} High Limit	7	6	5	4	3	2	1	0
0x87	R/W	Configuration 9	D4V	D3V	D2V	D1V		PWM3OFF	PWM2OFF	PWM1OFF
0x88	R/W	PECI Config 2	#CPU	#CPU	DOM1	DOM2	DOM3			
0x89	R	Interrupt Status 7	OOL11	OVT_R2	OVT_LOC	OVT_R1	OVT3	OVT2	OVT1	OVT0
0x8A	R/W	PWM1 Source Control 1		PEC3	PEC2	PEC1	PEC0	REM2	REM1	LOC
0x8B	R/W	PWM1 Source Control 2	SMB7	SMB6	SMB5	SMB4	SMB3	SMB2	SMB1	SMB0
0x8C	R/W	PWM1 Source Control 3					PUSH3	PUSH2	PUSH1	PUSH0
0x8D	R/W	PWM2 Source Control 1		PEC3	PEC2	PEC1	PEC0	REM2	REM1	LOC
0x8E	R/W	PWM2 Source Control 2	SMB7	SMB6	SMB5	SMB4	SMB3	SMB2	SMB1	SMB0
0x8F	R/W	PWM2 Source Control 3					PUSH3	PUSH2	PUSH1	PUSH0
0x90	R/W	PWM3 Source Control 1		PEC3	PEC2	PEC1	PEC0	REM2	REM1	LOC
0x91	R/W	PWM3 Source Control 2	SMB7	SMB6	SMB5	SMB4	SMB3	SMB2	SMB1	SMB0
0x92	R/W	PWM3 Source Control 3					PUSH3	PUSH2	PUSH1	PUSH0
0x93		Revision	7	6	5	4	3	2	1	0
0x94	R/W	PECI0 Offset	7	6	5	4	3	2	1	0
0x95	R/W	PECI1 Offset	7	6	5	4	3	2	1	0
0x96	R/W	PECI2 Offset	7	6	5	4	3	2	1	0
0x97	R/W	PECI3 Offset	7	6	5	4	3	2	1	0
0x98	R/W	SMB Device0 Address		6	5	4	3	2	1	0
0x99	R/W	SMB Device 0 Command Code	7	6	5	4	3	2	1	0
0x9A	R/W	SMB Device1 Address		6	5	4	3	2	1	0
0x9B	R/W	SMB Device1 Pointer	7	6	5	4	3	2	1	0
0x9C	R/W	SMB Device2 Address		6	5	4	3	2	1	0
0x9D	R/W	SMB Device2 Pointer	7	6	5	4	3	2	1	0
0x9E	R/W	SMB Device3 Address		6	5	4	3	2	1	0
0x9F	R/W	SMB Device3 Pointer	7	6	5	4	3	2	1	0
0xA0	R/W	SMB Device4 Address		6	5	4	3	2	1	0
0xA1	R/W	SMB Device4 Pointer	7	6	5	4	3	2	1	0
0xA2	R/W	SMB Device5 Address		6	5	4	3	2	1	0

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xA3	R/W	SMB Device5 Pointer	7	6	5	4	3	2	1	0
0xA4	R/W	SMB Device6 Address		6	5	4	3	2	1	0
0xA5	R/W	SMB Device6 Pointer	7	6	5	4	3	2	1	0
0xA6	R/W	SMB Device7 Address		6	5	4	3	2	1	0
0xA7	R/W	SMB Device7 Pointer	7	6	5	4	3	2	1	0
0xA8	R	SMB Device0 Value (PCH)	7	6	5	4	3	2	1	0
0xA9	R	SMB Device1 Value (DIMM0)	7	6	5	4	3	2	1	0
0xAA	R	SMB Device2 Value (DIMM1)	7	6	5	4	3	2	1	0
0xAB	R	SMB Device3 Value (DIMM2)	7	6	5	4	3	2	1	0
0xAC	R	SMB Device4 Value (DIMM3)	7	6	5	4	3	2	1	0
0xAD	R	SMB Device5 Value	7	6	5	4	3	2	1	0
0xAE	R	SMB Device6 Value	7	6	5	4	3	2	1	0
0xAF	R	SMB Device7 Value	7	6	5	4	3	2	1	0
0xB0	R/W	SMB Config1	RS7	RS6	RS5	RS4	RS3	RS2	RS1	RS0
0xB1	R/W	SMB Config2	PEC7	PEC6	PEC5	PEC4	PEC3	PEC2	PEC1	PEC0
0xB2	R/W	SMB Config3	TFMT3	TFMT3	TFMT2	TFMT2	TFMT1	TFMT1	TFMT0	TFMT0
0xB3	R/W	SMB Config4	TFMT7	TFMT7	TFMT6	TFMT6	TFMT5	TFMT5	TFMT4	TFMT4
0xB4	R	Reserved								
0xB5	R/W	SMB Config5	PCHDIMM	R2DIMM	R1DIMM	SHYS3	SHYS2	SHYS1	SHYS0	SMBMEN
0xB6	R	SMB Status 1	NACK7	NACK6	NACK5	NACK4	NACK3	NACK2	NACK1	NACK0
0xB7	R	SMB Status 2	PEC7	PEC6	PEC5	PEC4	PEC3	PEC2	PEC1	PEC0
0xB8	R	SMB Status 3	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
0xB9	R	SMB Status 4	HILO7	HILO6	HILO5	HILO4	HILO3	HILO2	HILO1	HILO0
0xBA	R	SMB Status 5	TIV7	TIV6	TIV5	TIV4	TIV3	TIV2	TIV1	TIV0
0xBB	R	SMB Status 6	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
0xBC	R/W	SMB Mask 1	NACK7	NACK6	NACK5	NACK4	NACK3	NACK2	NACK1	NACK0
0xBD	R/W	SMB Mask 2	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0xBE	R/W	SMB Mask 3	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
0xBF	R/W	SMB Mask 4	HILO7	HILO6	HILO5	HILO4	HILO3	HILO2	HILO1	HILO0
0xC0	R/W	SMB Mask 5	TIV7	TIV6	TIV5	TIV4	TIV3	TIV2	TIV1	TIV0
0xC1	R/W	SMB High Limit	7	6	5	4	3	2	1	0
0xC2	R/W	SMB Low Limit	7	6	5	4	3	2	1	0
0xC3	R/W	SMB THERM Limit	7	6	5	4	3	2	1	0
0xC4	R	Reserved	7	6	5	4	3	2	1	0
0xC5	R	Reserved	7	6	5	4	3	2	1	0
0xC6	R/W	SMB Device Tmin	7	6	5	4	3	2	1	0
0xC7	R/W	SMB Device Trange	SMBINT1	SMBINT0			RNG	RNG	RNG	RNG
0xC8	R/W	Push0 Value	7	6	5	4	3	2	1	0
0xC9	R/W	Push1 Value	7	6	5	4	3	2	1	0
0xCA	R/W	Push2 Value	7	6	5	4	3	2	1	0
0xCB	R/W	Push3 Value	7	6	5	4	3	2	1	0
0xCC	R/W	Push Tmin	7	6	5	4	3	2	1	0
0xCD	R/W	Push Trange					RNG	RNG	RNG	RNG
0xCE	R/W	Push High Limit	7	6	5	4	3	2	1	0
0xCF	R/W	Push Low Limit	7	6	5	4	3	2	1	0

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xD0	R/W	Push THERM Limit	7	6	5	4	3	2	1	0
0xD1	R/W	Generic PECI Address	7	6	5	4	3	2	1	0
0xD2	R/W	Write Length	7	6	5	4	3	2	1	0
0xD3	R/W	Read Length	7	6	5	4	3	2	1	0
0xD4	R/W	WRDAT0	7	6	5	4	3	2	1	0
0xD5	R/W	WRDAT1	7	6	5	4	3	2	1	0
0xD6	R/W	WRDAT2	7	6	5	4	3	2	1	0
0xD7	R/W	WRDAT3	7	6	5	4	3	2	1	0
0xD8	R/W	WRDAT4	7	6	5	4	3	2	1	0
0xD9	R/W	WRDAT5	7	6	5	4	3	2	1	0
0xDA	R/W	WRDAT6	7	6	5	4	3	2	1	0
0xDB	R/W	WRDAT7	7	6	5	4	3	2	1	0
0xDC	R/W	WRDAT8	7	6	5	4	3	2	1	0
0xDD	R/W	WRDAT9	7	6	5	4	3	2	1	0
0xDE	R/W	WRDAT10	7	6	5	4	3	2	1	0
0xDF	R/W	WRDAT11	7	6	5	4	3	2	1	0
0xE0	R/W	WRDAT12	7	6	5	4	3	2	1	0
0xE1	R/W	RDDAT0	7	6	5	4	3	2	1	0
0xE2	R/W	RDDAT1	7	6	5	4	3	2	1	0
0xE3	R/W	RDDAT2	7	6	5	4	3	2	1	0
0xE4	R/W	RDDAT3	7	6	5	4	3	2	1	0
0xE5	R/W	RDDAT4	7	6	5	4	3	2	1	0
0xE6	R/W	RDDAT5	7	6	5	4	3	2	1	0
0xE7	R/W	RDDAT6	7	6	5	4	3	2	1	0
0xE8	R/W	RDDAT7	7	6	5	4	3	2	1	0
0xE9	R/W	RDDAT8	7	6	5	4	3	2	1	0
0xEA	R/W	PECI Config 5						PEX	AW	
0xEB	R/W	Push Hyst					PushHys3	PushHys2	PushHys1	PushHys0
0xEC to 0xFE	R	Reserved								
0xFF	R/W	Page Select								RGMP
0x100	R/W	Fan1 LUT Temp1	7	6	5	4	3	2	1	0
0x101	R/W	Fan1 LUT PWM1	7	6	5	4	3	2	1	0
0x102	R/W	Fan1 LUT Temp2	7	6	5	4	3	2	1	0
0x103	R/W	Fan1 LUT PWM2	7	6	5	4	3	2	1	0
0x104	R/W	Fan1 LUT Temp3	7	6	5	4	3	2	1	0
0x105	R/W	Fan1 LUT PWM3	7	6	5	4	3	2	1	0
0x106	R/W	Fan1 LUT Temp4	7	6	5	4	3	2	1	0
0x107	R/W	Fan1 LUT PWM4	7	6	5	4	3	2	1	0
0x108	R/W	Fan1 LUT Temp5	7	6	5	4	3	2	1	0
0x109	R/W	Fan1 LUT PWM5	7	6	5	4	3	2	1	0
0x10A	R/W	Fan1 LUT Temp6	7	6	5	4	3	2	1	0
0x10B	R/W	Fan1 LUT PWM6	7	6	5	4	3	2	1	0
0x10C	R/W	Fan1 LUT Temp7	7	6	5	4	3	2	1	0
0x10D	R/W	Fan1 LUT PWM7	7	6	5	4	3	2	1	0

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10E	R/W	Fan1 LUT Temp8	7	6	5	4	3	2	1	0
0x10F	R/W	Fan1 LUT PWM8	7	6	5	4	3	2	1	0
0x110	R/W	Fan2 LUT Temp1	7	6	5	4	3	2	1	0
0x111	R/W	Fan2 LUT PWM1	7	6	5	4	3	2	1	0
0x112	R/W	Fan2 LUT Temp2	7	6	5	4	3	2	1	0
0x113	R/W	Fan2 LUT PWM2	7	6	5	4	3	2	1	0
0x114	R/W	Fan2 LUT Temp3	7	6	5	4	3	2	1	0
0x115	R/W	Fan2 LUT PWM3	7	6	5	4	3	2	1	0
0x116	R/W	Fan2 LUT Temp4	7	6	5	4	3	2	1	0
0x117	R/W	Fan2 LUT PWM4	7	6	5	4	3	2	1	0
0x118	R/W	Fan2 LUT Temp5	7	6	5	4	3	2	1	0
0x119	R/W	Fan2 LUT PWM5	7	6	5	4	3	2	1	0
0x11A	R/W	Fan2 LUT Temp6	7	6	5	4	3	2	1	0
0x11B	R/W	Fan2 LUT PWM6	7	6	5	4	3	2	1	0
0x11C	R/W	Fan2 LUT Temp7	7	6	5	4	3	2	1	0
0x11D	R/W	Fan2 LUT PWM7	7	6	5	4	3	2	1	0
0x11E	R/W	Fan2 LUT Temp8	7	6	5	4	3	2	1	0
0x11F	R/W	Fan2 LUT PWM8	7	6	5	4	3	2	1	0
0x120	R/W	Fan3 LUT Temp1	7	6	5	4	3	2	1	0
0x121	R/W	Fan3 LUT PWM1	7	6	5	4	3	2	1	0
0x122	R/W	Fan3 LUT Temp2	7	6	5	4	3	2	1	0
0x123	R/W	Fan3 LUT PWM2	7	6	5	4	3	2	1	0
0x124	R/W	Fan3 LUT Temp3	7	6	5	4	3	2	1	0
0x125	R/W	Fan3 LUT PWM3	7	6	5	4	3	2	1	0
0x126	R/W	Fan3 LUT Temp4	7	6	5	4	3	2	1	0
0x127	R/W	Fan3 LUT PWM4	7	6	5	4	3	2	1	0
0x128	R/W	Fan3 LUT Temp5	7	6	5	4	3	2	1	0
0x129	R/W	Fan3 LUT PWM5	7	6	5	4	3	2	1	0
0x12A	R/W	Fan3 LUT Temp6	7	6	5	4	3	2	1	0
0x12B	R/W	Fan3 LUT PWM6	7	6	5	4	3	2	1	0
0x12C	R/W	Fan3 LUT Temp7	7	6	5	4	3	2	1	0
0x12D	R/W	Fan3 LUT PWM7	7	6	5	4	3	2	1	0
0x12E	R/W	Fan3 LUT Temp8	7	6	5	4	3	2	1	0
0x12F	R/W	Fan3 LUT PWM8	7	6	5	4	3	2	1	0
0x130–0x1CF		Reserved								
0x1D0	R/W	Test Reg 1	7	6	5	4	3	2	1	0
0x1D1	R/W	Test Reg 2	7	6	5	4	3	2	1	0
0x1D2	R/W	Test Reg 3	7	6	5	4	3	2	1	0
0x1D3	R/W	Test Reg 4	7	6	5	4	3	2	1	0
0x1D4	R/W	Test Reg 5	7	6	5	4	3	2	1	0
0x1D5	R/W	Test Reg 6	7	6	5	4	3	2	1	0
0x1D6	R/W	Test Reg 7	7	6	5	4	3	2	1	0
0x1D7	R/W	Test Reg 8	7	6	5	4	3	2	1	0
0x1D8	R/W	Test Reg 9	7	6	5	4	3	2	1	0

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Table 31. REGISTER TABLES

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1D9 – 0x1DF		Reserved								
0x1E0	R/W	Fuse Reg 1	7	6	5	4	3	2	1	0
0x1E1	R/W	Fuse Reg 2	7	6	5	4	3	2	1	0
0x1E2	R/W	Fuse Reg 3	7	6	5	4	3	2	1	0
0x1E3	R/W	Fuse Reg 4	7	6	5	4	3	2	1	0
0x1e4	R/W	Fuse Reg 5	7	6	5	4	3	2	1	0
0x1E5	R/W	Fuse Reg 6	7	6	5	4	3	2	1	0
0x1E6	R/W	Fuse Reg 7	7	6	5	4	3	2	1	0
0x1E7	R/W	Fuse Reg 8	7	6	5	4	3	2	1	0
0x1E8	R/W	Fuse Reg 9	7	6	5	4	3	2	1	0
0x1E9	R/W	Fuse Reg 10	7	6	5	4	3	2	1	0
0x1EA	R/W	Fuse Reg 11	7	6	5	4	3	2	1	0
0x1EB	R/W	Fuse Reg 12	7	6	5	4	3	2	1	0
0x1FF	R/W	Page Select Clear								RGMPCL

Table 32. PECI ADDRESS REGISTERS (Note 1) **(Power−On Default = 0x00)**

Register Address	R/W	Description
0x00	R/W	PECI0 CPU Address
0x01	R/W	PECI1 CPU Address
0x02	R/W	PECI2 CPU Address
0x03	R/W	PECI3 CPU Address

1. These registers are automatically populated when the PECI interface is enabled. They can be over−written if necessary.

Table 33. PECI_Abs REGISTERS (Note 2) **(Power−On Default = 0x00)**

Register Address	R/W	Description
0x04	R/W	PECI0 absolute value. 8 bit unsigned.
0x05	R/W	PECI1 absolute value. 8 bit unsigned.
0x06	R/W	PECI2 absolute value. 8 bit unsigned.
0x07	R/W	PECI3 absolute value. 8 bit unsigned.

2. These registers return the absolute CPU temperature calculated using the Tjmax value for each PECI channel.

Table 34. PECI Tcontrol LIMIT REGISTERS (Note 3) **(Power−On Default = 0x00)**

Register Address	R/W	Description
0x3D	R/W	PECI0 Tcontrol
0x08	R/W	PECI1 Tcontrol
0x09	R/W	PECI2 Tcontrol
0x0A	R/W	PECI3 Tcontrol

3. If any PECI reading exceeds its $T_{CONTROL}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail−safe mechanism incorporated to cool the system in the event of a critical over−temperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below T_{CONTRO} limit − hysteresis.

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Table 35. PECI TJMAX REGISTERS (Note 4) **(Power−On Default = 0x00)**

Register Address	R/W	Description
0x0B	R	PECI0 Tjmax
0x0C	R	PECI1 Tjmax
0x0D	R	PECI2 Tjmax
0x0E	R	PECI3 Tjmaxl

4. The maximum junction temperature for each CPU is returned in these registers. These are automatically read from the PECI interface on power−up

Table 36. REGISTER 0x0F − PECI Configuration Register 4 (Power−On Default = 0x00)

Bit	Mnemonic	R/W	Description
<1:0>	DM0CPU	R/W	Sets the DIMM0 CPU assignment: 00 = CPU0 01 = CPU1 10 = CPU2 11 = CPU3
<3:2>	DM1CPU	R/W	Sets the DIMM1 CPU assignment: 00 = CPU0 01 = CPU1 10 = CPU2 11 = CPU3
<5:4>	DM2CPU	R/W	Sets the DIMM2 CPU assignment: 00 = CPU0 01 = CPU1 10 = CPU2 11 = CPU3
<7:6>	DM3CPU	R/W	Sets the DIMM3 CPU assignment: 00 = CPU0 01 = CPU1 10 = CPU2 11 = CPU3

Table 37. REGISTER 0x10 − Configuration Register 6 (Power−On Default = 0x18)

Bit	Mnemonic	R/W	Description
<0>	PWM1Mode	R/W	0 = PWM1 uses Tmin/Trange control 1 = PWM1 uses LUT control
<1>	PWM2Mode	R/W	0 = PWM 2 uses Tmin/Trange control 1 = PWM2 uses LUT control
<2>	PWM3Mode	R/W	0 = PWM3 uses Tmin/Trange control 1 = PWM3 uses LUT control
<4:3>	SMBRT (Note 5)	R/W	Sets the SMBus Master Retry delay time: 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms
<5>	IFT	R/W	1 = Ignore first tach pulse during tach measurement. This can be used to stabilize readings from fans that produce erroneous glitches in 3−wire mode.

5. If an error occurs in the SMBus Master sequence then the interface will attempt to read from the slave device again. The interval between read attempts is set by SMBRT

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Table 37. REGISTER 0x10 − Configuration Register 6 (Power−On Default = 0x18)

Bit	Mnemonic	R/W	Description
<6>	V_{CCP}Low	R/W	VCCPLow = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (VCCP) drops below its VCCP low limit value (Reg. 0x46), the following occurs: Status Bit 1 in Status Register 1 is set. $\overline{\text{SMBALERT}}$ is generated, if enabled. $\overline{\text{PROCHOT}}$ monitoring is disabled. Everything is re−enabled once VCCP increases above the VCCP low limit. When VCCP increases above the low limit: $\overline{\text{PROCHOT}}$ monitoring is enabled. Fans return to their programmed state after a spin−up cycle.
<7>	Reserved	R	

5. If an error occurs in the SMBus Master sequence then the interface will attempt to read from the slave device again. The interval between read attempts is set by SMBRT

Table 38. REGISTER 0x11 − Configuration Register 7 (Power−On Default = 0x04)

Bit	Mnemonic	R/W	Description
<0>	THERMHys	R/W	Setting this bit to 1 enables $\overline{\text{THERM}}$ hysteresis. Note that hysteresis on $\overline{\text{THERM}}$ is disabled by default. To enable hysteresis this bit must be set to logic 1 and also bit <2> of register 0x7D must be cleared to 0.
<1>	FSPD	R/W	When set to 1, this bit runs all fans at max speed as programmed in the max PWM duty cycle registers (0x38 to 0x3A). Power−on default = 0. This bit is not locked at any time.
<2>	Vtt	R/W	Setting this bit to 1 includes Vtt in the analog monitoring cycle
<3>	FSPDIS	R/W	Logic 1 disables fan spin−up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin−up timeout selected.
<4>	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. In this state, if at any point during an SMBus transaction involving the NCT7491 activity ceases for more than 35 ms, the NCT7491 assumes the bus is locked and releases the bus. This allows the NCT7491 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
<5>	SMBFS1	R/W	PWM1 response to 3 consecutive SMBus Slave device errors; 0=no response; 1=PWM1 go to max speed or 100%
<6>	SMBFS2	R/W	PWM2 response to 3 consecutive SMBus Slave device errors; 0=no response; 1=PWM2 go to max speed or 100%
<7>	SMBFS3	R/W	PWM3 response to 3 consecutive SMBus Slave device errors; 0=no response; 1=PWM3 go to max speed or 100%

Table 39. REGISTER 0x12 − Interrupt Status 6 (Power−On Default = 0x00)

Bit	Mnemonic	R/W	Description
<0>	OOL0	R	1 = ALERT assertion in register 0x41
<1>	OOL4	R	1 = ALERT assertion in register 0x7E
<2>	OOL5	R	1 = ALERT assertion in register 0xB6
<3>	OOL6	R	1 = ALERT assertion in register 0xB7
<4>	OOL7	R	1 = ALERT assertion in register 0xB8
<5>	OOL8	R	1 = ALERT assertion in register 0xB9
<6>	OOL9	R	1 = ALERT assertion in register 0xBA
<7>	OOL10	R	1 = ALERT assertion in register 0x89

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Table 40. REGISTER 0x13 − Configuration Register 8 (Power−On Default = 0xFF)

Bit	Mnemonic	R/W	Description
<0>	Local	R/W	Setting this bit to 1 includes Local temperature in the analog monitoring cycle
<1>	Rem1	R/W	Setting this bit to 1 includes Rem1 temperature in the analog monitoring cycle
<2>	Rem2	R/W	Setting this bit to 1 includes Rem2 temperature in the analog monitoring cycle
<3>	12V	R/W	Setting this bit to 1 includes 12V in the analog monitoring cycle
<4>	5V	R/W	Setting this bit to 1 includes 5V in the analog monitoring cycle
<5>	Vccp	R/W	Setting this bit to 1 includes Vccp in the analog monitoring cycle
<6>	2.5V	R/W	Setting this bit to 1 includes 2.5V in the analog monitoring cycle
<7>	Vcc	R/W	Setting this bit to 1 includes Vcc in the analog monitoring cycle errors.

Table 41. PWM STEPPING LEVEL REGISTERS (Power−On Default = 0x00)

Register Address	Register	R/W	Description
0x14	PWMStep1	R/W	Sets the PWM level on a THERM assertion if THERM stepping is enabled
0x15	PWMStep2	R/W	Sets the PWM level if THERM stepping is enabled and the temperature is greater than THERM + Step (Note 6)

6. The temperature interval for each step is programmed in registers 0x18 and 0x19

Table 42. REGISTER 0x16 − THERM Configuration Register 1 (Power−On Default = 0x1C)

Bit	Mnemonic	R/W	Description
<1:0>	TMRP	R/W	00 = Disabled 01 = Pin 14 (QSOP), Pin 11 (QFN) is THERM timer input 10 = Pin 19 (QSOP), Pin 16 (QFN) is THERM timer input 11 = Pin 22 (QSOP), Pin 19 (QFN) is THERM timer input
<2>	Max/Full 1	R/W	1= PWM1 goes to 100% on THERM 0= PWM1 goes to Max programmed PWM on THERM
<3>	Max/Full 2	R/W	1= PWM2 goes to 100% on THERM 0= PWM2 goes to Max programmed PWM on THERM
<4>	Max/Full 3	R/W	1= PWM3 goes to 100% on THERM 0= PWM3 goes to Max programmed PWM on THERM
<5>	Push THERM	R/W	1 = THERM assertions enabled for Push temperatures 0 = THERM assertions disabled for Push temperatures
<6>	SMBus THERM	R/W	1 = THERM assertions enabled for SMBus slave temperatures 0 = THERM assertions disabled for SMBus slave temperatures
<7>	Reserved	R	

Table 43. REGISTER 0x17 − THERM Configuration Register 2 (Power−On Default = 0x07)

Bit	Mnemonic	R/W	Description
<0>	P1TH	R/W	If set to 1 then PWM1 will respond to THERM events
<1>	P2TH	R/W	If set to 1 then PWM2 will respond to THERM events
<2>	P3TH	R/W	If set to 1 then PWM3 will respond to THERM events
<3>	Reserved	R	
<4>	Reserved	R	
<5>	Reserved	R	
<6>	Reserved	R	
<7>	Reserved	R	

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Table 44. REGISTER 0x18 – THERM Configuration Register 3 (Power−On Default = 0x00)

Bit	Mnemonic	R/W	Description
<3:0>	SMBSTEP	R/W	Sets the Step size used by the THERM stepping function when applied to SMBus Master device THERM assertions
<7:4>	PECSTEP	R/W	Sets the Step size used by the THERM stepping function when applied to PECI Tcontrol assertions

Table 45. REGISTER 0x19 – THERM Configuration Register 4 (Power−On Default = 0x00)

Bit	Mnemonic	R/W	Description
<3:0>	SNRSTEP	R/W	Sets the Step size used by the THERM stepping function when applied to Remote1/Local/ Remote2 sensor THERM assertions
<7:4>	PSHSTEP	R/W	Sets the Step size used by the THERM stepping function when applied to Push temperature THERM assertions

Table 46. PECI READING REGISTERS (Power−On Default = 0x80)

Register Address	R/W	Description
0x33	R	PECI0: This register reads the 8 bits representative of PECI0
0x1A	R	PECI1: This register reads the 8 bits representative of PECI1
0x1B	R	PECI2: This register reads the 8 bits representative of PECI2
0x1C	R	PECI3: This register reads the 8 bits representative of PECI 3

Table 47. DEVICE ID REGISTER (Power−On Default = 0x91)

Register Address	R/W	Description	Power−On Default
0x1D	R	Device ID	0x91

Table 48. V_{TT} READING REGISTER (Power−On Default = 0x00)

Register Address	R/W	Description
0x1E	R	Reflects the voltage measurement at the V_{TT} input on Pin 8 of the QSOP package, Pin 5 of the QFN package (8 MSBs of reading). Input range of 0 to 2v

Table 49. REGISTER 0x1F EXTENDED RESOLUTION 3 (Power−On Default = 0x00)

Bits	R/W	Description
<3:0>	R	RESERVED
<5:4>	R	Bits <5:4> hold the two LSB's of the 10−bit V_{TT} measurement
<7:6>	R	RESERVED

Table 50. VOLTAGE READING REGISTERS (Power−On Default = 0x00) (Note 7)

Register Address	R/W	Description
0x20	R	Reflects the voltage measurement at the 2.5 V input on Pin 22 of the QSOP package, Pin 19 of the QFN package (8 MSBs of reading).
0x21	R	Reflects the voltage measurement (Note 8) at the V_{CCP} input on Pin 23 of the QSOP package, Pin 20 of the QFN package (8 MSBs of reading).
0x22	R	Reflects the voltage measurement (Note 9) at the V_{CC} input on Pin 4 of the QSOP package, Pin 1 of the QFN package (8 MSBs of reading).
0x23	R	Reflects the voltage measurement at the 5 V input on Pin 20 of the QSOP package, Pin 17 of the QFN package (8 MSBs of reading).
0x24	R	Reflects the voltage measurement at the 12 V input on Pin 21 of the QSOP package, Pin 18 of the QFN package (8 MSBs of reading).

7. If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
8. If V_{CCP}Low (Bit 6 of 0x10) is set, V_{CCP} can control the sleep state of the NCT7491.
9. V_{CC} (Pin 4 on the QSOP package, Pin1 on the QFN package) is the supply voltage for the NCT7491.

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Table 51. TEMPERATURE READING REGISTERS (Power−On Default = 0x80) (Notes 10, 11, 12)

Register Address	R/W	Description
0x25	R	Remote 1 temperature reading (Notes 12, 13) (8 MSB of reading).
0x26	R	Local temperature reading (8 MSB of reading).
0x27	R	Remote 2 temperature reading (Notes 12, 13) (8 MSB of reading).

10. If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
11. These temperature readings can be in twos complement or offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
12. In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
13. In offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 52. FAN TACHOMETER READING REGISTERS (Power−On Default = 0x00) (Note 14)

Register Address	R/W	Description
0x28	R	TACH1 low byte.
0x29	R	TACH1 high byte.
0x2A	R	TACH2 low byte.
0x2B	R	TACH2 high byte.
0x2C	R	TACH3 low byte.
0x2D	R	TACH3 high byte.
0x2E	R	TACH4 low byte.
0x2F	R	TACH4 high byte.

14. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the fan pulses per revolution register (Reg. 0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes be read, the low byte *must* be read first. Both the low and high bytes are then frozen until read. At power−on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up. A count of 0xFFFF indicates that a fan is one of the following: stalled or blocked (object jamming the fan), failed (internal circuitry destroyed), or not populated. (The NCT7491 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFF.)

Table 53. CURRENT PWM DUTY CYCLE REGISTERS (Power−On Default = 0xFF) (Note 15)

Register Address	R/W	Description
0x30	R/W	PWM1 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x31	R/W	PWM2 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x32	R/W	PWM3 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).

15. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the NCT7491 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In manual mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 54. REGISTER 0x33 PECI0 READING REGISTER (Power−On Default = 0x80)

Register Address	R/W	Description
0x33	R	PECI0: This register reads the 8 bits representative of PECI Client Address stored in register 0x00

Table 55. PECI LIMIT REGISTERS REGISTER

Register Address	R/W	Description	Power−On Default
0x34	R/W	PECI Low Limit	0x81
0x35	R/W	PECI High Limit	0x00

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Table 56. REGISTER 0x36 PECI CONFIGURATION REGISTER 1 (Power−On Default = 0x00)

BIT	NAME	R/W	Description	
<2:0>	AVG	R/W	PECI Averaging Count	
			Code	Averaged Samples
			000	1
			001	2
			010	4
			011	8
			100	Reserved
			101	Reserved
			110	Reserved
			111	Reserved
<3>	DOM0	R/W	CPU Domain Count information. Set to 0 indicates that CPU 1 associated with the PECI0 reading has a single domain (Default). Set to 1 indicates that the system CPU 1 contains two domains.	
<4>	Reserved			
<5>	Reserved			
<7:6>	Reserved			

Table 57. REGISTER 0x37 PECI CONFIGURATION REGISTER 3 (Power−On Default = 0x32)

Bit	Name	R/W	Description
<0>	PDET	R/W	1 = at least one PECI enabled processor detected 0 = no processors detected
<1>	RTYDIS	R/W	1 = PECI retry bit is disabled 0 = PECI retry bit is enabled This bit allows the user to disable the PECI retry bit for any subsequent commands following a bad Completion Code from the CPU. It is enabled by default.
<2>	Reserved	R	
<3>	Reserved	R	
<5:4>	Rate	R/W	PECI update rate 00 = 1/sec 01 = 2/sec 10 = 5/sec 11 = 10/sec
<6>	Reserved		
<7>	PWEN	R/W	1=PECI CPU writes are enabled 0=PECI CPU writes are disabled

Table 58. MAXIMUM PWM DUTY CYCLE (Power−On Default = 0xFF) (Note 16)

Register Address	R/W[2]	Description
0x38	R/W	Maximum duty cycle for PWM1 output, default = 100% (0xFF.)
0x39	R/W	Maximum duty cycle for PWM2 output, default = 100% (0xFF).
0x3A	R/W	Maximum duty cycle for PWM3 output, default = 100% (0xFF).

16. These registers set the maximum PWM duty cycle of the PWM output.

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Table 59. PECI T_{MIN} REGISTER (Power−On Default = 0x80)

Register Address	R/W	Description	Power−On Default
0x3B	R/W	PECI T_{MIN} When the PECI measurement exceeds PECI T_{MIN} the appropriate fans run at PWM_{MIN} and increase according to the automatic fan speed control slope. If Absolute PECI mode is used then the maximum valid Tmin value is 175°C.	0xD6 (−42°C)

Table 60. REGISTER 0x3C − PECI T_{RANGE} (Power−On Default = 0xC0)

Bit	Name	R/W[1]	Description
<2:0>	Reserved	R	
< 3 >	Reserved	R	
<7:4>	T_{RANGE}	R/W	These bits determine the PWM duty cycle vs. the PECI temperature range for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

Table 61. PECI0 $T_{CONTROL}$ LIMIT REGISTER (Note 17)

Register Address	R/W	Description	Power−On Default
0x3D	R/W	PECI0 $T_{CONTROL}$ limit.	0x00

17. If any PECI reading exceeds the $T_{CONTROL}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail−safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below T_{CONTRO} limit − hysteresis.

Table 62. COMPANY ID REGISTER

Register Address	R/W	Description	Power−On Default
0x3E	Read	Company ID	0x1A

Table 63. REGISTER 0x3F VERSION/REVISION REGISTER (Power−On−Default = 0x6C)

Bit	Name	R/W	Description
<1:0>	REV	Read	These two bits indicate the NCT7491 silicon revision number. 0x00 indicates rev 0, 0x01 indicates Rev 1 etc…
<2>	PECI	Read	This bit is set to 1 indicating that the NCT7491 supports the PECI interface
<3>	4 Wire	Read	This bit is set to 1 indicating that the NCT7491 may be configured to drive 4−wire fans using high frequency PWM.
<7:4>	VER	Read	These bits indicate the Heceta version number of the device.

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Table 64. REGISTER 0x40 − Configuration Register 1 (Power−On Default = 0x84)

Bit	Name	R/W	Description
<0>	STRT (Notes 18, 19)	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control is based on the default power−up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK bit) has been set.
<1>	LOCK	Write once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the NCT7491 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
<2>	RDY	R	This bit is set to 1 by the NCT7491 to indicate that the device is fully powered−up and ready to begin system monitoring.
<3>	Fan Boost	R/W	When this bit is set to logic 1 all PWM outputs go to 100% regardless of other fan speed configurations and automatic fan speed control settings. When this bit is set to 0 the fan speed control returns to the fan speed setting calculated by the pre−programmed fan speed control settings. This bit remains writable after the lock bit is set.
<4>	PECI Monitor	R/W	Set this bit to logic 1 to enable CPU thermal monitoring via PECI interface. This bit becomes read only when the lock bit is set.
<5>	THERM Override	R/W	When this bit is set to logic 1, any $\overline{\text{THERM}}$ pin assertion will cause the fans to go to 100% or Max PWM, depending on bits <4:2> of register 0x16, overriding any other fan setting, even when the PWM's are configured for manual mode, or disabled. This bit becomes read only when the lock bit is set.
<7:6>	AVELN	R/W	Sets the averaging length for all analog channels 00 = 4 readings per averaged value 01 = 8 readings per averaged value 10 = 16 readings per averaged value 11 = 32 readings per averaged value

18. Bit 0 (STRT) of Configuration Register 1 (0x40) remains writable after lock bit is set.
19. When monitoring (STRT) is disabled, PWM outputs always go to 100% for thermal protection.

Table 65. REGISTER 0x41 − Interrupt Status Register 1 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	2.5 V	R	2.5 V = 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	V_{CCP}	R	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<2>	V_{CC}	R	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<3>	5 V	R	A 1 indicates that the 5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<4>	RIT	R	RIT = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	R	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<6>	R2T	R	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	R	OOL = 1 indicates that an out−of−limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2 (0x42). Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out−of−limit, which eliminates the need to read Status Register 2 during every interrupt or polling cycle.

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Table 66. REGISTER 0x42 – Interrupt Status Register 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	12 V	R	A 1 indicates that the 12 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	OOL	R	OOL = 1 indicates that an out−of−limit event has been latched in Status Register 3 (0x43). This bit is a logical OR of all status bits in Status Register 3 Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 3 are out−of−limit, which eliminates the need to read Status Register 3 during every interrupt or polling cycle.
<2>	FAN1	R	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM 1 output is off.
<3>	FAN2	R	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM 2 output is off.
<4>	FAN3	R	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM 3 output is off.
<5>	FAN4	R	When Pin 14 on the QSOP package, Pin 11 on the QFN package is programmed as a TACH4 input, FAN4 = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
<6>	D1	R	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	R	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 67. REGISTER 0x43 – Interrupt Status Register 3 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PECI0	R	A logic 1 indicates that the PECI high or low limit has been exceeded by the PECI value from PECI client address 0x30. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	Data	R	A logic 1 indicates that valid PECI data cannot be obtained for the processor and a specified error code has been recorded.
<2>	Comm	R	A logic 1 indicates that there is a communications error (e.g. invalid FCS) on the PECI interface.
<3>	OVT	R	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ over temperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ − T_{HYST}.
<6:4>	DAT	R	If a DATA error occurs then bits <6:4> indicate the error type <000> = General sensor error (0x8000) <001> = Sensor underflow (0x8002) <010> = Sensor overflow (0x8003) <111> = Other
<7>	OOL3	R	OOL3 = 1 indicates that an out−of−limit event has been latched in Status Register 4 (0x81). This bit is a logical OR of all status bits in Status Register 4 Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 4 are out−of−limit, which eliminates the need to read Status Register 4 during every interrupt or polling cycle.

Table 68. VOLTAGE LIMIT REGISTERS (Note 20)

Register Address	R/W	Description (Note 21)	Power−On Default
0x44	R/W	2.5 V low limit.	0x00
0x45	R/W	2.5 V high limit.	0xFF
0x46	R/W	V_{CCP} low limit.	0x00
0x47	R/W	V_{CCP} high limit.	0xFF
0x48	R/W	V_{CC} low limit.	0x00
0x49	R/W	V_{CC} high limit.	0xFF
0x4A	R/W	5 V low limit.	0x00
0x4B	R/W	5 V high limit.	0xFF
0x4C	R/W	12 V low limit.	0x00
0x4D	R/W	12 V high limit.	0xFF

20. Setting the Configuration Register 1 lock bit has no effect on these registers.
21. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

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Table 69. TEMPERATURE LIMIT REGISTERS (Note 22)

Register Address	R/W	Description (Note 23)	Power−On Default
0x4E	R/W	Remote 1 temperature low limit.	0x81
0x4F	R/W	Remote 1 temperature high limit.	0x7F
0x50	R/W	Local temperature low limit.	0x81
0x51	R/W	Local temperature high limit.	0x7F
0x52	R/W	Remote 2 temperature low limit.	0x81
0x53	R/W	Remote 2 temperature high limit.	0x7F

22. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 lock bit has no effect on these registers.
23. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 70. FAN TACHOMETER LIMIT REGISTERS (Note 24)

Register Address	R/W	Description	Power−On Default
0x54	R/W	TACH1 minimum low byte.	0xFF
0x55	R/W	TACH1 minimum high byte	0xFF
0x56	R/W	TACH2 minimum low byte.	0xFF
0x57	R/W	TACH2 minimum high byte.	0xFF
0x58	R/W	TACH3 minimum low byte.	0xFF
0x59	R/W	TACH3 minimum high byte.	0xFF
0x5A	R/W	TACH4 minimum low byte.	0xFF
0x5B	R/W	TACH4 minimum high byte.	0xFF

24. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure.

Table 71. PWM CONFIGURATION REGISTERS

Register Address		R/W	Description	Power−On Default
0x5C		R/W	PWM1 configuration.	0x02
0x5D		R/W	PWM2 configuration.	0x02
0x5E		R/W	PWM3 configuration.	0x02
Bit	Name	R/W	Description	
<2:0>	SPIN	R/W	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, then the TACH measurement reads 0xFFFF and Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, then the Status Register 2 bit is not set, even if the fan has not started.	
			000 = No startup timeout	
			001 = 100 ms	
			010 = 250 ms (default)	
			011 = 400 ms	
			100 = 667 ms	
			101 = 1 sec	
			110 = 2 sec	
			111 = 4 sec	
<3>	Reserved			
<4>	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output, so 100% duty cycle corresponds to a logic low output.	
<7:5>	Reserved			

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Table 72. TEMP TRANGE/PWM FREQUENCY REGISTERS

Register Address		R/W	Description	Power−On Default
0x5F		R/W	Remote 1 T_{RANGE}/PWM1 frequency.	0xC3
0x60		R/W	Local temperature T_{RANGE}/PWM2 frequency.	0xC3
0x61		R/W	Remote 2 T_{RANGE}/PWM3 frequency.	0xC3
Bit	**Name**	**R/W**	**Description**	
<2:0>	FREQ	R/W	These bits control the PWMx frequency (only apply when PWM channel is in low frequency mode).	
			000 = 11.0 Hz	
			001 = 14.7 Hz	
			010 = 22.1 Hz	
			011 = 29.4 Hz (default)	
			100 = 35.3 Hz	
			101 = 44.1 Hz	
			110 = 58.8 Hz	
			111 = 88.2 Hz	
<3>	HF/LF	R/W	HF/LF = 1, High frequency PWM mode is enabled for PWMx. HF/LF = 0, Low frequency PWM mode is enabled for PWMx.	
<7:4>	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control.	
			0000 = 2°C	
			0001 = 2.5°C	
			0010 = 3.33°C	
			0011 = 4°C	
			0100 = 5°C	
			0101 = 6.67°C	
			0110 = 8°C	
			0111 = 10°C	
			1000 = 13.33°C	
			1001 = 16°C	
			1010 = 20°C	
			1011 = 26.67°C	
			1100 = 32°C (default)	
			1101 = 40°C	
			1110 = 53.33°C	
			1111 = 80°C	

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Table 73. REGISTER 0x62 – Enhanced Acoustics Register 1 (Power−On Default = 0x20)

Bit	Name	R/W	Description	
<2:0>	ACOU	R/W	These bits define the maximum rate of change of the PWM1 output. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			Time Slot Increase	Time for 0% to 100%
			000 = 1	37.5 sec
			001 = 2	18.8 sec
			010 = 3	12.5 sec
			011 = 4	7.5 sec
			100 = 8	4.7 sec
			101 = 12	3.1 sec
			110 = 24	1.6 sec
			111 = 48	0.8 sec
<3>	EN1	R/W	When this bit is 1, smoothing is enabled on PWM1 output.	
<4>	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.	
<5>	MIN1	R/W	When the NCT7491 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM1 minimum duty cycle below T_{MIN} – hysteresis.	
<6>	MIN2	R/W	When the NCT7491 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM 2 minimum duty cycle below T_{MIN} – hysteresis.	
<7>	MIN3	R/W	When the NCT7491 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM3 minimum duty cycle below T_{MIN} – hysteresis.	

Table 74. REGISTER 0x63 – Enhanced Acoustics Register 2 (Power−On Default = 0x00)

Bit	Name	R/W (Note 25)	Description	
<2:0>	ACOU3	R/W	These bits define the maximum rate of change of the PWM3 output. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			Time Slot Increase	Time for 0% to 100%
			000 = 1	37.5 sec
			001 = 2	18.8 sec
			010 = 3	12.5 sec
			011 = 4	7.5 sec
			100 = 8	4.7 sec
			101 = 12	3.1 sec
			110 = 24	1.6 sec
			111 = 48	0.8 sec
< 3 >	EN3	R/W	When this bit is 1, smoothing is enabled on the PWM3 output.	

25. These registers become read−only when the NCT7491 is in automatic fan control mode.

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Table 74. REGISTER 0x63 – Enhanced Acoustics Register 2 (Power−On Default = 0x00)

Bit	Name	R/W (Note 25)	Description	
<6:4>	ACOU2	R/W	These bits define the maximum rate of change of the PWM2 output. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			Time Slot Increase	Time for 0% to 100%
			000 = 1	37.5 sec
			001 = 2	18.8 sec
			010 = 3	12.5 sec
			011 = 4	7.5 sec
			100 = 8	4.7 sec
			101 = 12	3.1 sec
			110 = 24	1.6 sec
			111 = 48	0.8 sec
<7>	EN2	R/W	When this bit is 1, smoothing is enabled on the PWM2 output.	

25. These registers become read−only when the NCT7491 is in automatic fan control mode.

Table 75. PWM MINIMUM DUTY CYCLE REGISTERS

Register Address		R/W (Note 26)	Description	Power−On Default
0x64		R/W	PWM1 minimum duty cycle.	0x80 (50% duty cycle)
0x65		R/W	PWM2 minimum duty cycle.	0x80 (50% duty cycle)
0x66		R/W	PWM3 minimum duty cycle.	0x80 (50% duty cycle)
Bit	**Name**	**R/W** (Note 26)	**Description**	
<7:0>	PWM duty cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx.	
			0x00 = 0% duty cycle (fan off).	
			0x40 = 25% duty cycle.	
			0x80 = 50% duty cycle.	
			0xFF = 100% duty cycle (fan full speed).	

26. These registers become read−only when the NCT7491 is in automatic fan control mode.

Table 76. T_{MIN} REGISTERS (Note 27)

Register Address	R/W	Description	Power−On Default
0x67	R/W	Remote 1 Temperature T_{MIN}.	0x5A (90°C)
0x68	R/W	Local Temperature T_{MIN}.	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T_{MIN}.	0x5A (90°C)

27. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.

Table 77. $\overline{\text{THERM}}$ LIMIT REGISTERS (Note 28)

Register Address	R/W	Description	Power−On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ limit.	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ limit.	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ limit.	0x64 (100°C)

28. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail−safe mechanism incorporated to cool the system in the event of a critical over temperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ limit − hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.

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Table 78. TEMPERATURE/T_{MIN} HYSTERESIS REGISTERS (Note 29)

Register Address	R/W	Description	Power−On Default
0x6D	R/W	Remote 1 and Local Temperature hysteresis.	0x44
<3:0>	HYSL	Local Temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Local temperature AFC control loops.	
<7:4>	HYSR1	Remote 1 Temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 Temperature AFC control loops.	
0x6E	R/W	PECI and Remote 2 Temperature hysteresis.	0x44
<3:0>	HYSP	PECI Temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the PECI AFC control loops.	
<7:4>	HYSR2	Remote 2 Temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Local Temperature AFC control loops.	

29. Each 4−bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel, if its $\overline{THERM}$ limit is exceeded. The PWM output being controlled goes to 100%, if the $\overline{THERM}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{THERM}$ − hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.

Table 79. REGISTER 0x6F − XNOR Tree Test Enable (Power−On Default = 0x00)

Register Address	R/W (Note 30)	Description
<0>	XEN	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.
<7:1>	Reserved	Unused. Do not write to these bits.

30. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 80. REMOTE 1 TEMPERATURE OFFSET (Note 31)

Register Address	R/W (Note 31)	Description	Power−On Default
0x70	R/W	Remote 1 temperature offset.	0x00
<7:0>	R/W	Allows a temperature offset to be automatically applied to the remote temperature 1 channel measurement. Bit 1 of 0x7C (Configuration Register 5) determines the range and resolution of this register.	

31. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 81. LOCAL TEMPERATURE OFFSET (Note 32)

Register Address	R/W (Note 32)	Description	Power−On Default
0x71	R/W	Local temperature offset.	0x00
<7:0>	R/W	Allows a temperature offset to be automatically applied to the local temperature measurement. Bit 1 of 0x7C (Configuration Register 5) determines the range and resolution of this register.	

32. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 82. REMOTE 2 TEMPERATURE OFFSET (Note 33)

Register Address	R/W (Note 33)	Description	Power−On Default
0x72	R/W	Remote 2 temperature offset.	0x00
<7:0>	R/W	Allows a temperature offset to be automatically applied to the remote temperature 2 channel measurement. Bit 1 of 0x7C (Configuration Register 5) determines the range and resolution of this register.	

33. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

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Table 83. REGISTER 0x73 – Configuration Register 2 (Power–On Default = 0x00) (Note 34)

Bit	Name	R/W (Note 34)	Description
0	Reserved	R	
1	Reserved	R	
2	ABS/REL	R/W	0 = PECI uses relative values for fan control 1 = PECI uses absolute value for fan control
3	VAVG	R/W	VAVG = 1 indicates that averaging on the voltage measurements is turned off. This allows measurements on each channel to be made much faster.
4	TAVG	R/W	TAVG = 1 indicates that averaging on the temperature measurements is turned off. This allows measurements on each channel to be made much faster.
<6:5>	FQ	R/W	Sets the fault queue length: <00> = 1 event <01> = 2 events <10> = 3 events <11> = 4 events
7	Shutdown	R/W	

34. This register becomes read–only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 84. REGISTER 0x74 – Interrupt Mask Register 1 (Power–On Default = 0x00)

Bit	Name	R/W	Description
0	2.5 V	R/W	2.5 V = 1, masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the 2.5 V channel.
1	V_{CCP}	R/W	V_{CCP} = 1 masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the V_{CCP} channel.
2	V_{CC}	R/W	V_{CC} = 1 masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the V_{CC} channel.
3	5 V	R/W	5 V = 1 masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the 5 V channel.
4	RIT	R/W	RIT = 1 masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the Remote 1 Temperature channel.
5	LT	R/W	LT = 1 masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the Local Temperature channel.
6	R2T	R/W	R2T = 1 masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the Remote 2 Temperature channel.
7		R	Reserved

Table 85. REGISTER 0x75 – Interrupt Mask Register 2 (Power–On Default = 0x00)

Bit	Name	R/W	Description
0	12 V	R/W	12 V = 1, masks $\overline{\text{SMBALERT}}$ for out–of–limit conditions on the 12 V channel.
1		R	Reserved
2	FAN1	R/W	FAN1 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
3	FAN2	R/W	FAN2 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
4	FAN3	R/W	FAN3 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
5	FAN4	R/W	FAN4 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault.
6	D1	R/W	D1 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 1 channel.
7	D2	R/W	D2 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 2 channel.

Table 86. REGISTER 0x76 – Extended Resolution Register 1 (Note 35) **(Power–On Default = 0x00)**

Bit	Name	R/W	Description
<1:0>	2.5 V	R	2.5 V LSBs. Holds the 2 LSBs of the 10–bit 2.5 V measurement.
<3:2>	V_{CCP}	R	V_{CCP} LSBs. Holds the 2 LSBs of the 10–bit V_{CCP} measurement.
<5:4>	V_{CC}	R	V_{CC} LSBs. Holds the 2 LSBs of the 10–bit V_{CC} measurement.
<7:6>	5 V	R	5 V LSBs. Holds the 2 LSBs of the 10–bit 5 V measurement.

35. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

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Table 87. REGISTER 0x77 – Extended Resolution Register 2 (Note 36) **(Power−On Default = 0x00)**

Bit	Name	R/W	Description
<1:0>	12 V	R	12 V LSBs. Holds the 2 LSBs of the 10−bit 12 V measurement.
<3:2>	TDM1	R	Remote 1 Temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 1 temperature measurement.
<5:4>	LTMP	R	Local Temperature LSBs. Holds the 2 LSBs of the 10−bit local temperature measurement.
<7:6>	TDM2	R	Remote 2 Temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 2 temperature measurement.

36. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 88. REGISTER 0x78 – Configuration Register 3 (Power−On Default = 0x00)

Bit	Name	R/W (Note 37)	Description
<0>	ALERT	R/W	ALERT = 1, Pin 10 on the QSOP package, Pin 7 on the QFN package (PWM2/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out−of−limit error conditions. ALERT = 0, Pin 10 on the QSOP package, Pin 7 on the QFN package (PWM2/$\overline{\text{SMBALERT}}$) is configured as the PWM2 output.
<1>	$\overline{\text{THERM}}$ / 2.5 V	R/W	$\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ functionality on Pin 22 on the QSOP package, Pin 19 on the QFN package
<2>	Reserved	R	
<3>	FAST	R/W	FAST = 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4 x).
<4>	DC1	R/W	DC1 = 1 enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
<5>	DC2	R/W	DC2 = 1 enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
<6>	DC3	R/W	DC3 = 1 enables TACH measurements to be continuously made on TACH3. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
<7>	DC4	R/W	DC4 = 1 enables TACH measurements to be continuously made on TACH4. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.

37. Bits <3:0> of this register become read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to bits <3:0> have no effect.

Table 89. REGISTER 0x79 – $\overline{\text{THERM}}$ Timer Value Register (Power−On Default = 0x00)

Bit	Name	R/W	Description
<7:1>	TMR	R	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read zero until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
<0>	ASRT/ TMR0	R	This bit is set high on the assertion of the $\overline{\text{THERM}}$ input and is cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8−bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 sec to be reported back with a resolution of 22.76 ms.

Table 90. REGISTER 0x7A – $\overline{\text{THERM}}$ Timer Limit Register (Power−On Default = 0xFF)

Bit	Name	R/W	Description
<7:0>	LIMT	R/W	Sets maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8−bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 s to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (Reg. 0x42) is set. If the limit value is 0x00, an interrupt is generated immediately on the assertion of the $\overline{\text{THERM}}$ input. If $\overline{\text{THERM}}$ is configured as an output the $\overline{\text{THERM}}$ timer limit should be set to 0xFF to avoid unwanted alerts from being generated.

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Table 91. REGISTER 0x7B − TACH Pulses per Revolution Register (Power−On Default = 0x55)

Bit	Name	R/W	Description
<1:0>	FAN1	R/W	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4
<3:2>	FAN2	R/W	Sets number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4
<5:4>	FAN3	R/W	Sets number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4
<7:6>	FAN4	R/W	Sets number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4

Table 92. REGISTER 0x7C − Configuration Register 5 (Power−On Default = 0x05)

Bit	Name	R/W (Note 38)	Description
<0>	2sC	R/W	2sC = 1 sets the temperature range to the twos complement temperature range. 2sC = 0 changes the temperature range to the offset 64 temperature range. When this bit is changed, the NCT7491 interprets all relevant temperature register values as defined by this bit.
<1>	TempOffset	R/W	TempOffset = 0 sets offset range to −63C to +64C with 0.5°C resolution. TempOffset = 1 sets offset range to −63°C to +127°C with 1°C resolution. These settings apply to registers 0x70, 0x71, and 0x72 (Remote 1, Internal and Remote2 Temperature offset registers. Note: PECI offset is always 1°C resolution.)
<3:2>	Pin19 Function	R/W	00 = Pin 19 is $\overline{\text{SMBALERT}}$ 01 = Pin 19 is THERM 10 = Pin 19 is GPIO3 11 = reserved **Note:** Pin 19 refers to the QSOP package. The equivalent pin on the QFN package is pin 16.

38. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

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Table 92. REGISTER 0x7C − Configuration Register 5 (Power−On Default = 0x05)

Bit	Name	R/W (Note 38)	Description
<4>	PECI $\overline{T_{CONTROL}}$	R/W	PECI = 1 enables $\overline{THERM}$ assertions when the PECI temperature read is higher than the PECI $T_{CONTROL}$ limit and the $\overline{THERM}$ pin is bidirectional. If $\overline{THERM}$ is configured as an output the $\overline{THERM}$ timer limit (register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. PECI = 0 indicates that the $\overline{THERM}$ pin is configured as a timer input only. Can also be disabled by writing −128°C to the relevant PECI $T_{CONTROL}$ limit register.
<5>	R1 $\overline{THERM}$	R/W	R1 = 1 enables $\overline{THERM}$ assertions when the Remote 1 temperature read is higher than the Remote 1 $\overline{THERM}$ limit and the $\overline{THERM}$ pin is bidirectional. If $\overline{THERM}$ is configured as an output the $\overline{THERM}$ timer limit (register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. R1 = 0 indicatesthat the $\overline{THERM}$ pin is configured as a timer input only. can also be disabled by writing one of the below values to the Remote 1 $\overline{THERM}$ limit register (0x6A): Writing −64°C in offset 64 mode. Writing −128°C in twos complement mode.
<6>	Local $\overline{THERM}$	R/W	Local = 1 enables $\overline{THERM}$ assertions when the Local temperature read is higher than the Local $\overline{THERM}$ limit and the $\overline{THERM}$ pin is bidirectional. If $\overline{THERM}$ is configured as an output the $\overline{THERM}$ timer limit (register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. can also be disabled by writing one of the below values to the Remote 1 $\overline{THERM}$ limit register (0x6B): Writing −64°C in offset 64 mode. Writing −128°C in twos complement mode.
<7>	R2 $\overline{THERM}$	R/W	R2 = 1 enables $\overline{THERM}$ assertions when the Remote 2 temperature read is higher than the Remote 2 $\overline{THERM}$ limit and the $\overline{THERM}$ pin is bidirectional. If $\overline{THERM}$ is configured as an output the $\overline{THERM}$ timer limit (register 0x7A) should be set to 0xFF to avoid unwanted alerts from being generated. can also be disabled by writing one of the below values to the Remote 1 $\overline{THERM}$ limit register (0x6C): Writing −64°C in offset 64 mode. Writing −128°C in twos complement mode.

38. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 93. REGISTER 0x7D − Configuration Register 4 (Power−On Default = 0x00)

Bit	Name	R/W (Note 39)	Description
<1:0>	PIN14FUNC	R/W	These bits set the functionality of Pin 14: 00 = TACH4 (default) 01 = $\overline{THERM}$ 10 = $\overline{SMBALERT}$ 11 = RESERVED **Note:** Pin 14 refers to the QSOP package. The equivalent pin on the QFN package is pin 11.
<2>	$\overline{THERM}$ Disable	R/W	$\overline{THERM}$ Disable = 0 enables $\overline{THERM}$ overtemperature output assuming $\overline{THERM}$ is correctly configured (registers 0x78, 0x7C, 0x7D). $\overline{THERM}$ Disable = 1 disables $\overline{THERM}$ overtemperature output on all channels. $\overline{THERM}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{THERM}$ temperature limit in offset 64 mode. Writing −128°C to the appropriate $\overline{THERM}$ temperature limit in twos complement mode.
<3>	BpAtt Vtt	R/W	Bypass Vtt attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2 V (0xFF).
<4>	BpAtt2.5 V	R/W	Bypass 2.5 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2 V (0xFF).
<5>	BpAttV_{CCP}	R/W	Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2 V (0xFF).
<6>	BpAtt5 V	R/W	Bypass 5 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2 V (0xFF).
<7>	BpAtt12 V	R/W	Bypass 12 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2 V (0xFF).

39. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

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Table 94. REGISTER 0x7E – Interrupt Status 5 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PUSH0	R	Logic 1 indicates ALERT assertion for Push0 temperature
<1>	PUSH1	R	Logic 1 indicates ALERT assertion for Push1 temperature
<2>	PUSH2	R	Logic 1 indicates ALERT assertion for Push2 temperature
<3>	PUSH3	R	Logic 1 indicates ALERT assertion for Push3 temperature
<4>	OVT_P0	R	Logic 1 indicates THERM assertion for Push0 temperature
<5>	OVT_P1	R	Logic 1 indicates THERM assertion for Push1 temperature
<6>	OVT_P2	R	Logic 1 indicates THERM assertion for Push2 temperature
<7>	OVT_P3	R	Logic 1 indicates THERM assertion for Push3 temperature

Table 95. REGISTER 0x7F – Interrupt Mask 5 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PUSH0	R/W	Logic 1 masks PUSH0 ALERT assertions
<1>	PUSH1	R/W	Logic 1 masks PUSH1 ALERT assertions
<2>	PUSH2	R/W	Logic 1 masks PUSH2 ALERT assertions
<3>	PUSH3	R/W	Logic 1 masks PUSH3 ALERT assertions
<4>	Reserved	R	Reserved
<5>	Reserved	R	Reserved
<6>	Reserved	R	Reserved
<7>	Reserved	R	Reserved

Table 96. REGISTER 0x80 – GPIO Register (Power−On Default = 0xCE)

Bit	Name	R/W	Description
<0>	RES	RESERVED	
<1>	GPEN		1= GPIO1 enabled on pin 5, GPIO2 enabled on pin 6 0 = GPIO1 and GPIO2 are disabled This bit only has effect if the SMBus master port is disabled (0xB5 <0> =0)
<2>	GPIO2	R/W	If GPIO2 is set to input, this register reflects the state of the pin. If GPIO2 is configured as an output, writing to this register asserts the output high or low depending on the polarity.
<3>	GPIO1	R/W	If GPIO1 is set to input, this register reflects the state of the pin. If GPIO1 is configured as an output, writing to this register asserts the output high or low depending on the polarity.
<4>	GPIO2 POL	R/W	GPIO2 polarity bit. Set to 0 for active low. Set to1 for active high.
<5>	GPIO1 POL	R/W	GPIO1 polarity bit. Set to 0 for active low. Set to1 for active high.
<6>	GPIO2 DIR	R/W	GPIO2 direction bit. Set to 1 for GPIO2 to act as an input, set to 0 for GPIO2 to act as an output.
<7>	GPIO1 DIR	R/W	GPIO1 direction bit. Set to 1 for GPIO1 to act as an input, set to 0 for GPIO1 to act as an output.

Table 97. REGISTER 0x81 – Interrupt Status Register 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PCC	R	PECI Completion code interrupt
<1>	TTS	R	Logic 1 indicates that the THERM Timer limit has been exceeded.
<2>	GCOMM	R	Logic 1 indicates a COMM error resulting from a Generic PECI instruction
<3>	PECI1	R	A logic 1 indicates that the PECI high or low limit has been exceeded by the PECI1 value.
<4>	PECI2	R	A logic 1 indicates that the PECI high or low limit has been exceeded by the PECI2 value.
<5>	PECI3	R	A logic 1 indicates that the PECI high or low limit has been exceeded by the PECI3 value.

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Table 97. REGISTER 0x81 – Interrupt Status Register 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<6>	SMBCNT	R	Logic 1 indicates that the byte count returned by the SMBus Master Block Read is too low. If the PCH temperature only is required then the returned byte count should be 2 or greater. If DIMM temperatures are being read from the PCH then the returned byte count should be 9 or greater.
<7>	V_{TT}	R	A logic 1 indicates that the V_{TT} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.

Table 98. REGISTER 0x82 – Interrupt Mask Register 3 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PECI0	R/W	A logic 1 masks $\overline{\text{SMBALERT}}$ assertions for out−of−limit conditions on PECI0.
<1>	DATA	R/W	A logic 1 masks $\overline{\text{SMBALERT}}$ assertions for PECI Data errors. This also disables the fan over−ride function for PECI errors.
<2>	COMM	R/W	A logic 1 masks $\overline{\text{SMBALERT}}$ assertions for PECI communications errors. This also disables the fan over−ride function for PECI errors.
<3>	OVT	R/W	OVT = 1 masks $\overline{\text{SMBALERT}}$ for over temperature $\overline{\text{THERM}}$ conditions.
<6:4>	RES	R/W	Reserved
<7>		R	Reserved

NOTE: If the mask bits in register 0x82 are set it is also necessary to set the OOL mask bit in register 0x75 to ensure the $\overline{\text{SMBALERT}}$ output is not asserted.

Table 99. REGISTER 0x83 – Interrupt Mask Register 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PCC	R/W	Logic 1 masks $\overline{\text{ALERT}}$ assertions for PECI completion codes.
<1>	TTS	R/W	Logic 1 masks assertions for THERM Timer status bit
<2>	GCOMM	R/W	Logic 1 masks the GCOMM PECI status bit
<3>	PECI1	R/W	A logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on PECI1.
<4>	PECI2	R/W	A logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on PECI2.
<5>	PECI3	R/W	A logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on PECI3.
<6>	SMBCNT	R/W	Logic 1 masks $\overline{\text{ALERT}}$ assertions for incorrect byte count values returned by the Block Read command
<7>	V_{TT}	R/W	A logic 1 masks $\overline{\text{ALERT}}$ assertions for out−of−limit conditions on V_{TT}.

NOTE: If the mask bits in register 0x83 are set it is also necessary to set the OOL mask bit in register 0x82 to ensure the $\overline{\text{SMBALERT}}$ output is not asserted.

Table 100. V_{TT} LOW LIMIT REGISTER

Register Address	R/W	Description	Power−On Default
0x84	R/W	V_{TT} Low Limit	0x00

Table 101. REGISTER 0x85 – GPIO Config2 (Power−On Default = 0x80)

Bit	Name	R/W	Description
<4:0>	Reserved		
<5>	GPIO3	R/W	If GPIO3 is set to input, this bit reflects the state of the pin. If GPIO3 is configured as an output, writing to this register asserts the output high or low depending on the polarity.
<6>	GPIO3 POL	R/W	GPIO3 polarity bit. Set to 0 for active low. Set to1 for active high.
<7>	GPIO3 DIR	R/W	GPIO3 direction bit. Set to 1 for GPIO3 to act as an input, set to 0 for GPIO3 to act as an output, OOL must also be masked.

Table 102. V_{TT} HIGH LIMIT REGISTER

Register Address	R/W	Description	Power−On Default
0x86	R/W	V_{TT} High Limit	0xFF

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Table 103. REGISTER 0x87 − Configuration 9 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PWM1OFF	R/W	1= Disables PWM1
<1>	PWM2OFF	R/W	1= Disables PWM2
<2>	PWM3OFF	R/W	1 = Disables PWM3
<3>	Reserved	R	
<4>	D0V	R/W	1 = DIMM0 is populated, must be set to enable DIMM0 temperature to be written to CPU
<5>	D1V	R/W	1 = DIMM1 is populated, must be set to enable DIMM1 temperature to be written to CPU
<6>	D2V	R/W	1 = DIMM2 is populated, must be set to enable DIMM2 temperature to be written to CPU
<7>	D3V	R/W	1 = DIMM3 is populated, must be set to enable DIMM3 temperature to be written to CPU

Table 104. REGISTER 0x88 − PECI Configuration Register 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<2:0>	RES	R	RESERVED
<3>	DOM3	R/W	CPU Domain Count information. Set to 0 indicates that CPU 4 associated with the PECI3 reading has a single domain (Default). Set to 1 indicates that the system CPU4 contains two domains.
<4>	DOM2	R/W	CPU Domain Count information. Set to 0 indicates that CPU 3 associated with the PECI2 reading has a single domain (Default). Set to 1 indicates that the system CPU3 contains two domains.
<5>	DOM1	R/W	CPU Domain Count information. Set to 0 indicates that CPU 2 associated with the PECI1 reading has a single domain (Default). Set to 1 indicates that the system CPU2 contains two domains.
<7:6>	#CPU	R/W	CPU Count. These bits indicate the number of CPU's in the system. That will provide PECI thermal information to the NCT7491. 00 = 1 CPU 01 = 2 CPUs 10 = 3 CPUs 11 = 4 CPUs

Table 105. REGISTER 0x89 − Interrupt Status 7 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	OVT0	R	1 = PECI0 Tcontrol exceeded
<1>	OVT1	R	1 = PECI1 Tcontrol exceeded
<2>	OVT2	R	1 = PECI2 Tcontrol exceeded
<3>	OVT3	R	1 = PECI3 Tcontrol exceeded
<4>	OVT_R1	R	1 = Remote1 THERM exceeded
<5>	OVT_LOC	R	1 = Local THERM exceeded
<6>	OVT_R2	R	1 = Remote2 THERM exceeded
<7>	OOL11	R	1 indicates an out of limit condition in register 0xBB

Table 106. REGISTER 0x8A − PWM1 Source Control 1 (Power−On Default = 0x08)

Bit	Name	R/W	Description
<0>	LOC	R/W	Logic 1 enables Local temperature to control PWM1 in automatic fan control loop
<1>	REM1	R/W	Logic 1 enables Remote1 temperature to control PWM1 in automatic fan control loop
<2>	REM2	R/W	Logic 1 enables Remote2 temperature to control PWM1 in automatic fan control loop
<3>	PEC0	R/W	Logic 1 enables PECI0 temperature to control PWM1 in automatic fan control loop
<4>	PEC1	R/W	Logic 1 enables PECI1 temperature to control PWM1 in automatic fan control loop
<5>	PEC2	R/W	Logic 1 enables PECI2 temperature to control PWM1 in automatic fan control loop
<6>	PEC3	R/W	Logic 1 enables PECI3 temperature to control PWM1 in automatic fan control loop
<7>	Reserved		

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Table 107. REGISTER 0x8B – PWM1 Source Control 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	SMB0	R/W	Logic 1 enables SMBus Slave Device 0 to control PWM1 in automatic fan control loop
<1>	SMB1	R/W	Logic 1 enables SMBus Slave Device 1 to control PWM1 in automatic fan control loop
<2>	SMB2	R/W	Logic 1 enables SMBus Slave Device 2 to control PWM1 in automatic fan control loop
<3>	SMB3	R/W	Logic 1 enables SMBus Slave Device 3 to control PWM1 in automatic fan control loop
<4>	SMB4	R/W	Logic 1 enables SMBus Slave Device 4 to control PWM1 in automatic fan control loop
<5>	SMB5	R/W	Logic 1 enables SMBus Slave Device 5 to control PWM1 in automatic fan control loop
<6>	SMB6	R/W	Logic 1 enables SMBus Slave Device 6 to control PWM1 in automatic fan control loop
<7>	SMB7	R/W	Logic 1 enables SMBus Slave Device 7 to control PWM1 in automatic fan control loop

Table 108. REGISTER 0x8C – PWM1 Source Control 3 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PUSH0	R/W	Logic 1 enables Externally written temperature 0 to control PWM1 in automatic fan control loop
<1>	PUSH1	R/W	Logic 1 enables Externally written temperature 1 to control PWM1 in automatic fan control loop
<2>	PUSH2	R/W	Logic 1 enables Externally written temperature 2 to control PWM1 in automatic fan control loop
<3>	PUSH3	R/W	Logic 1 enables Externally written temperature 3 to control PWM1 in automatic fan control loop
<4>	Reserved		
<5>	Reserved		
<6>	Reserved		
<7>	Reserved		

Table 109. REGISTER 0x8D – PWM2 Source Control 1 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	LOC	R/W	Logic 1 enables Local temperature to control PWM2 in automatic fan control loop
<1>	REM1	R/W	Logic 1 enables Remote1 temperature to control PWM2 in automatic fan control loop
<2>	REM2	R/W	Logic 1 enables Remote2 temperature to control PWM2 in automatic fan control loop
<3>	PEC0	R/W	Logic 1 enables PECI0 temperature to control PWM2 in automatic fan control loop
<4>	PEC1	R/W	Logic 1 enables PECI1 temperature to control PWM2 in automatic fan control loop
<5>	PEC2	R/W	Logic 1 enables PECI2 temperature to control PWM2 in automatic fan control loop
<6>	PEC3	R/W	Logic 1 enables PECI3 temperature to control PWM2 in automatic fan control loop
<7>	Reserved		

Table 110. REGISTER 0x8E – PWM2 Source Control 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	SMB0	R/W	Logic 1 enables SMBus Slave Device 0 to control PWM2 in automatic fan control loop
<1>	SMB1	R/W	Logic 1 enables SMBus Slave Device 1 to control PWM2 in automatic fan control loop
<2>	SMB2	R/W	Logic 1 enables SMBus Slave Device 2 to control PWM2 in automatic fan control loop
<3>	SMB3	R/W	Logic 1 enables SMBus Slave Device 3 to control PWM2 in automatic fan control loop
<4>	SMB4	R/W	Logic 1 enables SMBus Slave Device 4 to control PWM2 in automatic fan control loop
<5>	SMB5	R/W	Logic 1 enables SMBus Slave Device 5 to control PWM2 in automatic fan control loop
<6>	SMB6	R/W	Logic 1 enables SMBus Slave Device 6 to control PWM2 in automatic fan control loop
<7>	SMB7	R/W	Logic 1 enables SMBus Slave Device 7 to control PWM2 in automatic fan control loop

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Table 111. REGISTER 0x8F – PWM2 Source Control 3 (Power–On Default = 0x00)

Bit	Name	R/W	Description
<0>	PUSH0	R/W	Logic 1 enables Externally written temperature 0 to control PWM2 in automatic fan control loop
<1>	PUSH1	R/W	Logic 1 enables Externally written temperature 1 to control PWM2 in automatic fan control loop
<2>	PUSH2	R/W	Logic 1 enables Externally written temperature 2 to control PWM2 in automatic fan control loop
<3>	PUSH3	R/W	Logic 1 enables Externally written temperature 3 to control PWM2 in automatic fan control loop
<4>	Reserved		
<5>	Reserved		
<6>	Reserved		
<7>	Reserved		

Table 112. REGISTER 0x90 – PWM3 Source Control 1 (Power–On Default = 0x00)

Bit	Name	R/W	Description
<0>	LOC	R/W	Logic 1 enables Local temperature to control PWM3 in automatic fan control loop
<1>	REM1	R/W	Logic 1 enables Remote1 temperature to control PWM3 in automatic fan control loop
<2>	REM2	R/W	Logic 1 enables Remote2 temperature to control PWM3 in automatic fan control loop
<3>	PEC0	R/W	Logic 1 enables PECI0 temperature to control PWM3 in automatic fan control loop
<4>	PEC1	R/W	Logic 1 enables PECI1 temperature to control PWM3 in automatic fan control loop
<5>	PEC2	R/W	Logic 1 enables PECI2 temperature to control PWM3 in automatic fan control loop
<6>	PEC3	R/W	Logic 1 enables PECI3 temperature to control PWM3 in automatic fan control loop
<7>	Reserved		

Table 113. REGISTER 0x91 – PWM3 Source Control 2 (Power–On Default = 0x00)

Bit	Name	R/W	Description
<0>	SMB0	R/W	Logic 1 enables SMBus Slave Device 0 to control PWM3 in automatic fan control loop
<1>	SMB1	R/W	Logic 1 enables SMBus Slave Device 1 to control PWM3 in automatic fan control loop
<2>	SMB2	R/W	Logic 1 enables SMBus Slave Device 2 to control PWM3 in automatic fan control loop
<3>	SMB3	R/W	Logic 1 enables SMBus Slave Device 3 to control PWM3 in automatic fan control loop
<4>	SMB4	R/W	Logic 1 enables SMBus Slave Device 4 to control PWM3 in automatic fan control loop
<5>	SMB5	R/W	Logic 1 enables SMBus Slave Device 5 to control PWM3 in automatic fan control loop
<6>	SMB6	R/W	Logic 1 enables SMBus Slave Device 6 to control PWM3 in automatic fan control loop
<7>	SMB7	R/W	Logic 1 enables SMBus Slave Device 7 to control PWM3 in automatic fan control loop

Table 114. REGISTER 0x92 – PWM3 Source Control 3 (Power–On Default = 0x00)

Bit	Name	R/W	Description
<0>	PUSH0	R/W	Logic 1 enables Externally written temperature 0 to control PWM3 in automatic fan control loop
<1>	PUSH1	R/W	Logic 1 enables Externally written temperature 1 to control PWM3 in automatic fan control loop
<2>	PUSH2	R/W	Logic 1 enables Externally written temperature 2 to control PWM3 in automatic fan control loop
<3>	PUSH3	R/W	Logic 1 enables Externally written temperature 3 to control PWM3 in automatic fan control loop
<4>	Reserved		
<5>	Reserved		
<6>	Reserved		
<7>	Reserved		

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Table 115. DEVICE ID REGISTER

Register Address	R/W	Description	Power−On Default
0x93	Read	Device Revision	

Table 116. PECI OFFSET REGISTERS

Register Address	R/W	Description	Power−On Default
0x94	R/W	PECI0 Offset	0x00
0x95	R/W	PECI1 Offset	0x00
0x96	R/W	PECI2 Offset	0x00
0x97	R/W	PECI3 Offset	0x00

Table 117. SMBus MASTER ADDRESS TABLE

Register Address	R/W	Description	Default
0x98	R/W	Device 0 (PCH) SMBus Address	0x00
0x99	R/W	Device 0 (PCH) Block Read command code	0x40
0x9A	R/W	Device 1 SMBus Address	0x00
0x9B	R/W	Device 1 Temperature Address Pointer	0x00
0x9C	R/W	Device 2 SMBus Address	0x00
0x9D	R/W	Device 2 Temperature Address Pointer	0x00
0x9E	R/W	Device 3 SMBus Address	0x00
0x9F	R/W	Device 3 Temperature Address Pointer	0x00
0xA0	R/W	Device 4 SMBus Address	0x00
0xA1	R/W	Device 4 Temperature Address Pointer	0x00
0xA2	R/W	Device 5 SMBus Address	0x00
0xA3	R/W	Device 5 Temperature Address Pointer	0x00
0xA4	R/W	Device 6 SMBus Address	0x00
0xA5	R/W	Device 6 Temperature Address Pointer	0x00
0xA6	R/W	Device 7 SMBus Address	0x00
0xA7	R/W	Device 7 Temperature Address Pointer	0x00

Table 118. SMBus MASTER TEMPERATURE VALUES

Register Address	R/W	Description	Default
0xA8	R/W	SMBus Device 0 (PCH) Temperature	0x80
0xA9	R/W	SMBus Device 1 (DIMM0) Temperature	0x80
0xAA	R/W	SMBus Device 2 (DIMM1) Temperature	0x80
0xAB	R/W	SMBus Device 3 (DIMM2) Temperature	0x80
0xAC	R/W	SMBus Device 4 (DIMM3) Temperature	0x80
0xAD	R/W	SMBus Device 5 Temperature	0x80
0xAE	R/W	SMBus Device 6 Temperature	0x80
0xAF	R/W	SMBus Device 7 Temperature	0x80

Table 119. Register 0xB0 − SMBus Master Configuration 1 (Power−On Default = 0xFF)

Bit	Name	R/W	Description
<0>	RS0	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 0
<1>	RS1	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 1

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Table 119. Register 0xB0 − SMBus Master Configuration 1 (Power−On Default = 0xFF)

Bit	Name	R/W	Description
<2>	RS2	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 2
<3>	RS3	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 3
<4>	RS4	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 4
<5>	RS5	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 5
<6>	RS6	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 6
<7>	RS7	R/W	Logic 1 enables the Repeated Start protocol for SMBus Slave Device 7

Table 120. REGISTER 0xB1 − SMBus Master Configuration 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PEC0	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 0
<1>	PEC1	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 1
<2>	PEC2	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 2
<3>	PEC3	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 3
<4>	PEC4	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 4
<5>	PEC5	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 5
<6>	PEC6	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 6
<7>	PEC7	R/W	Logic 1 enables PEC byte support for SMBus Slave Device 7

Table 121. REGISTER 0xB2 − SMBus Master Configuration 3 (Power−On Default = 0x03)

Bit	Name	R/W	Description
<1:0>	TMFT0	R/W	SMBus Device 0 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Block reads enabled
<3:2>	TMFT1	R/W	SMBus Device 1 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Block reads enabled
<5:4>	TMFT2	R/W	SMBus Device 2 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Block reads enabled
<7:6>	TMFT3	R/W	SMBus Device 3 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Block reads enabled

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Table 122. REGISTER 0xB3 – SMBus Master Configuration 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<1:0>	TMFT4	R/W	SMBus Device 4 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Reserved
<3:2>	TMFT5	R/W	SMBus Device 5 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Literal Format
<5:4>	TMFT6	R/W	SMBus Device 6 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Literal Format
<7:6>	TMFT7	R/W	SMBus Device 7 temperature format: 00 = 8−bit 2's Complement 01 = JEDEC SPD format 10 = 8−bit straight binary 11 = Literal Format

Table 123. REGISTER 0xB5 – SMBus Master Configuration 5 (Power−On Default = 0x08)

Bit	Name	R/W	Description
<0>	SMBEN	R/W	0 = SMBus Master disabled 1 = SMBus Master enabled
<4:1>	SHYS	R/W	SMBus Device temperature hysteresis
<5>	R1DIMM	R/W	1 = Over−write DIMM0/DIMM1 value registers with Remote1 value
<6>	R2DIMM	R/W	1 = Over−write DIMM2/DIMM3 value registers with Remote2 value
<7>	PCHDIMM	R/W	1 = Read DIMM temperatures from PCH. This setting overrides bits 5 and 6 of this register. 0 = Read DIMM temperatures from SMBus digital sensors

Table 124. REGISTER 0xB6 – SMBus Master Status 1 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	NACK0	Read	Logic 1 indicates a No Acknowledge from SMBus Device 0
<1>	NACK1	Read	Logic 1 indicates a No Acknowledge from SMBus Device 1
<2>	NACK2	Read	Logic 1 indicates a No Acknowledge from SMBus Device 2
<3>	NACK3	Read	Logic 1 indicates a No Acknowledge from SMBus Device 3
<4>	NACK4	Read	Logic 1 indicates a No Acknowledge from SMBus Device 4
<5>	NACK5	Read	Logic 1 indicates a No Acknowledge from SMBus Device 5
<6>	NACK6	Read	Logic 1 indicates a No Acknowledge from SMBus Device 6
<7>	NACK7	Read	Logic 1 indicates a No Acknowledge from SMBus Device 7

Table 125. REGISTER 0xB7 – SMBus Master Status 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PEC0	Read	Logic 1 indicates an SMBus Device 0 PEC error
<1>	PEC1	Read	Logic 1 indicates an SMBus Device 1 PEC error
<2>	PEC2	Read	Logic 1 indicates an SMBus Device 2 PEC error
<3>	PEC3	Read	Logic 1 indicates an SMBus Device 3 PEC error

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Table 125. REGISTER 0xB7 – SMBus Master Status 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<4>	PEC4	Read	Logic 1 indicates an SMBus Device 4 PEC error
<5>	PEC5	Read	Logic 1 indicates an SMBus Device 5 PEC error
<6>	PEC6	Read	Logic 1 indicates an SMBus Device 6 PEC error
<7>	PEC7	Read	Logic 1 indicates an SMBus Device 7 PEC error

Table 126. REGISTER 0xB8 – SMBus Master Status 3 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	TO0	Read	Logic 1 indicates an SMBus Device 0 timeout error
<1>	TO1	Read	Logic 1 indicates an SMBus Device 1 timeout error
<2>	TO2	Read	Logic 1 indicates an SMBus Device 2 timeout error
<3>	TO3	Read	Logic 1 indicates an SMBus Device 3 timeout error
<4>	TO4	Read	Logic 1 indicates an SMBus Device 4 timeout error
<5>	TO5	Read	Logic 1 indicates an SMBus Device 5 timeout error
<6>	TO6	Read	Logic 1 indicates an SMBus Device 6 timeout error
<7>	TO7	Read	Logic 1 indicates an SMBus Device 7 timeout error

Table 127. REGISTER 0xB9 – SMBus Master Status 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	HILO0	Read	Logic 1 indicates that the SMBus Device 0 reading is out of limits
<1>	HILO1	Read	Logic 1 indicates that the SMBus Device 1 reading is out of limits
<2>	HILO2	Read	Logic 1 indicates that the SMBus Device 2 reading is out of limits
<3>	HILO3	Read	Logic 1 indicates that the SMBus Device 3 reading is out of limits
<4>	HILO4	Read	Logic 1 indicates that the SMBus Device 4 reading is out of limits
<5>	HILO5	Read	Logic 1 indicates that the SMBus Device 5 reading is out of limits
<6>	HILO6	Read	Logic 1 indicates that the SMBus Device 6 reading is out of limits
<7>	HILO7	Read	Logic 1 indicates that the SMBus Device 7 reading is out of limits

Table 128. REGISTER 0Xba – SMBus Master Status 5 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	TIV0	Read	Logic 1 indicates that the PCH returned a reserved temperature code
<1>	TIV1	Read	Logic 1 indicates that the PCH returned a reserved temperature code
<2>	TIV2	Read	Logic 1 indicates that the PCH returned a reserved temperature code
<3>	TIV3	Read	Logic 1 indicates that the PCH returned a reserved temperature code
<4>	TIV4	Read	Logic 1 indicates that the PCH returned a reserved temperature code
<5>	Reserved	Read	Reserved
<6>	Reserved	Read	Reserved
<7>	Reserved	Read	Reserved

Table 129. REGISTER 0Xbb – SMBus Master Status 6 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	TH0	Read	Logic 1 indicates that the SMBus Device 0 reading is above the programmed THERM Limit
<1>	TH1	Read	Logic 1 indicates that the SMBus Device 1 reading is above the programmed THERM Limit
<2>	TH2	Read	Logic 1 indicates that the SMBus Device 2 reading is above the programmed THERM Limit

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Table 129. REGISTER 0Xbb – SMBus Master Status 6 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<3>	TH3	Read	Logic 1 indicates that the SMBus Device 3 reading is above the programmed THERM Limit
<4>	TH4	Read	Logic 1 indicates that the SMBus Device 4 reading is above the programmed THERM Limit
<5>	TH5	Read	Logic 1 indicates that the SMBus Device 5 reading is above the programmed THERM Limit
<6>	TH6	Read	Logic 1 indicates that the SMBus Device 6 reading is above the programmed THERM Limit
<7>	TH7	Read	Logic 1 indicates that the SMBus Device 7 reading is above the programmed THERM Limit

Table 130. REGISTER 0xBC – SMBus Master Mask 1 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	NACK0	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 0
<1>	NACK1	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 1
<2>	NACK2	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 2
<3>	NACK3	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 3
<4>	NACK4	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 4
<5>	NACK5	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 5
<6>	NACK6	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 6
<7>	NACK7	R/W	Logic 1 masks a No Acknowledge assertion for SMBus Device 7

Table 131. REGISTER 0xBD – SMBus Master Mask 2 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	PEC0	R/W	Logic 1 masks a PEC error assertion for SMBus Device 0
<1>	PEC1	R/W	Logic 1 masks a PEC error assertion for SMBus Device 1
<2>	PEC2	R/W	Logic 1 masks a PEC error assertion for SMBus Device 2
<3>	PEC3	R/W	Logic 1 masks a PEC error assertion for SMBus Device 3
<4>	PEC4	R/W	Logic 1 masks a PEC error assertion for SMBus Device 4
<5>	PEC5	R/W	Logic 1 masks a PEC error assertion for SMBus Device 5
<6>	PEC6	R/W	Logic 1 masks a PEC error assertion for SMBus Device 6
<7>	PEC7	R/W	Logic 1 masks a PEC error assertion for SMBus Device 7

Table 132. REGISTER 0Xbe – SMBus Master Mask 3 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	TO0	R/W	Logic 1 masks a timeout error assertion for SMBus Device 0
<1>	TO1	R/W	Logic 1 masks a timeout error assertion for SMBus Device 1
<2>	TO2	R/W	Logic 1 masks a timeout error assertion for SMBus Device 2
<3>	TO3	R/W	Logic 1 masks a timeout error assertion for SMBus Device 3
<4>	TO4	R/W	Logic 1 masks a timeout error assertion for SMBus Device 4
<5>	TO5	R/W	Logic 1 masks a timeout error assertion for SMBus Device 5
<6>	TO6	R/W	Logic 1 masks a timeout error assertion for SMBus Device 6
<7>	TO7	R/W	Logic 1 masks a timeout error assertion for SMBus Device 7

Table 133. REGISTER 0Xbf – SMBus Master Mask 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	HILO0	R/W	Logic 1 masks limit assertions for SMBus Device 0
<1>	HILO1	R/W	Logic 1 masks limit assertions for SMBus Device 1

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Table 133. REGISTER 0Xbf – SMBus Master Mask 4 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<2>	HILO2	R/W	Logic 1 masks limit assertions for SMBus Device 2
<3>	HILO3	R/W	Logic 1 masks limit assertions for SMBus Device 3
<4>	HILO4	R/W	Logic 1 masks limit assertions for SMBus Device 4
<5>	HILO5	R/W	Logic 1 masks limit assertions for SMBus Device 5
<6>	HILO6	R/W	Logic 1 masks limit assertions for SMBus Device 6
<7>	HILO7	R/W	Logic 1 masks limit assertions for SMBus Device 7

Table 134. REGISTER 0xC0 – SMBus Master Mask 5 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	TIV0	R/W	Logic 1 masks data invalid assertion for SMBus Device 0
<1>	TIV1	R/W	Logic 1 masks data invalid assertion for SMBus Device 1
<2>	TIV2	R/W	Logic 1 masks data invalid assertion for SMBus Device 2
<3>	TIV3	R/W	Logic 1 masks data invalid assertion for SMBus Device 3
<4>	TIV4	R/W	Logic 1 masks data invalid assertion for SMBus Device 4
<5>	TIV5	R/W	Logic 1 masks data invalid assertion for SMBus Device 5
<6>	TIV6	R/W	Logic 1 masks data invalid assertion for SMBus Device 6
<7>	TIV7	R/W	Logic 1 masks data invalid assertion for SMBus Device 7

Table 135. SMBus MASTER LIMIT REGISTERS

Register Address	R/W	Description	Power−On Default
0xC1	R/W	SMBus Device High Limit. Programmed as an unsigned 8−bit value	0x7F
0xC2	R/W	SMBus Device Low Limit. Programmed as an 8−bit 2's complement value.	0x81

Table 136. SMBus MASTER THERM LIMIT REGISTERS

Register Address	R/W	Description	Power−On Default
0xC3	R/W	SMBus Device THERM Limit. Programmed as an unsigned 8−bit value	0x64

Table 137. SMBus DEVICE TMIN REGISTER

Register Address	R/W	Description	Power−On Default
0xC6	R/W	SMBus Device Tmin value. This sets the the temperature at which fans controlled by any SMBus slave device will turn on. Programmed as an unsigned 8−bit value in the range 0°C to 175°C.	0x5A

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Table 138. REGISTER 0xC7 – SMBus Master Trange/Interval (Power−On Default = 0x0C)

Bit	Name	R/W	Description
<3:0>	RNG	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C
<5:4>	Reserved		
<7:6>	SMBINT	R/W	Sets the SMBus Master loop time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1 sec

Table 139. PUSH TEMPERATURE REGISTERS

Register Address	R/W	Description	Power−On Default
0xC8	R/W	Push0. This register is programmable by an external master to allow temperatures gathered externally to be used by the NCT7491 fan control loop	0x00
0xC9	R/W	Push1. This register is programmable by an external master to allow temperatures gathered externally to be used by the NCT7491 fan control loop	0x00
0xCA	R/W	Push2. This register is programmable by an external master to allow temperatures gathered externally to be used by the NCT7491 fan control loop	0x00
0xCB		Push3. This register is programmable by an external master to allow temperatures gathered externally to be used by the NCT7491 fan control loop	0x00

Table 140. PUSH TMIN REGISTER

Register Address	R/W	Description	Power−On Default
0xCC	R/W	Push Device Tmin value. This sets the the temperature at which fans controlled by any SMBus slave device will turn on. This value applies to all 4 Push temperature registers. This value should be programmed in the range 0°C to 127°C	0x5A

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Table 141. REGISTER 0xCD − Push Trange (Power−On Default = 0x0C)

Bit	Name	R/W	Description
<3:0>	RNG	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C
<7:4>	Reserved		

Table 142. PUSH TEMPERATURE LIMIT REGISTERS

Register Address	R/W	Description	Power−On Default
0xCE	R/W	Push High Limit	0x7F
0xCF	R/W	Push Low Limit	0x81
0xD0	R/W	Push THERM Limit	0x64

Table 143. GENERIC PECI INTERFACE BLOCK

Register Address	R/W	Description	Default
0xD1	R/W	Generic PECI CPU Address. This sets the target processor address for the PECI command	0x00
0xD2	R/W	Write Length. This sets the number of byte transferred to the target device when the command is executed	0x00
0xD3	R/W	Read Length. This specifies the number of bytes to be returned by the target.	0x00
0xD4	R/W	WRDAT0; The 1st byte to be transferred (Command Code)	0x00
0xD5	R/W	WRDAT1; 2nd byte to be transferred	0x00
0xD6	R/W	WRDAT2; 3rd byte to be transferred	0x00
0xD7	R/W	WRDAT3; 4th byte to be transferred	0x00
0xD8	R/W	WRDAT4; 5th byte to be transferred	0x00
0xD9	R/W	WRDAT5; 6th byte to be transferred	0x00
0xDA	R/W	WRDAT6; 7th byte to be transferred	0x00
0xDB	R/W	WRDAT7; 8th byte to be transferred	0x00
0xDC	R/W	WRDAT8; 9th byte to be transferred	0x00
0xDD	R/W	WRDAT9; 10th byte to be transferred	0x00
0xDE	R/W	WRDAT10; 11th byte to be transferred	0x00
0xDF	R/W	WRDAT11; 12th byte to be transferred	0x00
0xE0	R/W	WRDAT12; 13th byte to be transferred	0x00
0xE1	R/W	RDDAT0; The 1st byte returned	0x00
0xE2	R/W	RDDAT1; The 2nd byte returned	0x00
0xE3	R/W	RDDAT2; The 3rd byte returned	0x00
0xE4	R/W	RDDAT3; The 4th byte returned	0x00
0xE5	R/W	RDDAT4; The 5th byte returned	0x00

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Table 143. GENERIC PECI INTERFACE BLOCK

Register Address	R/W	Description	Default
0xE6	R/W	RDDAT5; The 6th byte returned	0x00
0xE7	R/W	RDDAT6; The 7th byte returned	0x00
0xE8	R/W	RDDAT6; The 8th byte returned	0x00
0xE9	R/W	RDDAT6; The 9th byte returned	0x00

Table 144. REGISTER 0xEA − PECI Configuration 5 (Power−On Default = 0x00)

Bit	Name	R/W	Description
<0>	Reserved		
<1>	AW	R/W	Logic 1 indicates that the command is an Assured Write command. The AW byte is automatically calculated and appended by the NCT7491. Even though the user does not program the AW value the Write Length register for an Assured Write command should include the AW byte (for example, if 5 bytes are to be written the Write length register should be set to 6 as the AW byte will be added to the end of the write sequence)
<2>	PEX	R/W	Logic 1 will cause the programmed PECI command sequence to be executed. This bit will automatically clear when the command has completed.
<7:3>	Reserved		

Table 145. REGISTER 0xEB − Push Hysteresis (Power−On Default = 0x04)

Bit	Name	R/W	Description
<3:0>	Push Hyst	R/W	Sets the hysteresis value associated with the Push temperature registers
<7:4>	Reserved		

Table 146. REGISTER 0xFF − Page Select

Bit	Name	R/W	Description
<0>	RGMP	R/W	1 = Selects register map page 1
<7:1>	Reserved	R	

Table 147. FAN1 LOOK UP TABLE

Register Address	R/W	Description	Default
0x100	R/W	Sets the temperature for the 1st LUT point for Fan1	0x00
0x101	R/W	Sets the PWM output for the 1st LUT point for Fan1	0xFF
0x102	R/W	Sets the temperature for the 2nd LUT point for Fan1	0x00
0x103	R/W	Sets the PWM output for the 2nd LUT point for Fan1	0xFF
0x104	R/W	Sets the temperature for the 3rd LUT point for Fan1	0x00
0x105	R/W	Sets the PWM output for the 3rd LUT point for Fan1	0xFF
0x106	R/W	Sets the temperature for the 4th LUT point for Fan1	0x00
0x107	R/W	Sets the PWM output for the 4th LUT point for Fan1	0xFF
0x108	R/W	Sets the temperature for the 5th LUT point for Fan1	0x00
0x109	R/W	Sets the PWM output for the 5th LUT point for Fan1	0xFF
0x10A	R/W	Sets the temperature for the 6th LUT point for Fan1	0x00
0x10B	R/W	Sets the PWM output for the 6th LUT point for Fan1	0xFF
0x10C	R/W	Sets the temperature for the 7th LUT point for Fan1	0x00
0x10D	R/W	Sets the PWM output for the 7th LUT point for Fan1	0xFF
0x10E	R/W	Sets the temperature for the 8th LUT point for Fan1	0x00
0x10F	R/W	Sets the PWM output for the 8th LUT point for Fan1	0xFF

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Table 148. FAN2 LOOK UP TABLE

Register Address	R/W	Description	Default
0x110	R/W	Sets the temperature for the 1st LUT point for Fan2	0xFF
0x111	R/W	Sets the PWM output for the 1st LUT point for Fan2	0xFF
0x112	R/W	Sets the temperature for the 2nd LUT point for Fan2	0xFF
0x113	R/W	Sets the PWM output for the 2nd LUT point for Fan2	0xFF
0x114	R/W	Sets the temperature for the 3rd LUT point for Fan2	0xFF
0x115	R/W	Sets the PWM output for the 3rd LUT point for Fan2	0xFF
0x116	R/W	Sets the temperature for the 4th LUT point for Fan2	0xFF
0x117	R/W	Sets the PWM output for the 4th LUT point for Fan2	0xFF
0x118	R/W	Sets the temperature for the 5th LUT point for Fan2	0xFF
0x119	R/W	Sets the PWM output for the 5th LUT point for Fan2	0xFF
0x11A	R/W	Sets the temperature for the 6th LUT point for Fan2	0xFF
0x11B	R/W	Sets the PWM output for the 6th LUT point for Fan2	0xFF
0x11C	R/W	Sets the temperature for the 7th LUT point for Fan2	0xFF
0x11D	R/W	Sets the PWM output for the 7th LUT point for Fan2	0xFF
0x11E	R/W	Sets the temperature for the 8th LUT point for Fan2	0xFF
0x11F	R/W	Sets the PWM output for the 8th LUT point for Fan2	0xFF

Table 149. FAN3 LOOK UP TABLE

Register Address	R/W	Description	Default
0x120	R/W	Sets the temperature for the 1st LUT point for Fan3	0xFF
0x121	R/W	Sets the PWM output for the 1st LUT point for Fan3	0xFF
0x122	R/W	Sets the temperature for the 2nd LUT point for Fan3	0xFF
0x123	R/W	Sets the PWM output for the 2nd LUT point for Fan3	0xFF
0x124	R/W	Sets the temperature for the 3rd LUT point for Fan3	0xFF
0x125	R/W	Sets the PWM output for the 3rd LUT point for Fan3	0xFF
0x126	R/W	Sets the temperature for the 4th LUT point for Fan3	0xFF
0x127	R/W	Sets the PWM output for the 4th LUT point for Fan3	0xFF
0x128	R/W	Sets the temperature for the 5th LUT point for Fan3	0xFF
0x129	R/W	Sets the PWM output for the 5th LUT point for Fan3	0xFF
0x12A	R/W	Sets the temperature for the 6th LUT point for Fan3	0xFF
0x12B	R/W	Sets the PWM output for the 6th LUT point for Fan3	0xFF
0x12C	R/W	Sets the temperature for the 7th LUT point for Fan3	0xFF
0x12D	R/W	Sets the PWM output for the 7th LUT point for Fan3	0xFF
0x12E	R/W	Sets the temperature for the 8th LUT point for Fan3	0xFF
0x12F	R/W	Sets the PWM output for the 8th LUT point for Fan3	0xFF

Table 150. REGISTER 0x1FF – Page Select Clear

Bit	Name	R/W	Description
<0>	RGMP	R/W	0 = Selects register map page 0
<7:1>	Reserved	R	

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ORDERING INFORMATION

Model	Termperature Range	Package Type	Shipping†
NCT7491RQR2G	−40°C to +125°C	QSOP24 (Pb−Free)	2500 / Tape & Reel
NCT7491MNTXG	−40°C to +125°C	QFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
5	Corrected the shipping quanitities for the two OPNs in order information table.	7/2/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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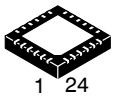
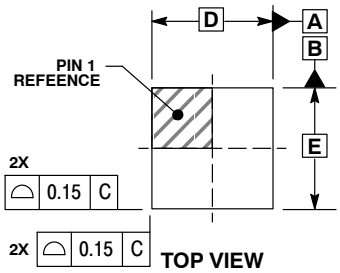
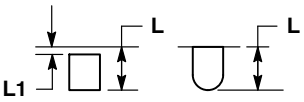
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

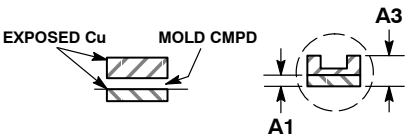


SCALE 2:1

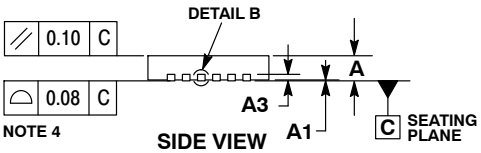


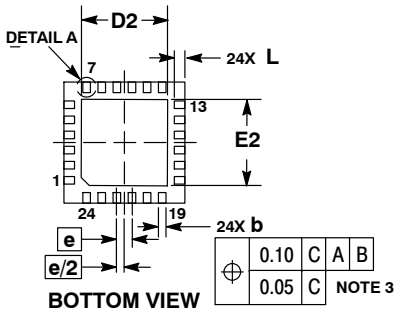


DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE TERMINAL CONSTRUCTIONS

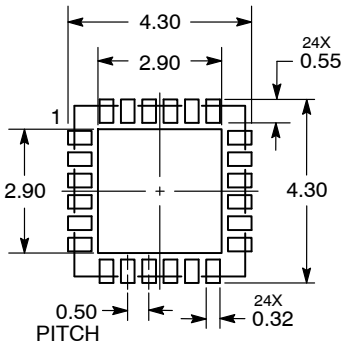




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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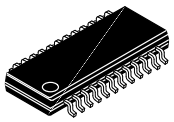
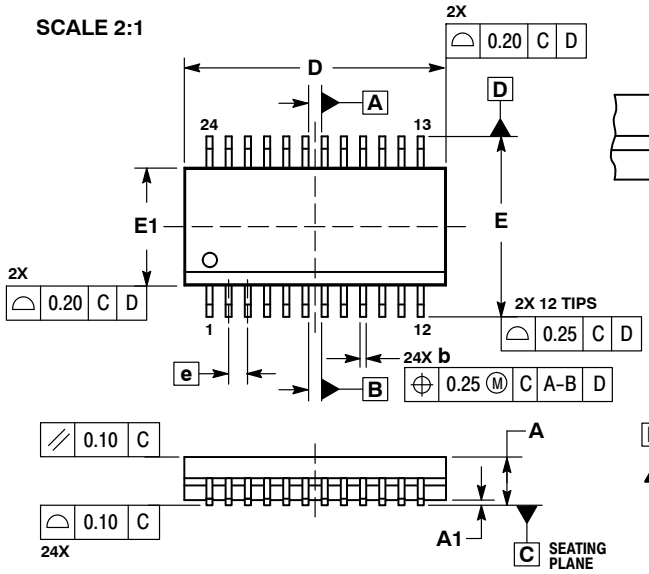
QSOP24 NB
CASE 492B−01
ISSUE A

DATE 06 MAY 2008



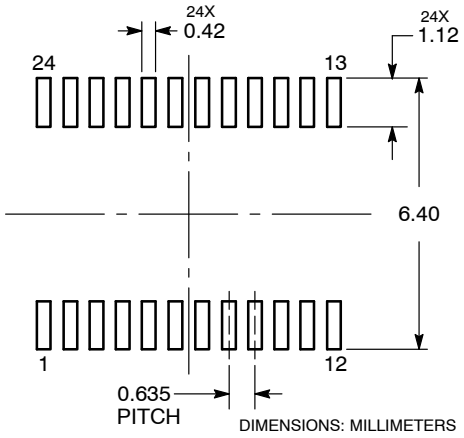
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.20	0.30
C	0.19	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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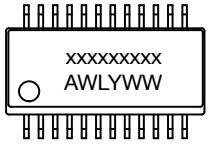
GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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