Charge Pump Buck/Boost Converter, LDO Regulator, Very Low Quiescent Current, 600 mA/300 mA

NCV48920

The NCV48920 is 600 mA buck and 300 mA boost charge pump regulator with integrated Very Low Quiescent Current LDO regulator for automotive applications. The NCV48920 requires very low number of external components. The Enable function can be used to disable the chip and hence to reduce quiescent current down to 1 μA. The NCV48920 contains protection functions such as current limit, thermal shutdown and reverse bias current protection.

Features

- Output Voltage: 5 V
- Output Current: 600 mA Buck and 300 mA Boost Mode
- Buck Mode Input Voltage Operation: down to 11.8 V
- Boost Mode Input Voltage Operation: from 3 V
- Enable Function (1 μA max quiescent current when disabled)
- Microprocessor Compatible Control Functions:
  - ♦ Reset Output
  - ♦ Enable Input
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Grade 1 Qualified and PPAP Capable
- Protection Features:
  - ♦ Current Limitation
  - ♦ Thermal Shutdown
  - ♦ Reverse Bias Output Current
- This is a Pb−Free Device

Typical Applications (for safety applications refer to Figure 37)

- Stop−Start Applications
- Body Electronics
- Instruments and Clusters
- Infotainment
- LED Supply

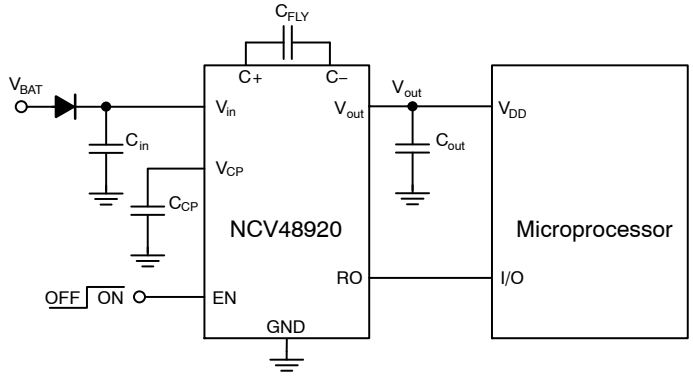

Figure 1. Application Schematic

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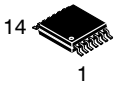
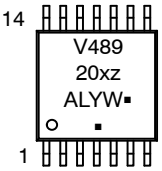
MARKING DIAGRAMS



TSSOP−14 EPAD
CASE 948AW



x	= Output Voltage Option: 5 – 5 V
z	= Reset Delay Time Options: 0 – 0 ms, 1 – 2 ms, 2 – 4 ms, 3 – 8 ms, 4 – 16 ms, 5 – 32 ms, 6 – 64 ms, 7 – 128 ms
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

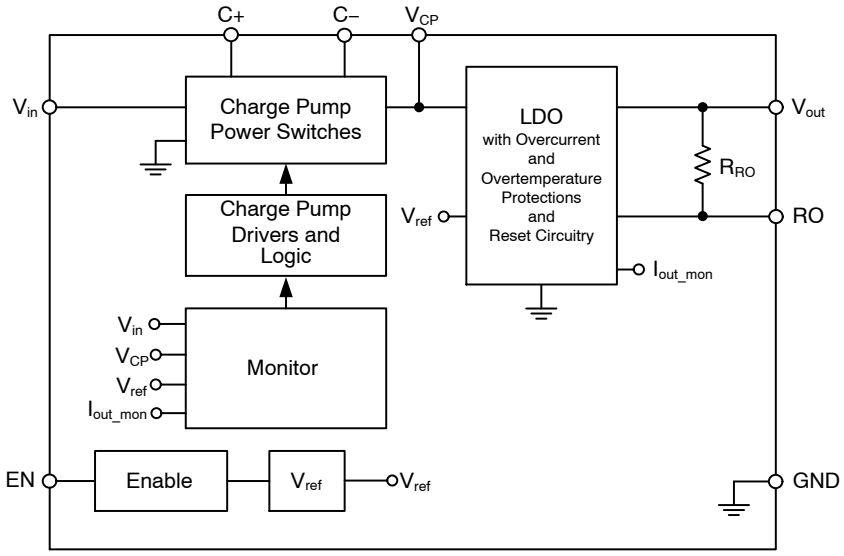


Figure 2. Simplified Block Diagram

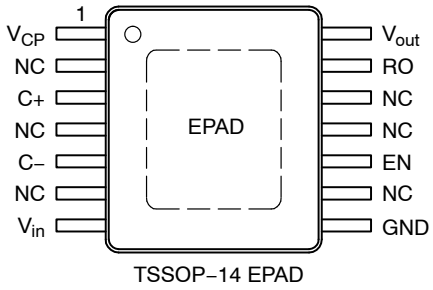


Figure 3. Pin Connections (Top View)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{CP}	Charge Pump Output Voltage (Input Voltage of LDO).
2	NC	Not Connected.
3	C+	Flying Capacitor Positive Connection.
4	NC	Not Connected.
5	C–	Flying Capacitor Negative Connection.
6	NC	Not Connected
7	V_{in}	Charge Pump Input Voltage.
8	GND	Power Supply Ground.
9	NC	Not Connected.
10	EN	Enable Input; low level disables the IC.
11	NC	Not Connected.
12	NC	Not Connected.
13	RO	Reset Output. 30 kΩ internal Pull–up resistor connected between RO and V_{out}. RO goes Low when V_{out} is out of regulation. See ELECTRICAL CHARCTERISTICS table for delay time specifications.
14	V_{out}	Regulated Output Voltage of LDO.
EPAD	EPAD	Connect to ground potential or leave unconnected.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Charge Pump Input Voltage DC (Note 1)	V_{in}	−0.3	40	V
Charge Pump Input Voltage, Enable Input Voltage (Note 2) Load Dump − Suppressed	U_{s*}	−	45	V
Charge Pump Output Voltage	V_{CP}	−0.3	25	V
Positive Flying Capacitor Voltage	V_{C+}	−0.3	25	V
Negative Flying Capacitor Voltage	V_{C-}	−0.3	40	V
Regulated Output Voltage	V_{out}	−0.3	16	V
Enable Input Voltage	V_{EN}	−0.3	40	V
Reset Output Voltage	V_{RO}	−0.3	16	V
Maximum Junction Temperature	$T_{J(max)}$	−	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device	ESD_{CDM}	−1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Value	Unit
Moisture Sensitivity Level	MSL	1	−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSSOP−14 EPAD			°C/W
Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	59	
Thermal Reference, Junction−to−Lead (pin 3−5 or 10−12) (Note 5)	$R_{\psi JL}$	21.0	
Thermal Resistance, Junction−to−Air (Note 6)	$R_{\theta JA}$	35	
Thermal Reference, Junction−to−Lead (pin 3−5 or 10−12) (Note 6)	$R_{\psi JL}$	16.0	

5. Values based on 1s0p board with copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3.
6. Values based on 1s2p board with copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. 4 layers − according to JEDEC51.7.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Charge Pump Input Voltage for Buck Mode	V_{in}	11.8	40	V
Charge Pump Input Voltage for Boost Mode	V_{in}	3	6.3	V
Charge Pump Output Voltage (Input Voltage of LDO)	V_{CP}	3.5	15	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3 V, I_{CP} = 0 mA, C_{FLY} = 10 μF, C_{CP} = 10 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CHARGER PUMP OUTPUT						
Undervoltage Lockout	V_{in} rising V_{in} falling	V_{in_UVLO}	2.6 2.2	2.8 2.4	3.0 2.6	V
Charge Pump Operating Range Buck Mode	V_{CP} decreasing (buck mode OFF threshold) V_{in} increasing (buck mode ON threshold)	V_{buck}	5.1 11.8	5.3 12.2	5.5 12.6	V
Charge Pump Operating Current Threshold for Buck Mode	I_{out} decreasing, I_{CP} = 0 mA (no load connected to V_{CP} pin)	$I_{out\_cp\_OFF}$	5	15	25	mA
Charge Pump Operating Range Boost Mode	V_{CP} decreasing (boost mode ON threshold) V_{in} increasing (boost mode OFF threshold)	V_{boost}	5.1 5.9	5.3 6.1	5.5 6.3	V
Charge Pump Voltage Drop (V_{in} − V_{CP})	V_{in} = 7 V, I_{out} = 300 mA	V_{DO_CP}	–	250	700	mV
Charge Pump Output Voltage Limit	V_{in} = 32 V to 40 V I_{out} = 0.1 mA V to 600 mA	V_{CP_LIM}	13	14	15	V
Charge Pump Output Current Limit	V_{CP} = 0 V (shorted to GND)	I_{CP_LIM}	800	–	1800	mA
Charge Pump Output Impedance	V_{in} = 3 V, I_{out} = 150 mA	R_{out_CP}	–	3.2	–	Ω
Switching Frequency	V_{in} = 3 V	f_{SW}	400	450	500	kHz
REGULATOR OUTPUT						
Output Voltage (Accuracy%)	T_J = −40°C to 150°C V_{in} = 13.5 V, I_{out} = 0.1 mA to 600 mA	V_{out}	4.9 (−2%)	5.0	5.1 (+2%)	V
Output Voltage (Accuracy%)	T_J = 25°C V_{in} = 12.2 V, I_{out} = 500 mA	V_{out}	4.8 (−4%)	5.0	5.1 (+2%)	V
Output Voltage (Accuracy%)	T_J = −40°C to 150°C V_{in} = 8 V, I_{out} = 0.1 mA to 600 mA	V_{out}	4.9 (−2%)	5.0	5.1 (+2%)	V
Output Voltage (Accuracy%)	T_J = 25°C V_{in} = 3 V, I_{out} = 300 mA	V_{out}	4.8 (−4%)	5.0	5.1 (+2%)	V
Output Voltage (Accuracy%)	T_J = −40°C to 150°C V_{in} = 3 V, I_{out} = 150 mA	V_{out}	4.8 (−4%)	5.0	5.1 (+2%)	V
Dropout Voltage (Note 8)	I_{out} = 300 mA	V_{DO}	–	150	300	mV
QUIESCENT CURRENT AND DISABLE CURRENT						
Disable Current	V_{EN} = 0 V, T_J < 85°C	I_{DIS}	–	–	1.5	μA
Quiescent Current	I_{out} = 0.1 mA, T_J = 25°C I_{out} = 0.1 mA, T_J < 85°C	I_q	– –	45 –	50 55	μA
CURRENT LIMIT PROTECTION						
Current Limit	V_{in} = 0 V, V_{CP} = 10 V, V_{out} = 0.96 x V_{out_nom}	I_{LIM}	650	–	1600	mA
Short Circuit Current Limit	V_{in} = 0 V, V_{CP} = 10 V, V_{out} = 0 V	I_{SC}	–	1000	–	mA
ENABLE						
Enable Input Threshold Voltage Logic Low Logic High		$V_{th(EN)}$	– 2.5	– –	0.8 –	V
Enable Input Current Logic High Logic Low	V_{EN} = 5 V V_{EN} = 0 V, T_J < 85°C	I_{EN_ON} I_{EN_OFF}	– –	3 0.5	5 1	μA
RESET OUTPUT						
Reset Output Thresholds High Low	V_{out} decreasing V_{out} increasing	$V_{th(RO)}$	90 90.5	92.5 –	95 97	% of V_{out}
Reset Output Low Voltage	I_{RO} < 200 μA, V_{out} > 1 V	V_{ROL}	–	0.15	0.25	V
Integrated Reset Output Pull Up Resistor		R_{RO}	15	30	50	kΩ
Reset Delay Time (Note 9)	Min Available Time Max Available Time	t_{RD}	– 102.4	0 128	– 153.6	ms

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3 V, I_{CP} = 0 mA, C_{FLY} = 10 μF, C_{CP} = 10 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET OUTPUT						
Reset Reaction Time		t_{RR}	16	25	38	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 10)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 10)		T_{SH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible
8. Measured when output voltage falls 100 mV below the regulated voltage at V_{CP} = 13.5 V.
9. Reset Delay Times can be chosen from list: 0, 2, 4, 8, 16, 32, 64, 128 ms (Reset Delay Time 0 ms represents Power Good function) and these delay times are factory preset.
10. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

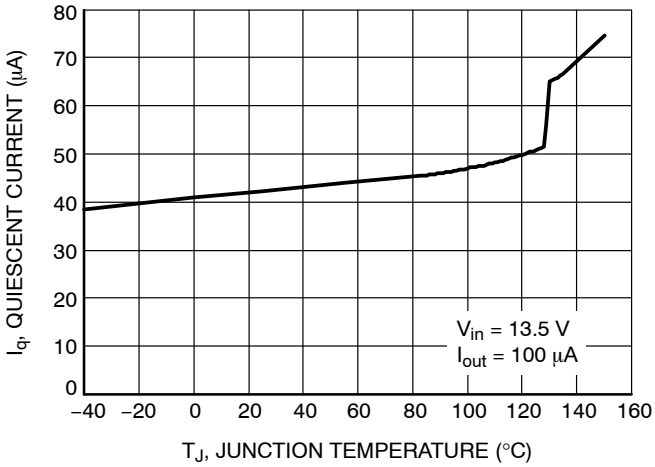


Figure 4. Quiescent Current vs. Junction Temperature

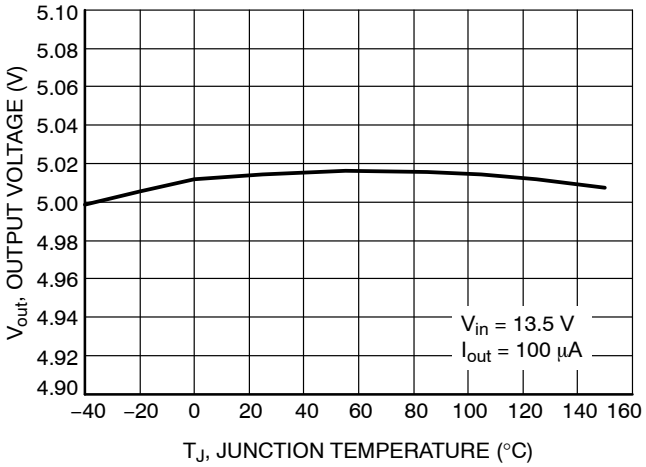


Figure 5. Output Voltage vs. Junction Temperature

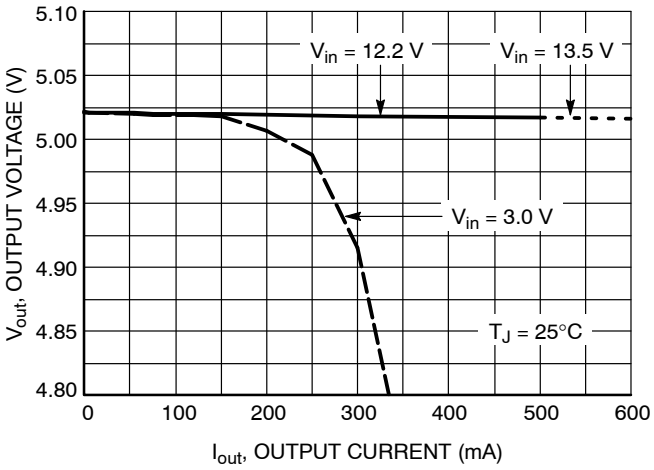


Figure 6. Output Voltage vs. Output Current

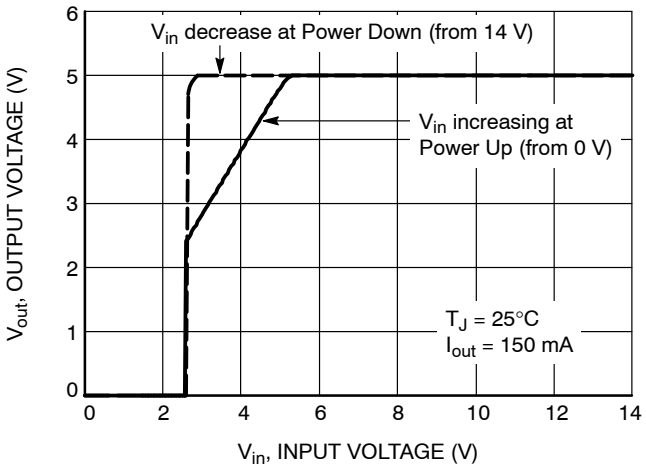


Figure 7. Output Voltage vs. Input Voltage

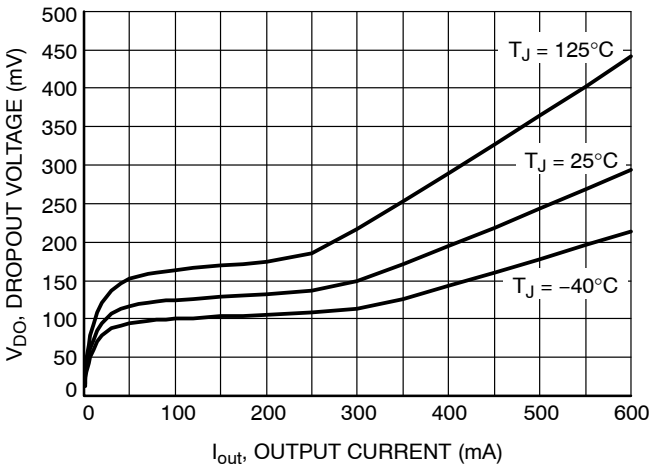


Figure 8. Dropout Voltage vs. Output Current

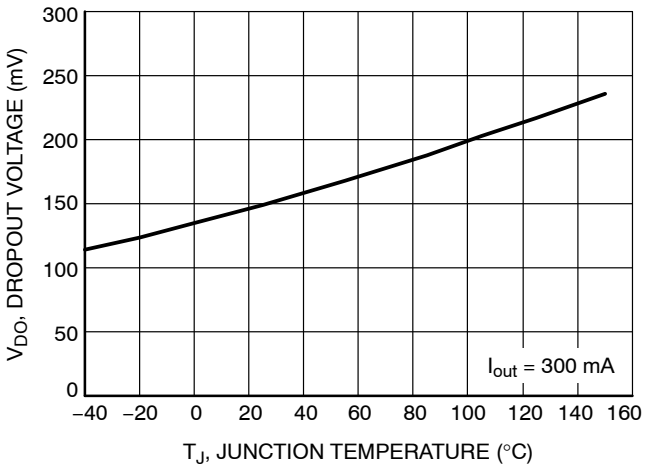


Figure 9. Dropout Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

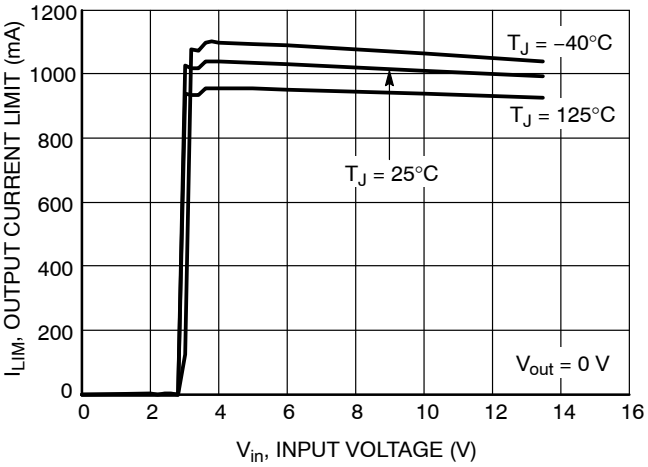


Figure 10. Output Current Limit vs. Input Voltage

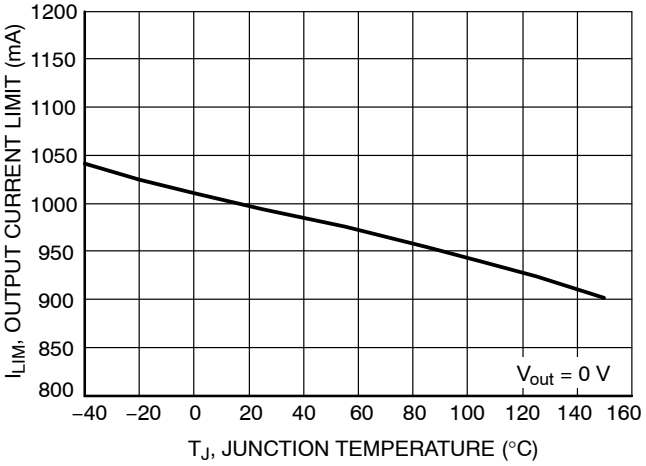


Figure 11. Output Current Limit vs. Junction Temperature

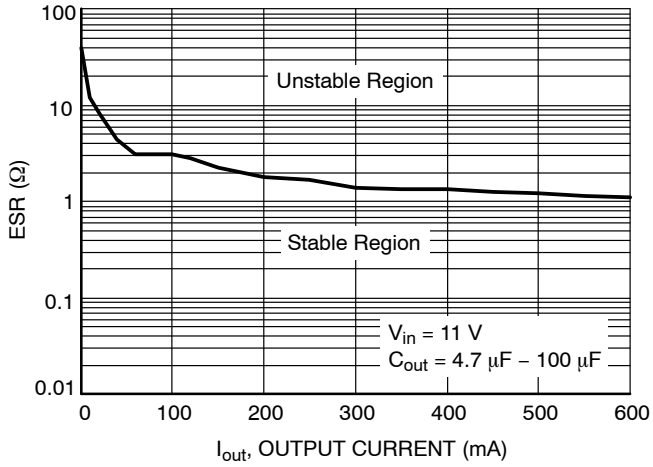


Figure 12. Output Stability with Output Capacitor ESR

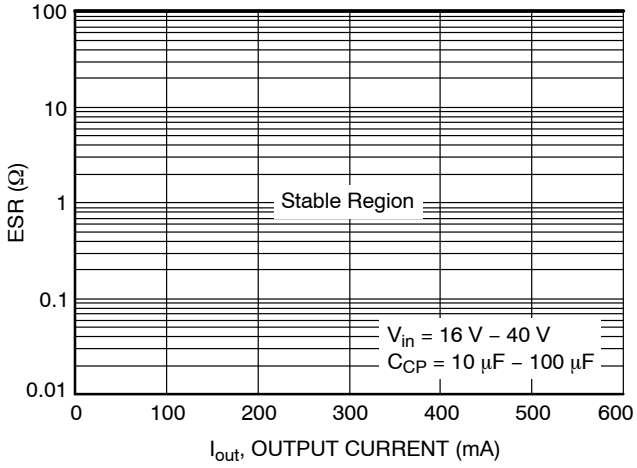


Figure 13. Charge Pump Output Stability with Charge Pump Output Capacitor ESR

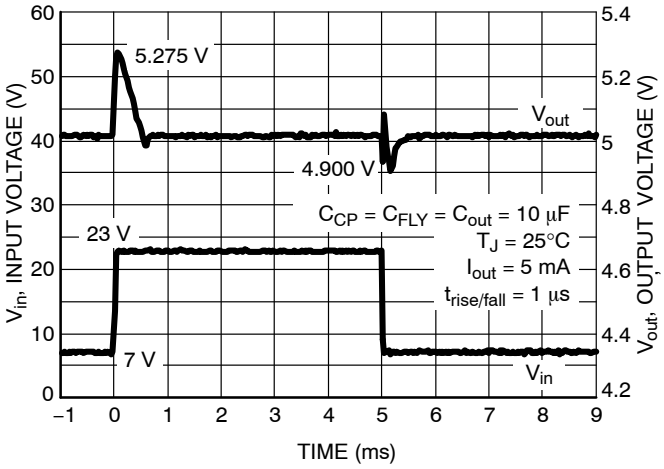


Figure 14. Line Transient

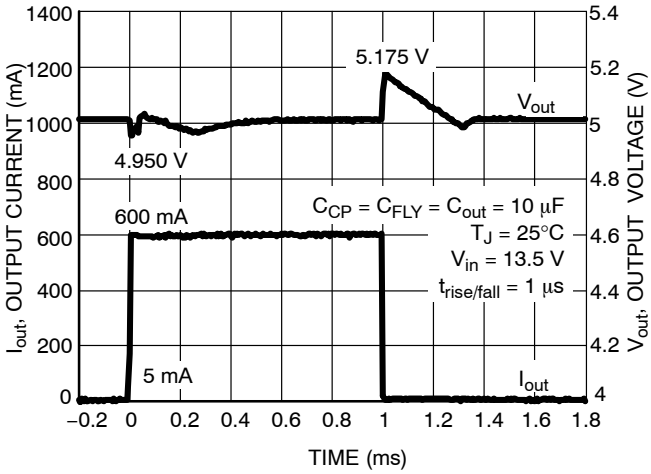


Figure 15. Load Transient

TYPICAL CHARACTERISTICS

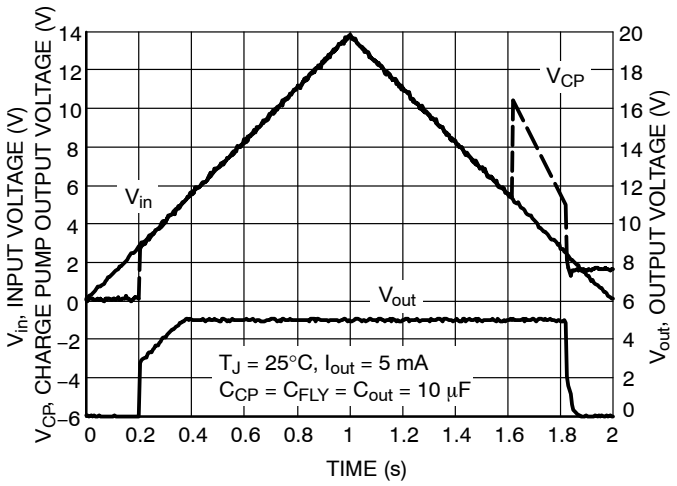


Figure 16. Start Up and Shut Down with Input Voltage

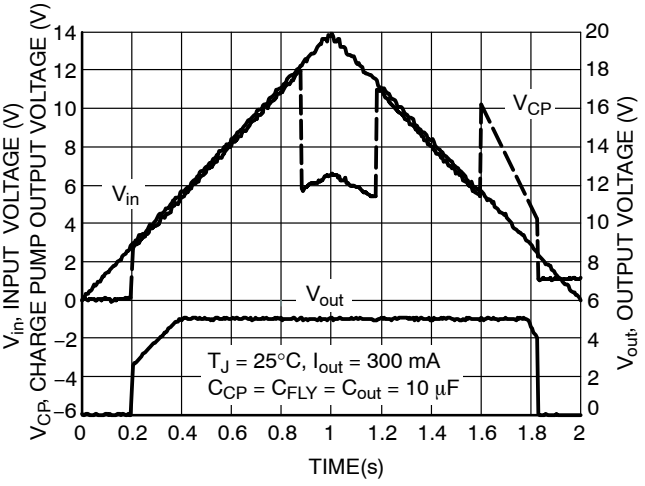


Figure 17. Start Up and Shut Down with Input Voltage

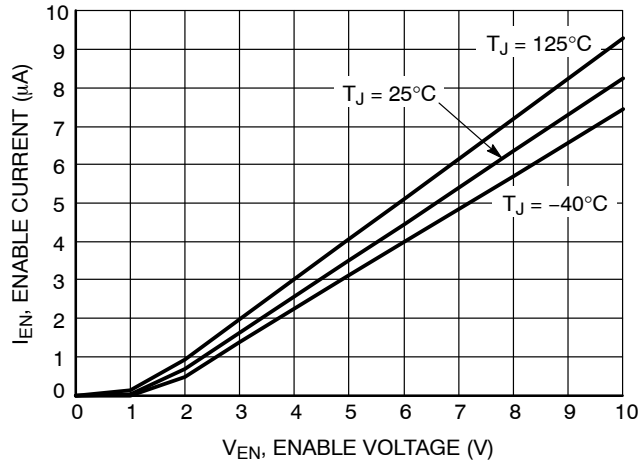


Figure 18. Enable Current vs. Enable Voltage (low range)

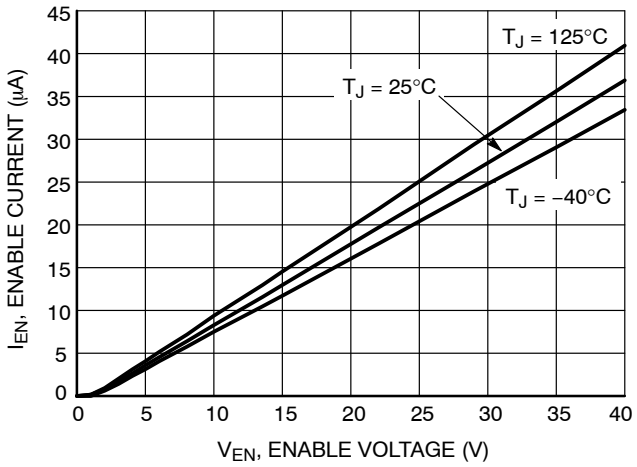


Figure 19. Enable Current vs. Enable Voltage (high range)

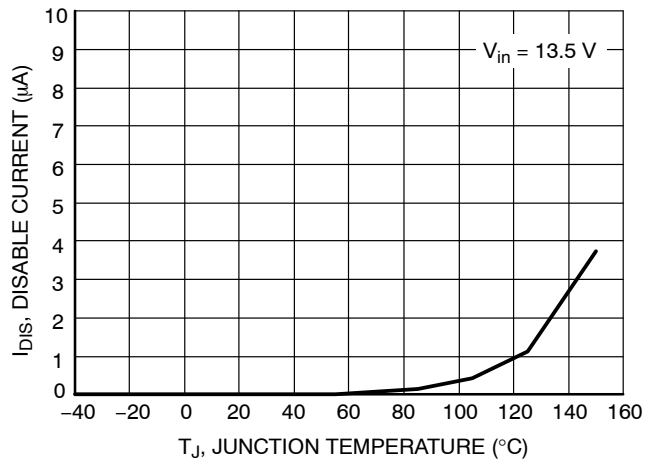


Figure 20. Disable Current vs. Junction Temperature

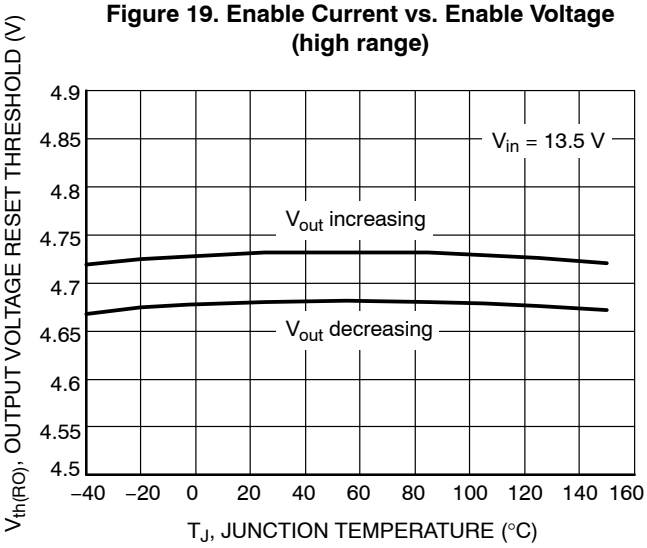


Figure 21. Output Voltage Reset Threshold vs. Junction Temperature

TYPICAL CHARACTERISTICS

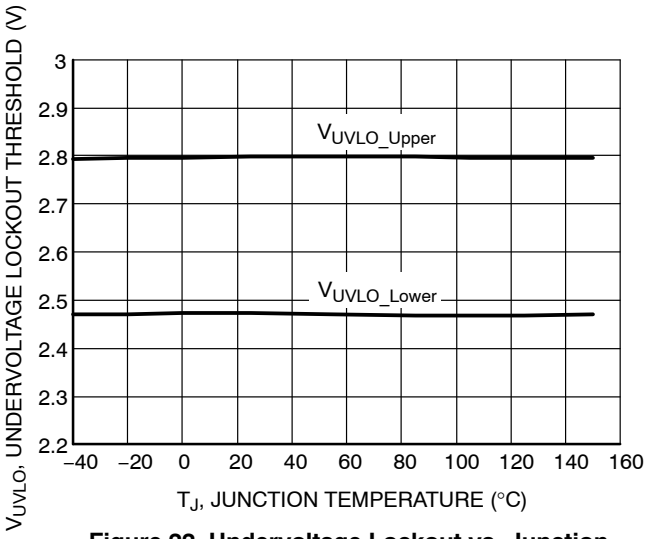


Figure 22. Undervoltage Lockout vs. Junction Temperature

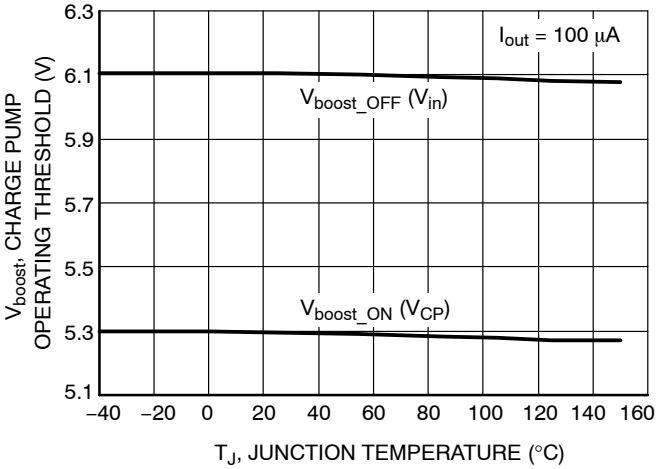


Figure 23. Charge Pump Operating Threshold vs. Junction Temperature (Boost Mode)

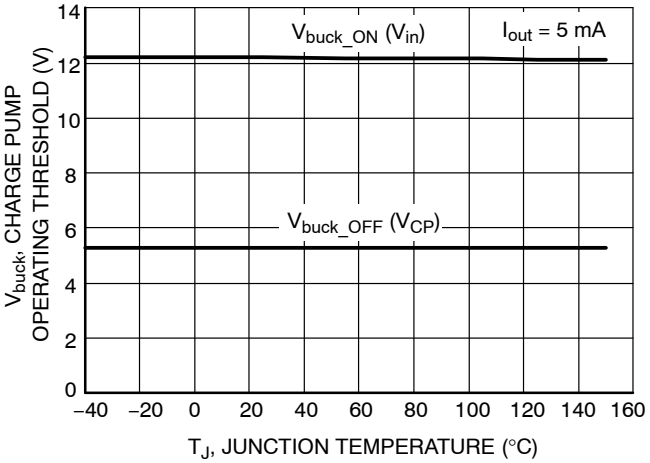


Figure 24. Charge Pump Operating Threshold vs. Junction Temperature (Buck Mode)

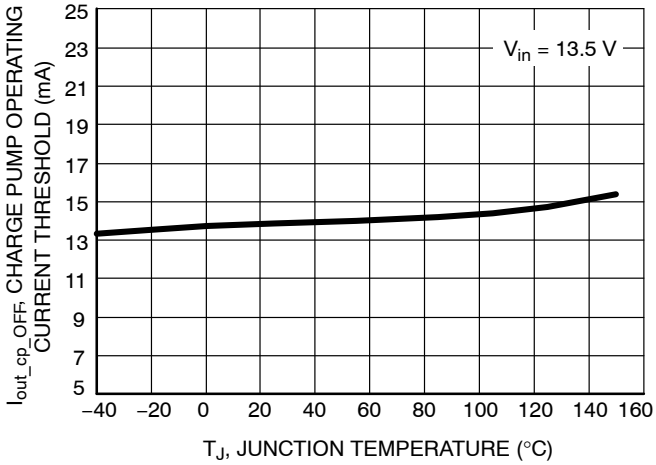


Figure 25. Charge Pump Operating Threshold vs. Junction Temperature (Buck Mode)

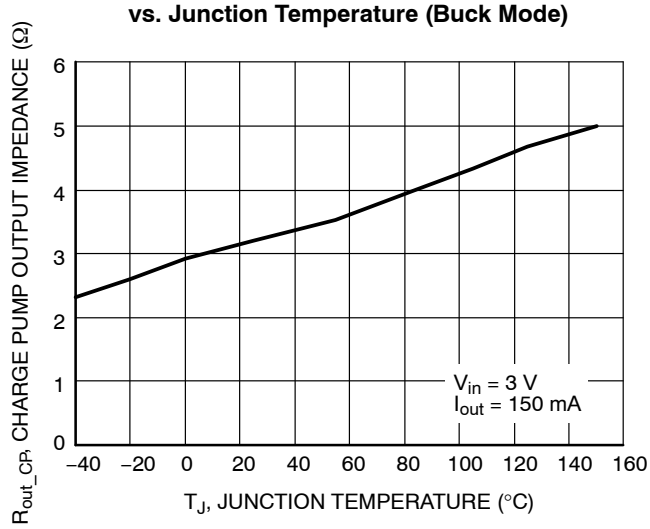


Figure 26. Charge Pump Output Impedance vs. Junction Temperature (Boost Mode)

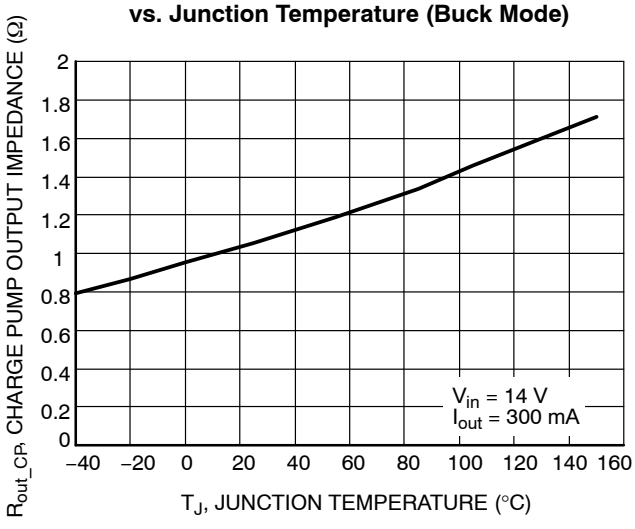


Figure 27. Charge Pump Output Impedance vs. Junction Temperature (Buck Mode)

TYPICAL CHARACTERISTICS

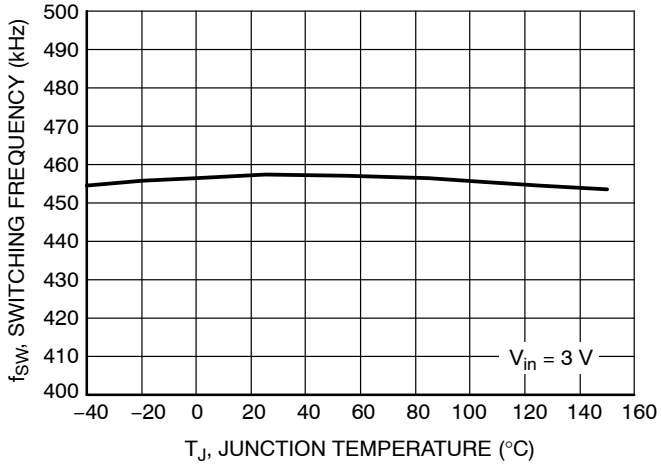


Figure 28. Switching Frequency vs. Junction Temperature

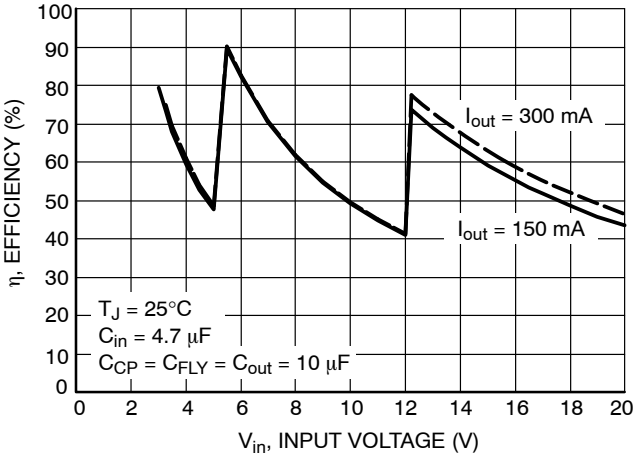


Figure 29. Efficiency vs. Input Voltage

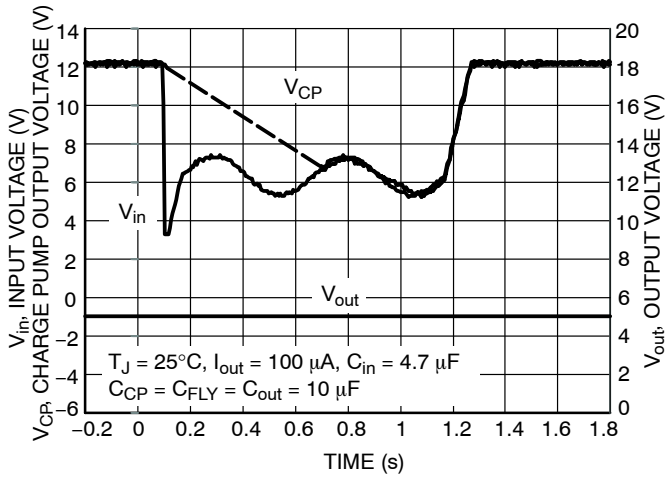


Figure 30. Starting Profile Transient

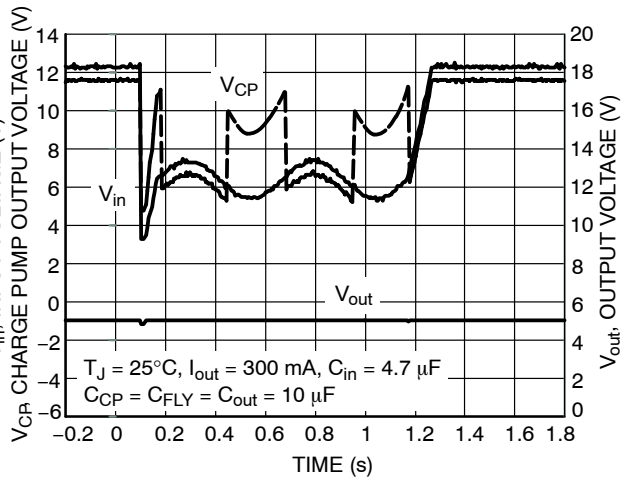


Figure 31. Starting Profile Transient

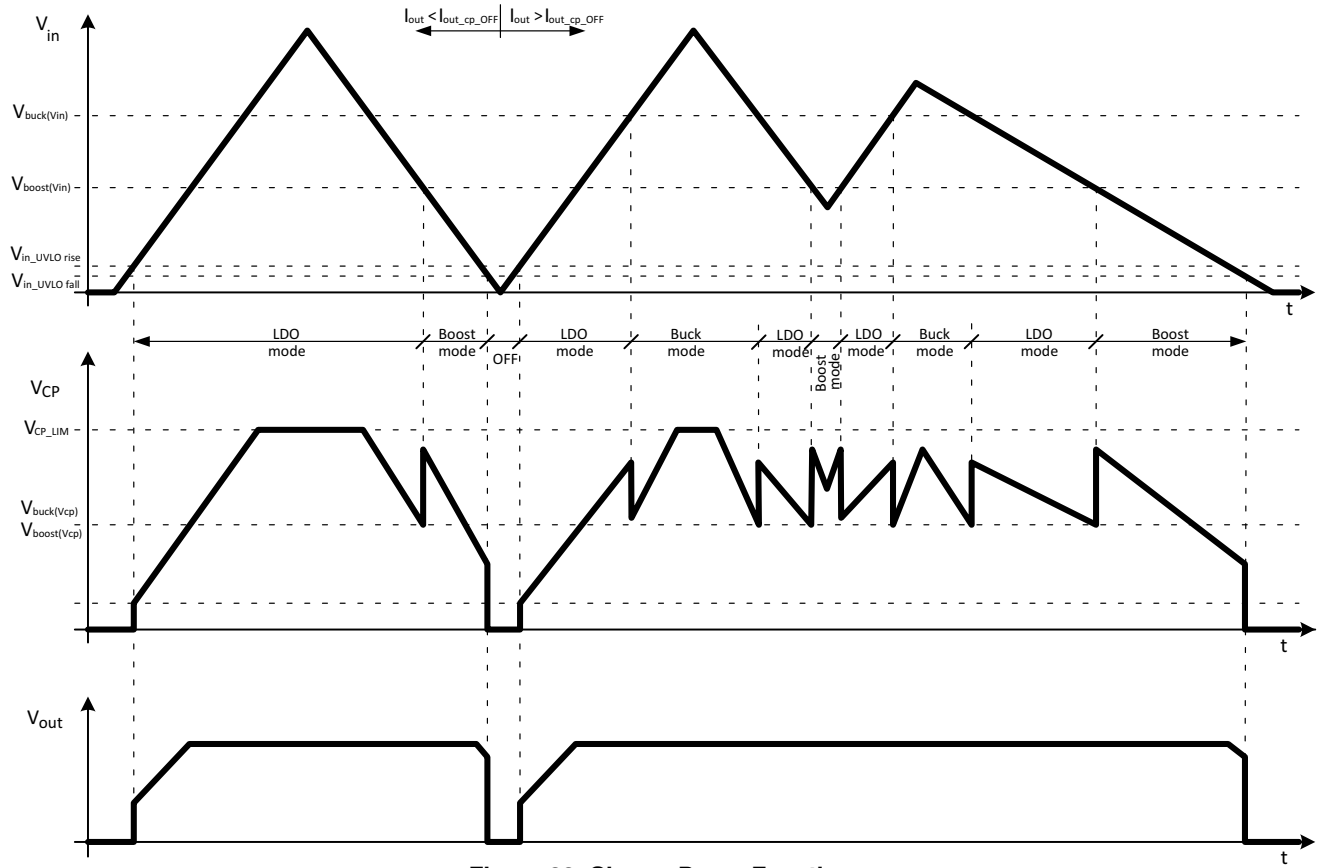


Figure 32. Charge Pump Function

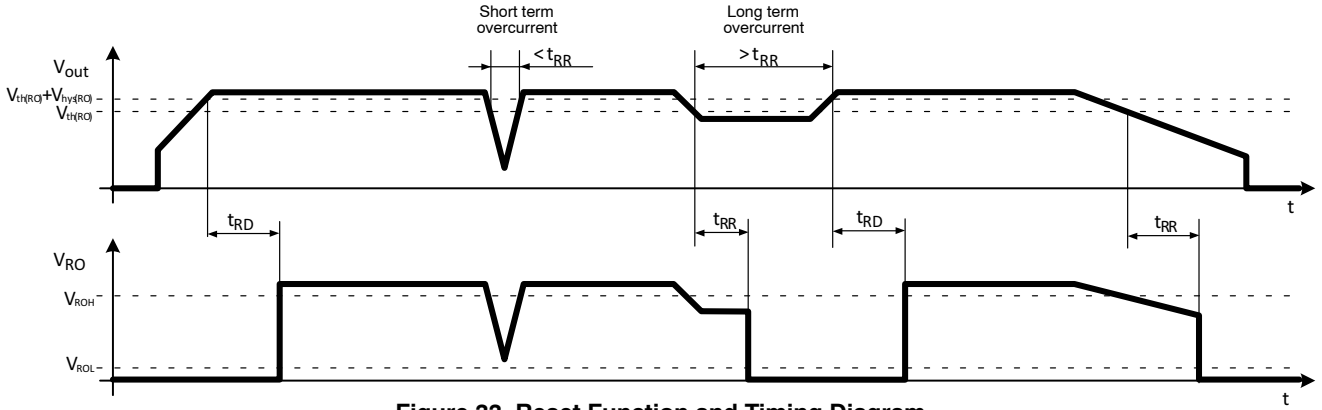


Figure 33. Reset Function and Timing Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Charge Pump Output Voltage

The charge pump output voltage level depends on the operating mode and is internally limited. The protected output can be used to supply other application with a limited supply range with respect to the total charge pump output current.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The charge pump output to regulated output differential at which the regulator output no longer maintains regulation against further reductions in charge pump output voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the charge pump input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

Circuit Description

The NCV48920 is an integrated low dropout regulator with integrated battery voltage charge pump buck/boost converter that provides a regulated voltage. The output current capability is 600 mA in buck mode and 300 mA in boost mode. Device is enabled with an input to the enable pin. The regulator voltage is provided by a PMOS pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Charge pump

The NCV48920 can operate in the three following modes: Buck, LDO and Boost Mode. In the basic view actual operation mode depends on input voltage level, charge pump output voltage level and output current value. The exact behavior are described in the section Charge Pump Operation Mode Selection.

Charge pump output voltage is internally limited to 15 V maximally. It is a protected output which can be used as an onboard voltage supply. Example is on Figure 34.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the gate of a PMOS series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PMOS is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Regulator Stability Considerations

The input capacitor (C_{in}) is necessary to stabilize the input impedance to avoid voltage line influences. The charge pump output capacitor (C_{CP}) reduces the voltage ripple at the charge pump output pin and serves as a voltage reservoir during switching between operation modes. The output capacitor (C_{out}) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor 10 μF (C_{out}), shown in Figure 1 should work for most applications; see also Figure 12 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 12 shows ESR values at which the regulated output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

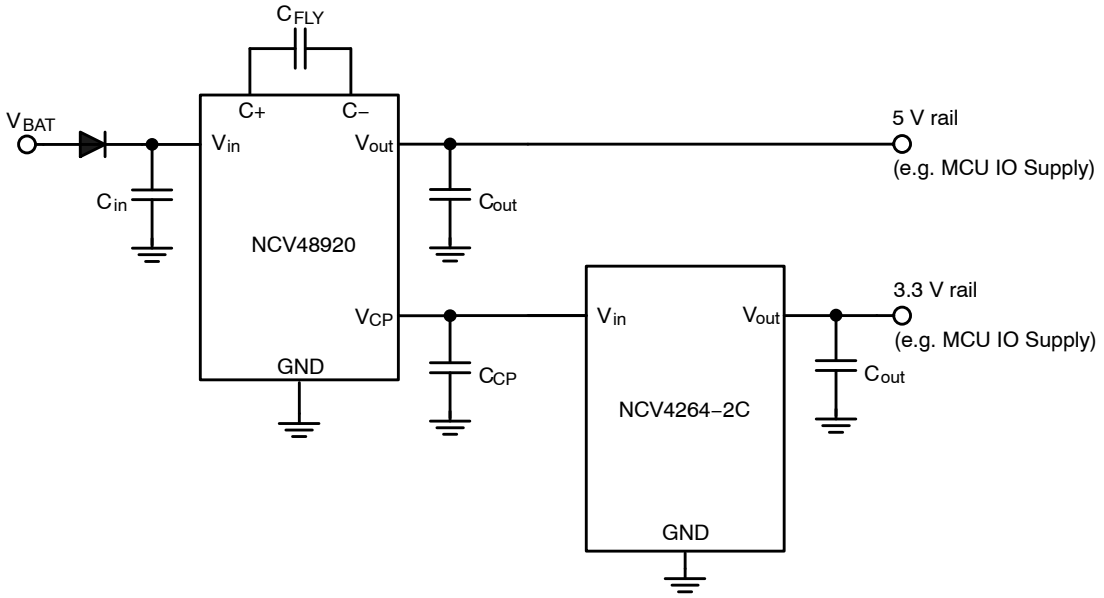


Figure 34. Onboard Dual Voltage Supply

List of recommended output capacitors:

GCM31CR71E475MA55 (4.7 μF, 25 V, X7R, 1206)
GCM31CC71E106MA03 (10 μF, 25 V, X7S, 1206)
KCM55WC71E107MH13 (100 μF, 25 V, X7S, 2220)

CGA5L1X7R1E475M (4.7 μF, 25 V, X7R, 1206)
CGA5L1X7R1E106M (10 μF, 25 V, X7R, 1206)
CKG57NX7S1C107M (100 μF, 16 V, X7S, 2220)

Charge Pump Capacitor Selection

Low ESR capacitors are necessary to minimize power losses. Especially in case of operation in buck or boost mode at a high load current. The exact value of C_{FLY} and C_{CP} is not strictly given. A 10 μF C_{FLY} is an optimum to yield maximum performance of the charge pump. Charge pump output impedance (R_{out_CP}) is given by Equation 1.

$$R_{out\_CP} \cong 2\times\sum(R_{SW}) + \frac{1}{f_{SW} \times C_{FLY}} + 4 \times ESR_{C_{FLY}} + ESR_{C_{CP}} \quad \text{(eq. 1)}$$

Charge pump output voltage ripple is determined by the value of C_{CP} and the load current (I_{out}). The C_{CP} is charged and discharged at a current roughly equal to the load current.

$$V_{ripple\_CP} = \frac{I_{out}}{2 \times f_{SW} \times C_{CP}} \quad \text{(eq. 2)}$$

This equation doesn't including the impact of non−overlap time and C_{CP} capacitor ESR. Since the output is not being driven during the non−overlap time, this time should be included in the ripple calculation. The C_{CP} capacitor discharge time is approximately 60% of a switching period

$$V_{ripple\_CP} = I_{out} \times \left(\frac{0.6}{f_{SW} \times C_{CP}} + 2 \times ESR_{C_{CP}}\right) \quad \text{(eq. 3)}$$

For example, with a 450 kHz switching frequency, a 10 μF C_{CP} capacitor with an ESR of 0.25 Ω and a 100 mA load the ripple voltage is 65 mV peak to peak.

Charge Pump Operation Mode Selection

The NCV48920 can operate in three different modes, which are LDO mode (simple LDO regulator), Boost mode (Step−Up regulator) and Buck mode (Step−Down regulator). The automated selection of the operation mode depends on the actual voltage level at the input supply pin, charge pump output pin and the actual output current level. Detailed operation mode selection is shown in Figure 35.

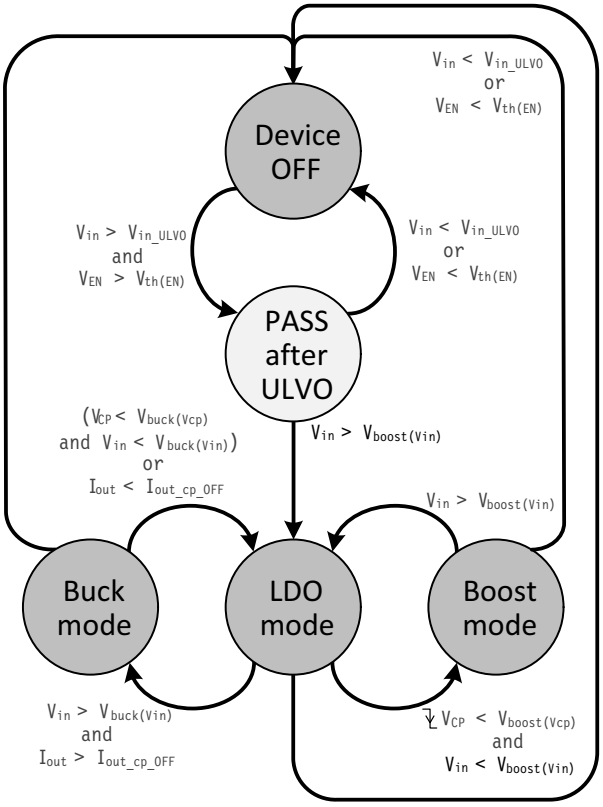


Figure 35. Flowchart for Operation Mode Selection

The NCV48920 starts always in LDO mode and stays in LDO mode until Buck or Boost mode is not activated. The conditions for switching from LDO mode to Buck mode are as follows:

$V_{in} > V_{buck(Vin)}$ AND $I_{out} > I_{out\_cp\_OFF}$

The conditions for switching from Buck mode to LDO mode are as follows:

($V_{in} < V_{buck(Vin)}$ AND $V_{CP} < V_{buck(Vcp)}$) OR $I_{out} < I_{out\_cp\_OFF}$

The conditions for switching from LDO mode to Boost mode are as follows:

($V_{CP} < V_{boost(Vcp)}$ AND $V_{in} < V_{boost(Vin)}$) AND in the past $V_{in} > V_{boost(Vin)}$

The condition for switching from Boost mode to LDO mode is as follow:

$V_{in} > V_{boost(Vin)}$

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin below 0.8 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.5 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

Thermal Considerations

As power in the NCV48920 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV48920 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV48920 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} + T_A\right]}{R_{\theta JA}} \quad \text{(eq. 4)}$$

Since T_J is not recommended to exceed 150°C, then the NCV48920 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2.1 W and up to 3.5 W for 3 layers PCB (all layers are 1 oz) when the ambient temperature (T_A) is 25°C. See Figure 36 for $R_{\theta JA}$ versus PCB area.

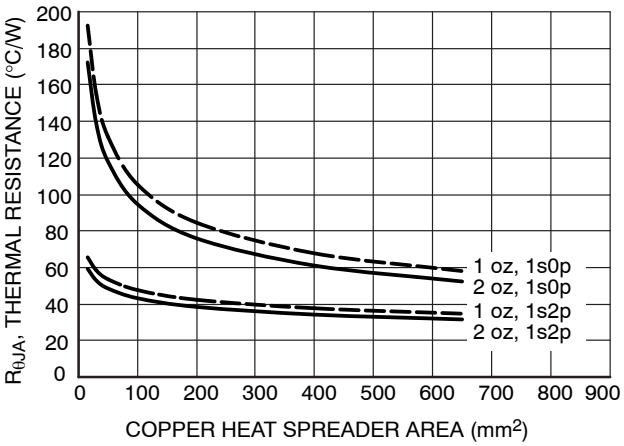


Figure 36. Thermal Resistance vs. PCB Copper Area (TSSOP−14 EP)

Power dissipated is given by three main parts. The first is dependent on the charge pump buck or boost mode activation. The second part including the power dissipated on LDO and the last represent current consumption.

CP active (boost mode):

$$P_{D\_CP1} = \left(2 \times V_{in} - V_{CP}\right) \times I_{out} \quad \text{(eq. 5)}$$

CP active (buck mode):

$$P_{D\_CP2} = \left(0.5 \times V_{in} - V_{CP}\right) \times I_{out} \quad \text{(eq. 6)}$$

CP inactive:

$$P_{D\_CP3} = \left(V_{in} - V_{CP}\right) \times I_{out} \quad \text{(eq. 7)}$$

$$P_{D\_LDO} = \left(V_{CP} - V_{out}\right) \times I_{out} \quad \text{(eq. 8)}$$

$$P_{D\_Iq} = V_{in} \times \left(I_q @ I_{out}\right) \quad \text{(eq. 9)}$$

The power dissipated by the NCV48920 can be calculated from the following equations depend on the operation mode:

$$P_{D1} = P_{D\_CP1} + P_{D\_LDO} + P_{D\_Iq} \quad \text{(eq. 10)}$$

$$P_{D2} = P_{D\_CP2} + P_{D\_LDO} + P_{D\_Iq} \quad \text{(eq. 11)}$$

$$P_{D3} = P_{D\_CP3} + P_{D\_LDO} + P_{D\_Iq} \quad \text{(eq. 12)}$$

Power dissipated by the NCV48920 can be also calculated from the equivalent resistance of the charge pump. In this case, the following equations can used.

CP active (boost mode):

$$P_{D\_CP\_Req1} = R_{out\_CP(boost)} \times {I_{out}}^2 \quad \text{(eq. 13)}$$

$$P_{D\_CPreg1} = \left(\left(2 \times V_{in} - R_{out\_CP(boost)} \times I_{out}\right) - V_{CP}\right) \times I_{out} \quad \text{(eq. 14)}$$

CP active (buck mode):

$$P_{D\_CP\_Req2} = R_{out\_CP(buck)} \times {I_{out}}^2 \quad \text{(eq. 15)}$$

$$P_{D\_CPreg2} = \left(\left(0.5 \times V_{in} - R_{out\_CP(buck)} \times I_{out}\right) - V_{CP}\right) \times I_{out} \quad \text{(eq. 16)}$$

CP inactive:

$$P_{D\_CP3} = 0 \quad \text{(eq. 17)}$$

$$P_{D\_CPreg3} = \left(V_{in} - V_{CP}\right) \times I_{out} \quad \text{(eq. 18)}$$

$$P_{D\_LDO} = \left(V_{CP} - V_{out}\right) \times I_{out} \quad \text{(eq. 19)}$$

$$P_{D4} = P_{D\_CP\_Req1} + P_{D\_CPreg1} + P_{D\_LDO} \quad \text{(eq. 20)}$$

$$P_{D5} = P_{D\_CP\_Req2} + P_{D\_CPreg2} + P_{D\_LDO} \quad \text{(eq. 21)}$$

$$P_{D6} = P_{D\_CP\_Req3} + P_{D\_CPreg3} + P_{D\_LDO} \quad \text{(eq. 22)}$$

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

Place filter components as near as possible to the device to increase EMC performance.

Input Capacitor C_{in} is required if regulator is located far from power supply filter. If extremely fast input voltage transients are expected with slew rate in excess of 4 V/μs then appropriate input filter must be used. The filter can be composed of several capacitors in parallel.

The NCV48920 is not developed in compliance with ISO26262 standard. If application is safety critical then the application example diagram shown in Figure 37 can be used.

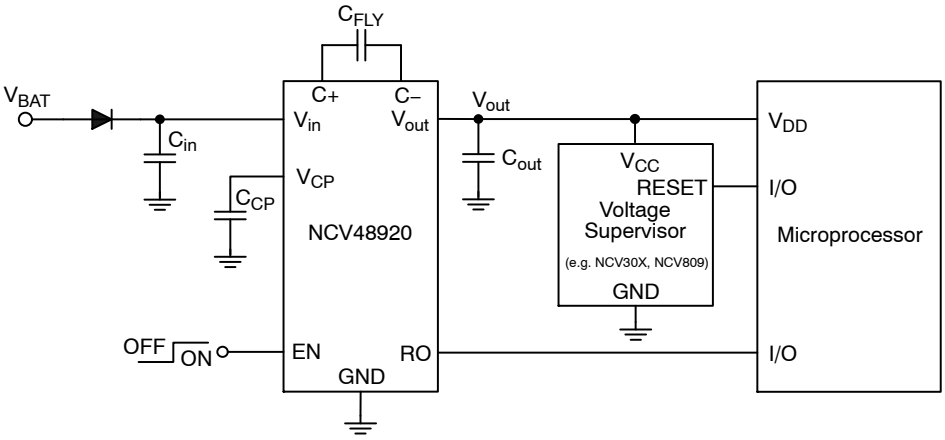


Figure 37. Application Diagram

ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time††	Marking	Package	Shipping†
NCV48920PA50R2G	5.0 V	0 ms	Line 1: V489 Line 2: 2050	TSSOP−14 EP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

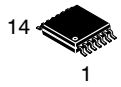
††For information about another Output Voltage, Reset Delay Time, Packages options contact factory. Reset Delay Time can be chosen from following list of values: 0, 2, 4, 8, 16, 32, 64 and 128 ms.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

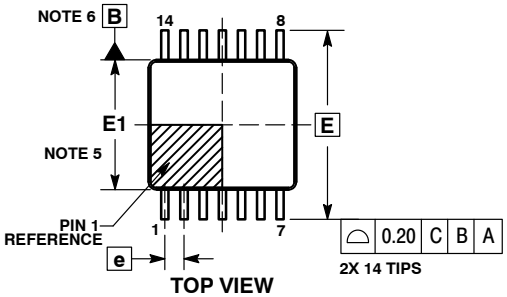
ON Semiconductor®

TSSOP−14 EP
CASE 948AW
ISSUE C

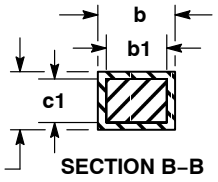
DATE 09 OCT 2012



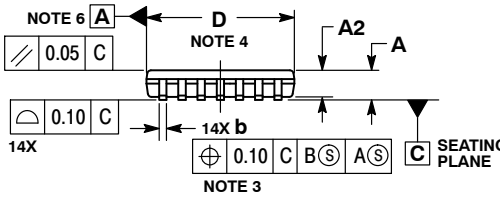
SCALE 1:1



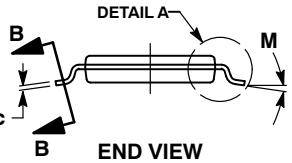
TOP VIEW



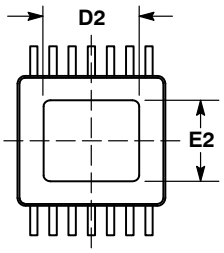
SECTION B−B
NOTE 8



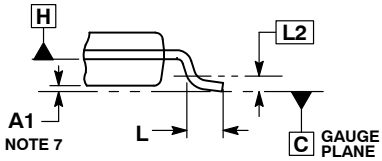
SIDE VIEW



END VIEW



BOTTOM VIEW

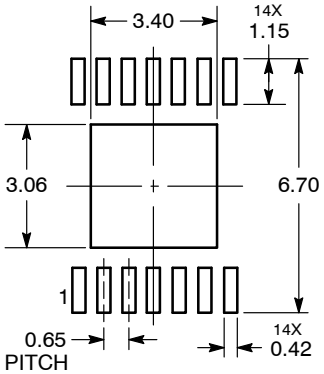


DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	----	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

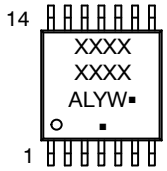
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−14 EP, 5.0X4.4**	**PAGE 1 OF 1**

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