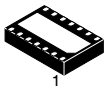
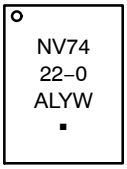
LIN Transceiver, Dual

NCV7422



DFN14
MW SUFFIX
CASE 507AC

MARKING DIAGRAM



NV7422−0 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year of Production, Last Number
W = Work Week
▪ = Pb−Free Package

Description

The NCV7422 is a two channel physical layer device using the Local Interconnect Network (LIN) protocol. It allows interfacing of two independent LIN physical buses and the LIN protocol controllers. The device is compliant to ISO 17987−4, LIN2.2a, LIN2.2, LIN2.1, LIN 2.0 and SAEJ2602 standards.

The NCV7422 LIN device is a member of the in−vehicle networking (IVN) transceiver family.

The LIN bus is designed to communicate low−rate data from control devices such as door locks, mirrors, car seats and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU−state machine that recognizes and translates the instructions specific to that function.

The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

Features

- DFN−14 Green Package (Pb−Free)

LIN−Bus Transceiver

- Compliant to ISO 17987−4 (Backwards Compatible to LIN Specification rev. 2.x, 1.3) and SAE J2602
- Bus Voltage ±42 V
- Transmission Rate 1 kbps to 20 kbps
- TxD Timeout Function
- Integrated Slope Control

Protection

- Thermal Shutdown
- Undervoltage Detection
- Bus Pins Protected Against Transients in an Automotive Environment

Modes

- Normal Mode: LIN Transceiver Enabled, Communication via the Bus is Possible
- Sleep Mode: LIN Transceiver Disabled, the Consumption from V_{BB} is Minimized
- Standby Mode: Transition Mode Reached after Wake−Up Event on LIN Bus

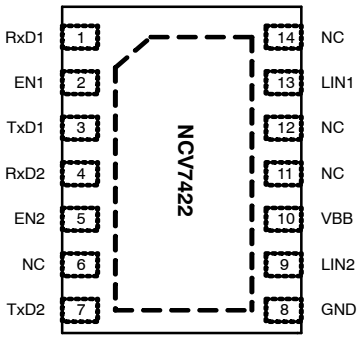
Compatible

- Pin−Compatible with NCV7329 DFN8 Package
- K−line Compatible

Quality

- Wettable Flank Package for Enhanced Optical Inspection
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

BLOCK DIAGRAM

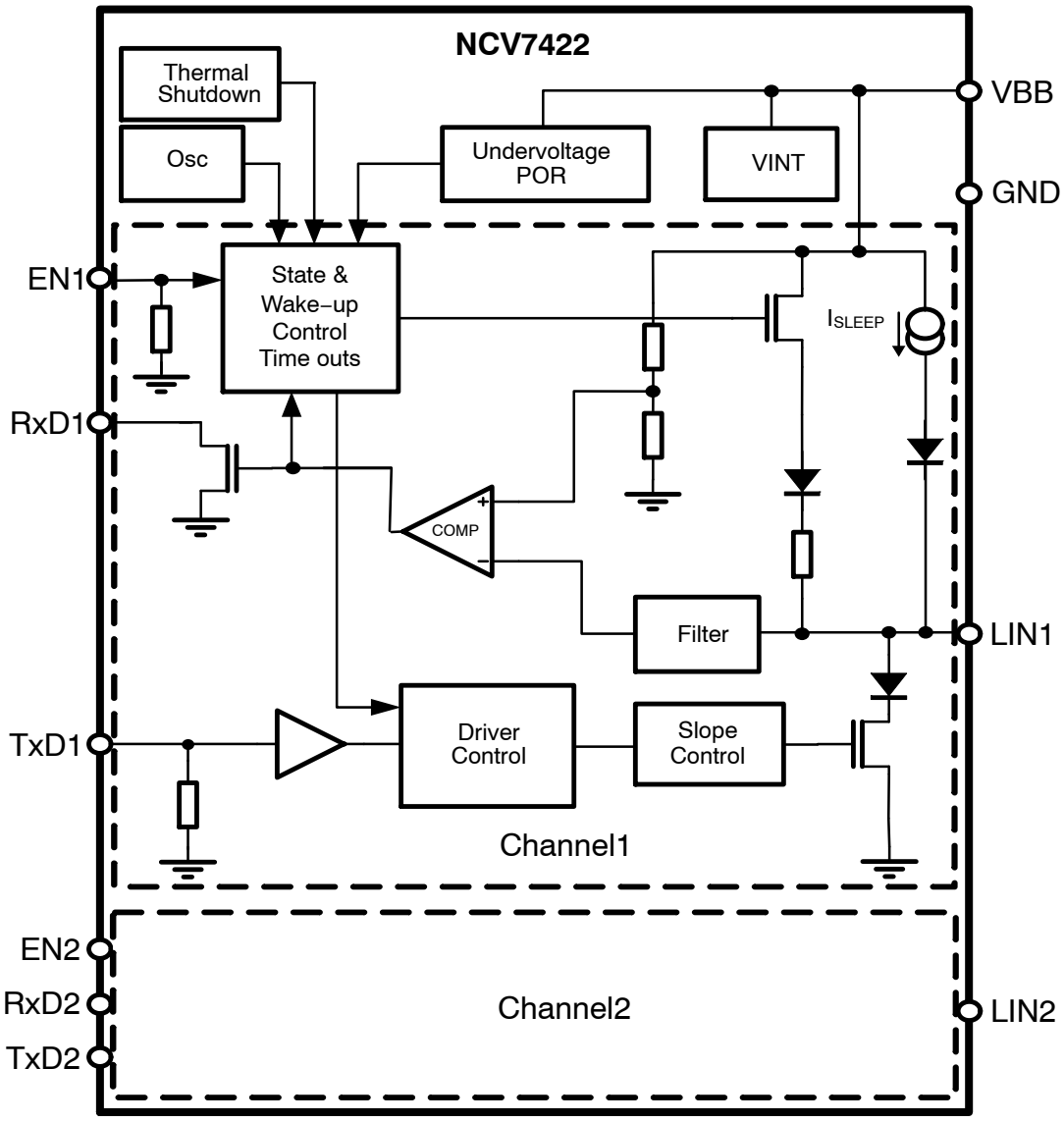


Figure 1. Block Diagram

TYPICAL APPLICATION DIAGRAM

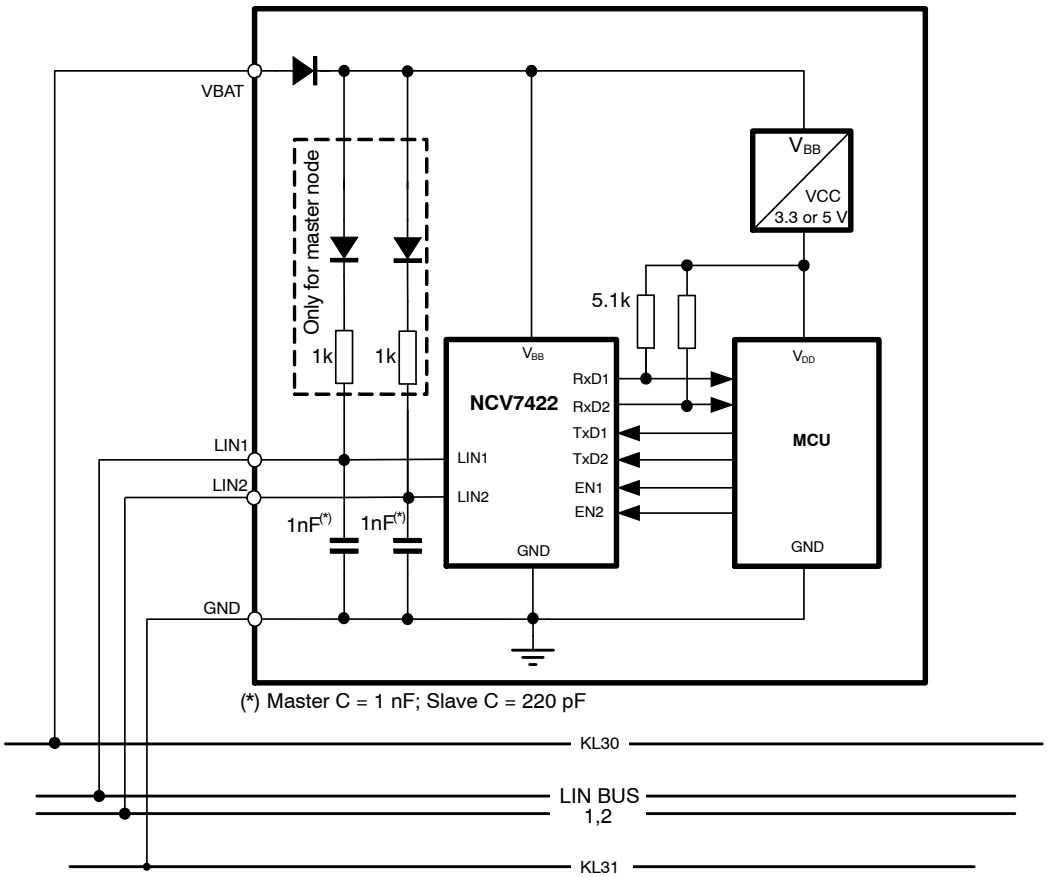


Figure 2. Application Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin DFN14	Name	Description
1	RxD1	Receive Data Output 1; Low in Dominant State; Open−Drain Output
2	EN1	Enable Input 1; Transceiver in Normal Operation Mode when High
3	TxD1	Transmit Data Input 1; Low for Dominant State; Pull−Down to GND
4	RxD2	Receive Data Output 2; Low in Dominant State; Open−Drain Output
5	EN2	Enable Input 2; Transceiver in Normal Operation Mode when High
6	NC	Not Connected
7	TxD2	Transmit Data Input 2; Low for Dominant State; Pull−Down to GND
8	GND	Ground
9	LIN2	LIN Bus Output / Input Channel 2
10	V_{BB}	Battery Supply Input
11	NC	Not Connected
12	NC	Not Connected
13	LIN1	LIN Bus Output / Input Channel 1
14	NC	Not Connected
−	EP	Exposed Pad. Recommended to connect to GND or Left Floating in Application

FUNCTIONAL DESCRIPTION

Overall Function Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications.

The NCV7422 contains two LIN transmitters, LIN receivers, power−on−reset (POR) circuit and thermal shutdown (TSD). The LIN transmitters are optimized for a maximum specified transmission speed of 20 kbps.

Table 2. OPERATING MODES

Pin ENx	Mode	Pin RxDx	LIN bus
x	Unpowered	Floating	OFF; Floating
Low	Sleep	Floating	OFF; Floating
Low	Standby	Low indicates wakeup	OFF; 30 kΩ
High	Normal	LOW: dominant HIGH: recessive	ON; 30 kΩ

Unpowered Mode

As long as V_{BB} remains below its power−on−reset level, the chip is kept in a safe unpowered state. LINs transmitters are inactive, LINx pins are left floating. Pins RxDx remain floating.

The unpowered state will be entered from any other state when V_{BB} falls below its power−on−reset level (PORL_VBB). When V_{BB} rises above power−on−reset high threshold level (PORH_VBB) the NCV7422 switches to Sleep mode.

Normal Mode

In normal mode, the full functionality of the LIN transceivers are available. Transceivers can transmit and receive data via LIN bus with speed up to 20 kbps. Data according the state of TxDx inputs are sent to the corresponding LIN bus while pin RxDx reflects the logical symbol received on the LIN bus − high−impedant for recessive and Low for dominant. A 30 kΩ resistor in series with reverse−protection diode is internally connected between LIN and V_{BB} pins.

The signal on pin TxDx passes through a timer, which releases the bus in case the TxDx remains low for longer than $t_{TxD\_TIMEOUT}$. It prevents the LIN bus being permanently driven dominant and thus blocking all subsequent communication due to a failure of the application (e.g. software error). The transmission can continue once the TxDx returns to High logical level.

In case the junction temperature increases above the thermal shutdown threshold ($T_{J(sd)}$), e.g. due to a short of the LIN wiring to the battery, the transmitter is disabled and releases LIN buses to recessive. Once the junction temperature decreases back below the thermal shutdown release level, the transmission can be enabled again – however, to avoid thermal oscillations, first a High logical level on TxDx must be encountered before the transmitter is enabled.

As required by SAE J2602, the transceiver must behave safely below its operating range – it shall either continue to transmit correctly (according its specification) or remain silent (transmit a recessive state regardless of the TxDx signal). A battery monitoring circuit in NCV7422 deactivates the transmitters in the Normal mode if the VBB level drops below MONL_VBB. Transmission is enabled again when VBB reaches MONH_VBB. The internal logic remains in the normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power−on−reset levels are overlapping, it's ensured by the implementation that the monitoring level never falls below the power−on−reset level.

The Normal mode can be entered from either standby or sleep mode when ENx pin is High for longer than t_{ENABLE}. When the transition is made from standby mode, RxDx is put high−impedance immediately after ENx becomes High (before the expiration of t_{ENABLE} filtering time). This excludes signal conflicts between the standby mode pin settings and the signals required to control the chip in the normal mode after local wake−up vs. High logical level on TxDx required to send a recessive symbol on LIN.

Sleep Mode

Sleep mode provides low current consumption. The LIN transceiver is inactive and the battery consumption is minimized.

This mode is entered in one of the following ways:

- After voltage level at V_{BB} pin rises above its power−on−reset level (PORH_VBB). In this case, RxD pins remain high−impedant.
- After assigning Low logical level to pin ENx for longer than $t_{DISABLE}$ while corresponding NCV7422 transceiver is in Normal mode. The LIN transmit path is immediately disabled when EN pin goes low.

Standby Mode

Standby mode is entered from Sleep mode when remote wake−up event occurred. Low level on RxDx pins indicates the interrupt flag for the microcontroller.

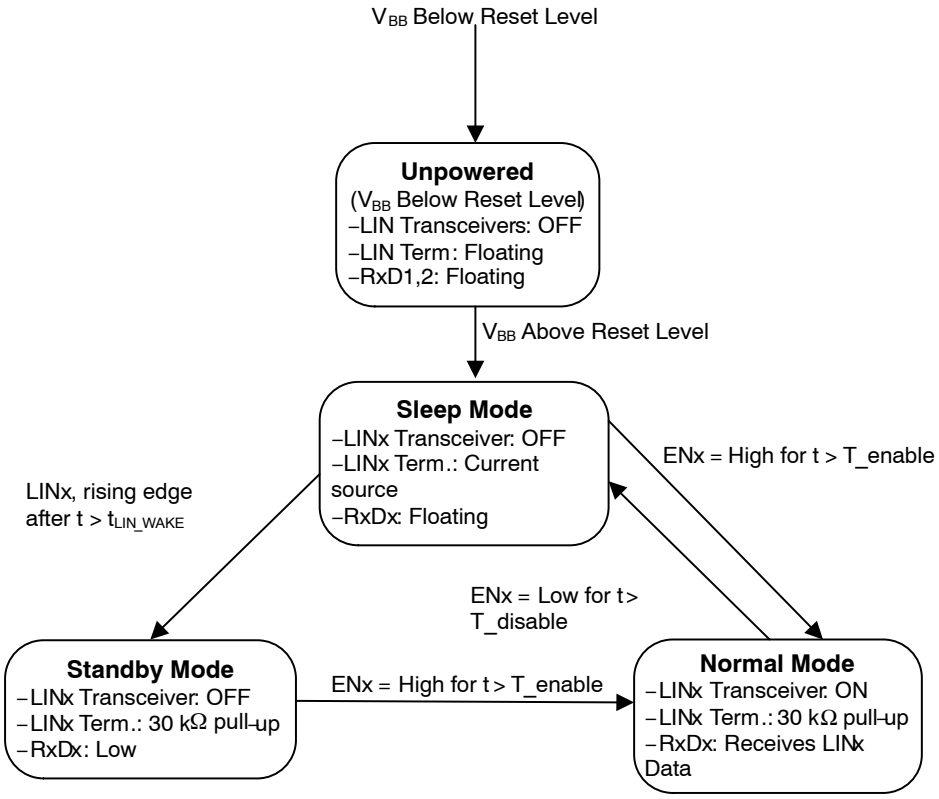


Figure 3. State Diagram

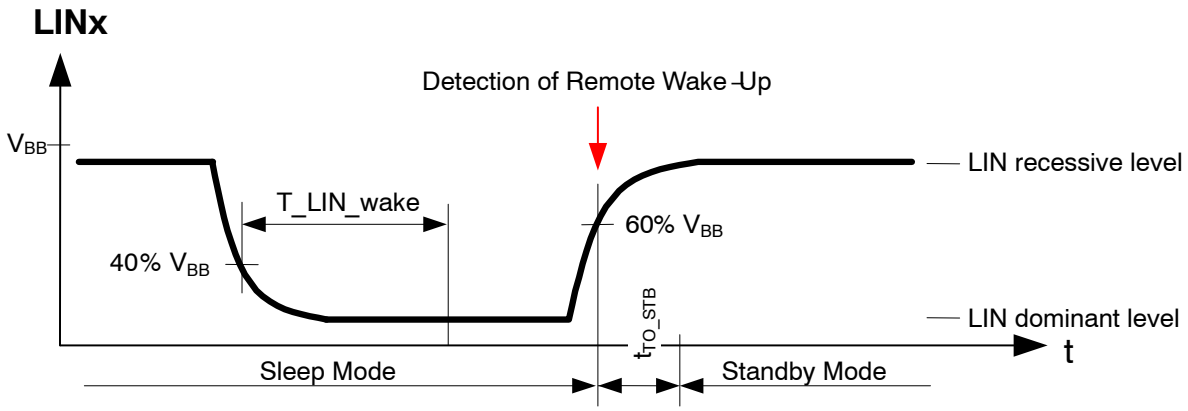


Figure 4. Remote (LIN) Wake−up Detection

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND unless otherwise specified. Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{BB}	Supply Voltage on Pin V_{BB}	−0.3	+42	V
V_{LINx}	LIN Bus Voltage with respect to GND	−42	+42	V
	LIN Bus Voltage with respect to V_{BB}	−42	+42	V
$V_{\_DIG\_IO}$	DC Voltage on Pins (ENx, RxDx, TxDx)	−0.3	+7	V
V_{ESD}	Human Body Model (LINx pin) (Note 1)	−8	+8	kV
	Human Body Model (All pins) (Note 1)	−4	+4	kV
	Charge Device Model (All pins) (Note 2)	−750	+750	V
	Machine Model (All pins) (Note 3)	−200	+200	V
V_{ESDIEC}	Electrostatic Discharge Voltage (LINx Pin) System Human Body Model (Note 4) Conform to IEC 61000−4−2	−8	+8	kV
T_J	Junction Temperature	−40	+150	°C
T_{STG}	Storage Temperature	−55	+150	°C
T_{SLD}	Peak Soldering Temperature (Note 5)	+260		°C
MSL_{DFN}	Moisture Sensitivity Level for DFNW14	1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC−Q100−011.
3. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and 0.75 μH coil.
4. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test−house.
5. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 4. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, JEDEC 1S0P PCB	Free air; (Note 6)	100	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, JEDEC 2S2P PCB	Free air; (Note 7)	51	K/W

6. Test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
7. Test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

Table 5. ELECTRICAL CHARACTERISTICS (V_{BB} = 5 V to 18 V; T_J = −40 to +150°C; Typical values are given at V_{BB} = 12 V and T_J = 25°C Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{BB})						
V_{BB}	Battery Supply		5.0	−	18	V
I_{BB}	Battery Supply Current − Both Channels	Normal Mode; LIN recessive	0.4	1.1	2.4	mA
		Normal Mode; TxDx = Low, both LINs Dominant	4.0	7.8	13	mA
		Sleep and Standby Mode; T_J < 85°C LIN recessive; $V_{LINx} = V_{BB}$	−	6.0	10	μA
		Sleep and Standby Mode; LIN recessive; $V_{LINx} = V_{BB}$	−	6.0	15	μA

Table 5. ELECTRICAL CHARACTERISTICS (V_{BB} = 5 V to 18 V; T_J = −40 to +150°C; Typical values are given at V_{BB} = 12 V and T_J = 25°C Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POR AND V_{BB} MONITOR						
PORH_V_{BB}	Power−on Reset; High Level on V_{BB}	V_{BB} Rising	2.7	3.5	4.4	V
PORL_V_{BB}	Power−on Reset; Low Level on V_{BB}	V_{BB} Falling	1.3	2.1	2.7	V
MONH_V_{BB}	Battery Monitoring High Level	V_{BB} Rising	3.2	4.2	5.0	V
MONL_V_{BB}	Battery Monitoring Low Level	V_{BB} Falling	3.0	4.0	4.8	V
TRANSMITTER DATA INPUT (Pin TxDx)						
V_{IL_TxD}	Low Level Input Voltage		−0.3	–	+0.8	V
V_{IH_TxD}	High Level Input Voltage		2.0	–	7.0	V
R_{PD_TxD}	Pull−down Resistor on TxDx Pin		50	125	325	kΩ
RECEIVER DATA OUTPUT (Pin RxDx)						
I_{OL_RxD}	Low Level Output Current	V_{RXDX} = 0.4V	2.0	–	–	mA
I_{OH_RxD}	High Level Leakage Current		−1.0	–	+1.0	μA
ENABLE INPUT (Pin ENx)						
V_{IL_EN}	Low Level Input Voltage		−0.3	–	+0.8	V
V_{IH_EN}	High Level Input Voltage		2.0	–	7.0	V
R_{PD_EN}	Pull−down Resistor to Ground		100	250	650	kΩ
LIN BUS LINE (Pin LINx)						
V_{BUS_DOM}	Bus Voltage for Dominant State		–	–	0.4V_{BB}	V
V_{BUS_REC}	Bus Voltage for Recessive State		0.6V_{BB}	–	–	V
V_{REC_DOM}	Receiver Threshold	LIN Bus Recessive − Dominant	0.4V_{BB}	–	0.6V_{BB}	V
V_{REC_REC}	Receiver Threshold	LIN Bus Dominant − Recessive	0.4V_{BB}	–	0.6V_{BB}	V
V_{REC_CNT}	Receiver Centre Voltage	(V_{REC_DOM} + V_{REC_REC}) / 2	0.475V_{BB}	0.500V_{BB}	0.525V_{BB}	V
V_{REC_HYS}	Receiver Hysteresis	(V_{REC_REC} − V_{REC_DOM})	0.050V_{BB}	–	0.175V_{BB}	V
V_{LIN_DOM}	Dominant Output Voltage	Normal mode; V_{BB} = 7 V	–	–	1.2	V
		Normal mode; V_{BB} = 18 V	–	–	2.0	V
$I_{BUS\_no\_GND}$	Communication not Affected	V_{BB} = GND = 12 V; 0 < V_{LIN} < 18 V	−1.0	–	+1.0	mA
$I_{BUS\_no\_VBB}$	LIN Bus Remains Operational	V_{BB} = GND = 0 V; 0 < V_{LIN} < 18 V	–	–	5.0	μA
I_{BUS_LIM}	Current limitation for Driver	Dominant State; V_{LIN} = V_{BB_MAX}	40	–	200	mA
$I_{BUS\_PAS\_dom}$	Receiver Leakage current; Driver OFF	V_{LIN} = 0 V; V_{BB} = 12 V	−1	–	–	mA
Isleep	Receiver Leakage current; see Figure 1	Sleep mode; VLIN = 0 V; VBB = 12 V	−16	−8.0	−3.0	μA
$I_{BUS\_PAS\_rec}$	Receiver Leakage current; Driver OFF; (Note 8)	TxD = High; 8 V < V_{BB} < 18 V; 8 V < V_{LIN}<18 V; V_{LIN} ≥ V_{BB}	–	–	20	μA
$V_{SERDiode}$	Voltage Drop on Serial Diode	Voltage drop on DS, see Figure 1	0.4	0.7	1.0	V
R_{SLAVE}	Internal Pull−up Resistance	see Figure 1	20	30	60	kΩ
C_{LIN}	Capacitance on Pin LIN (Note 8)		–	20	30	pF
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown Junction Temperature	Temperature Rising	160	180	200	°C

8. Values based on design and characterization. Not tested in production.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. AC CHARACTERISTICS (V_{BB} = 5 V to 18 V; T_J = −40 to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(MIN)}$ / ($2xt_{BIT}$); See Figure 5	$TH_{REC(max)}$ = 0.744 x V_{BB} $TH_{DOM(max)}$ = 0.581 x V_{BB} t_{BIT} = 50 μs V_{BB} = 5 V to 18 V	0.396	–	0.500	
D2	Duty Cycle 2 = $t_{BUS\_REC(MAX)}$ / ($2xt_{BIT}$); See Figure 5	$TH_{REC(max)}$ = 0.422 x V_{BB} $TH_{DOM(max)}$ = 0.284 x V_{BB} t_{BIT} = 50 μs V_{BB} = 5 V to 18 V	0.500	–	0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(MIN)}$ / ($2xt_{BIT}$); See Figure 5	$TH_{REC(max)}$ = 0.778 x V_{BB} $TH_{DOM(max)}$ = 0.616 x V_{BB} t_{BIT} = 96 μs V_{BB} = 5 V to 18 V	0.417	–	0.500	
D4	Duty Cycle 4 = $t_{BUS\_REC(MAX)}$ / ($2xt_{BIT}$); See Figure 5	$TH_{REC(max)}$ = 0.389 x V_{BB} $TH_{DOM(max)}$ = 0.251 x V_{BB} t_{BIT} = 96 μs V_{BB} = 5 V to 18 V	0.500	–	0.590	
$t_{TX\_PROP\_DOWN}$	Propagation Delay of TxDx to LINx. TxDx High to Low; See Figure 7		–	–	14	μs
$t_{TX\_PROP\_UP}$	Propagation Delay of TxDx to LINx. TxDx Low to High; See Figure 7		–	–	14	μs
LIN RECEIVER						
t_{RX_PD}	Propagation Delay of Receiver Rising and falling Edge (see Figure 6)	R_{RxDx} = 2.4 kΩ; C_{RxDx} = 20 pF	0.1	–	6.0	μs
t_{REC_SYM}	Propagation Delay Symmetry	R_{RxDx} = 2.4 kΩ; C_{RxDx} = 20 pF; Rising Edge with Respect to Falling Edge	−2.0	–	+2.0	μs
MODE TRANSITIONS AND TIMEOUTS						
t_{LIN_WAKE}	Duration of LIN Dominant for Detection of Wake−up via LIN Bus (See Figure 4)	Sleep Mode	40	70	150	μs
$t_{TxD\_TIMEOUT}$	TxDx Dominant Time−out	Normal Mode, TxDx = Low	14	25	46	ms
t_{INIT_NORM}	Time from Rising Edge of ENx pin to the moment when the Transmitter is able to correctly transmit		15	30	75	μs
t_{ENABLE}	Duration of ENx pin in High Level State for transition to Normal Mode		11	20	55	μs
$t_{DISABLE}$	Duration of ENx pin in Low Level State for transition to Sleep Mode		11	20	55	μs
t_{TO_STB}	Delay from LIN Bus Dominant to Recessive Edge to Entering of Standby Mode after Valid LIN Wake−up	Sleep Mode	5.0	10	40	μs

MEASUREMENT SETUPS AND DEFINITIONS

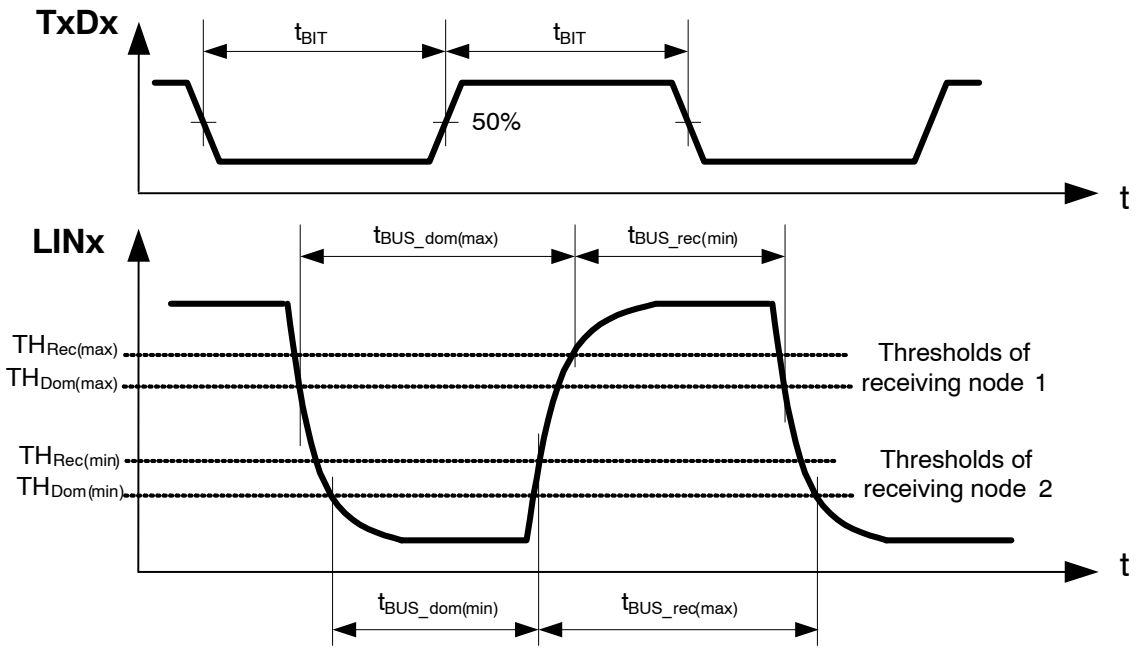


Figure 5. LIN Transmitter Duty Cycle

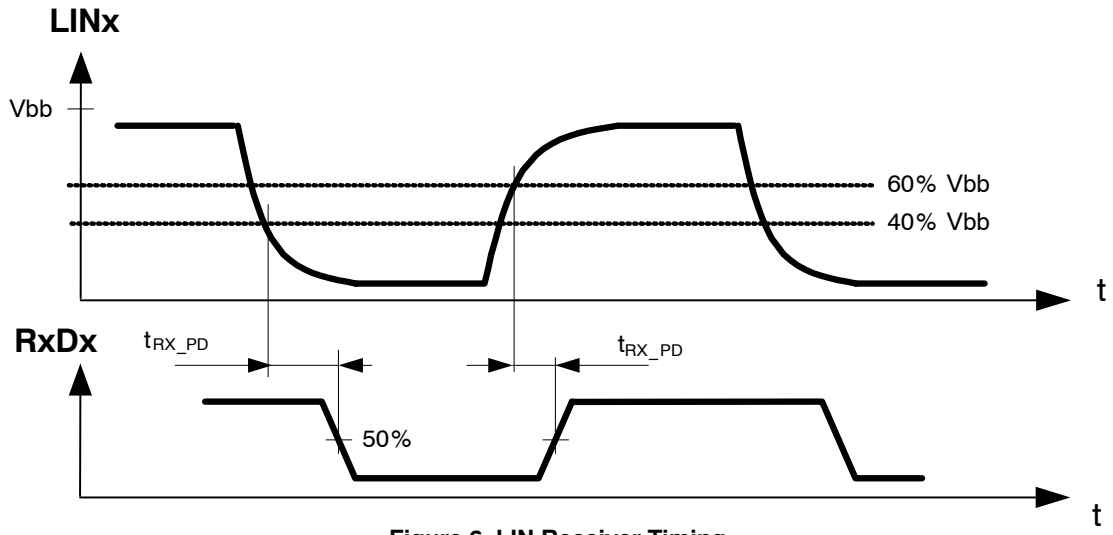


Figure 6. LIN Receiver Timing

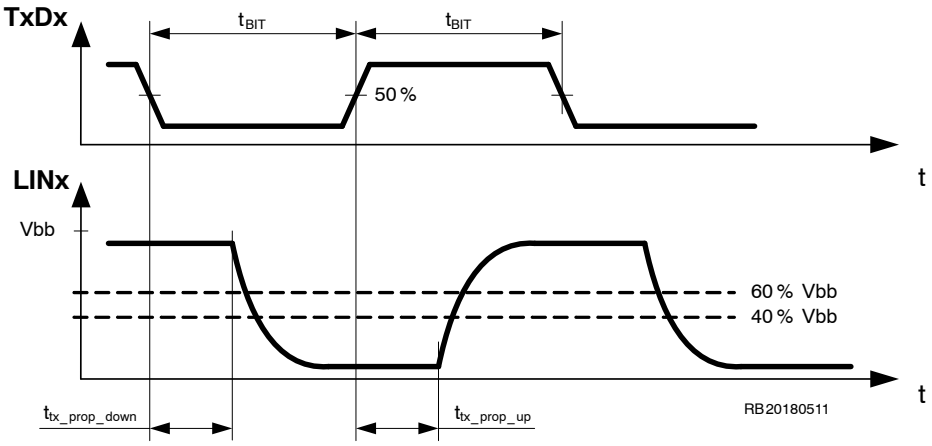
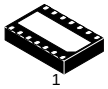


Figure 7. LIN Transmitter Timing

ORDERING INFORMATION

Device	Description	Temperature Range	Package	Shipping†
NCV7422MW0R2G	LIN Transceiver, Dual	−40°C to 150°C	DFN14 (Pb−Free)	5000 / Tape & Reel

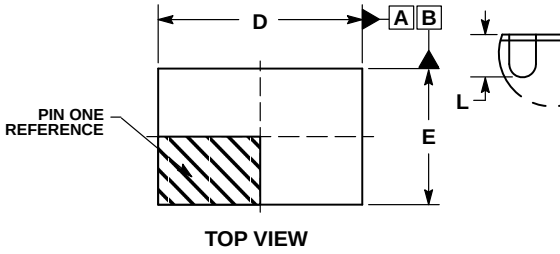
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

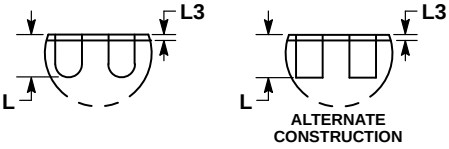


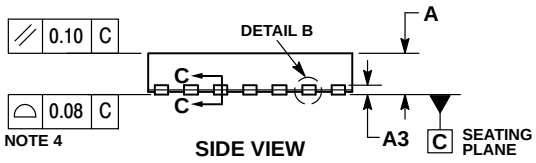
SCALE 2:1

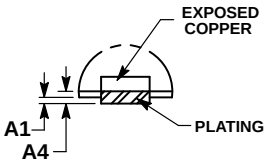
DFNW14 4.5x3, 0.65P
CASE 507AC
ISSUE D

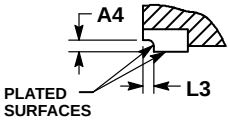
DATE 03 JUL 2018

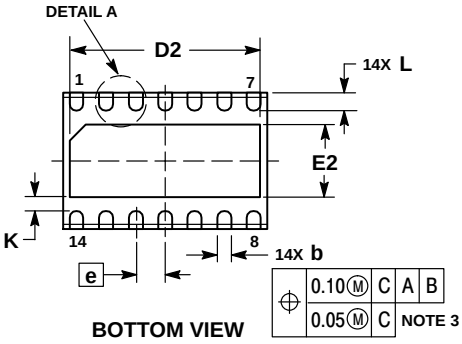








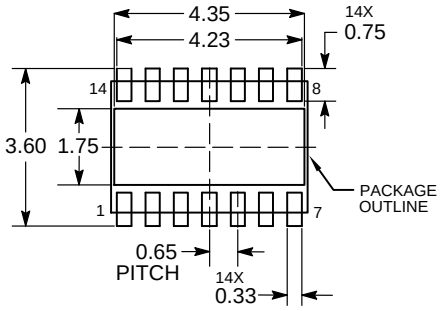




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	−−−	−−−	0.05
A3	0.20 REF		
A4	0.10	−−−	−−−
b	0.25	0.30	0.35
D	4.40	4.50	4.60
D2	4.13	4.20	4.27
E	2.90	3.00	3.10
E2	1.53	1.60	1.67
e	0.65 BSC		
K	0.30 REF		
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

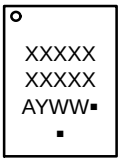
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW14 4.5x3, 0.65P**		**PAGE 1 OF 1**

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