Quad High-side Driver

NCV760040

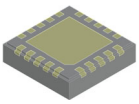
The NCV760040 is an automotive grade integrated driver with four high−side switches. The device features per−channel adjustable current limit and is protected for overtemperature conditions. Output control and diagnostic reporting is performed via I^2C bus. Current sense data is provided through I^2C in addition to a multiplexed analog current sense output pin. The NCV760040 is available in a QFNW20 3.5 x 3.5 mm step−cut package with wettable flanks and features an exposed pad for optimal thermal performance.

Features

- 4 High−side Channels
- 1.2 A Peak Current Per Channel
- RDS(ON) = 500 mΩ Typical, 1.0 Ω Max
- Global Enable Pin
- Low Quiescent Current in Sleep Mode
- Status Reporting via I^2C and via Open−drain Fault Pin
- Current Sense Readout via I^2C and via CS Pin
- Baseline Current Limit Set via External Resistor with Per−channel Current Limit Shift via I^2C
- Overtemperature Shutdown
- Short to Battery Protection with Per−channel Reverse Current Blocking
- Open Load Detection
- Loss of Ground Protection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Camera Switch
- LEDs, Sensors
- Advanced Driver Assistance Systems (ADAS)
- Infotainment
- Power Over Coax (PoC)



QFNW20
3.5x3.5, 0.5P
CASE 484AV

MARKING DIAGRAM

NCV760040 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCV760040MWTXG	QFNW20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Application Diagram

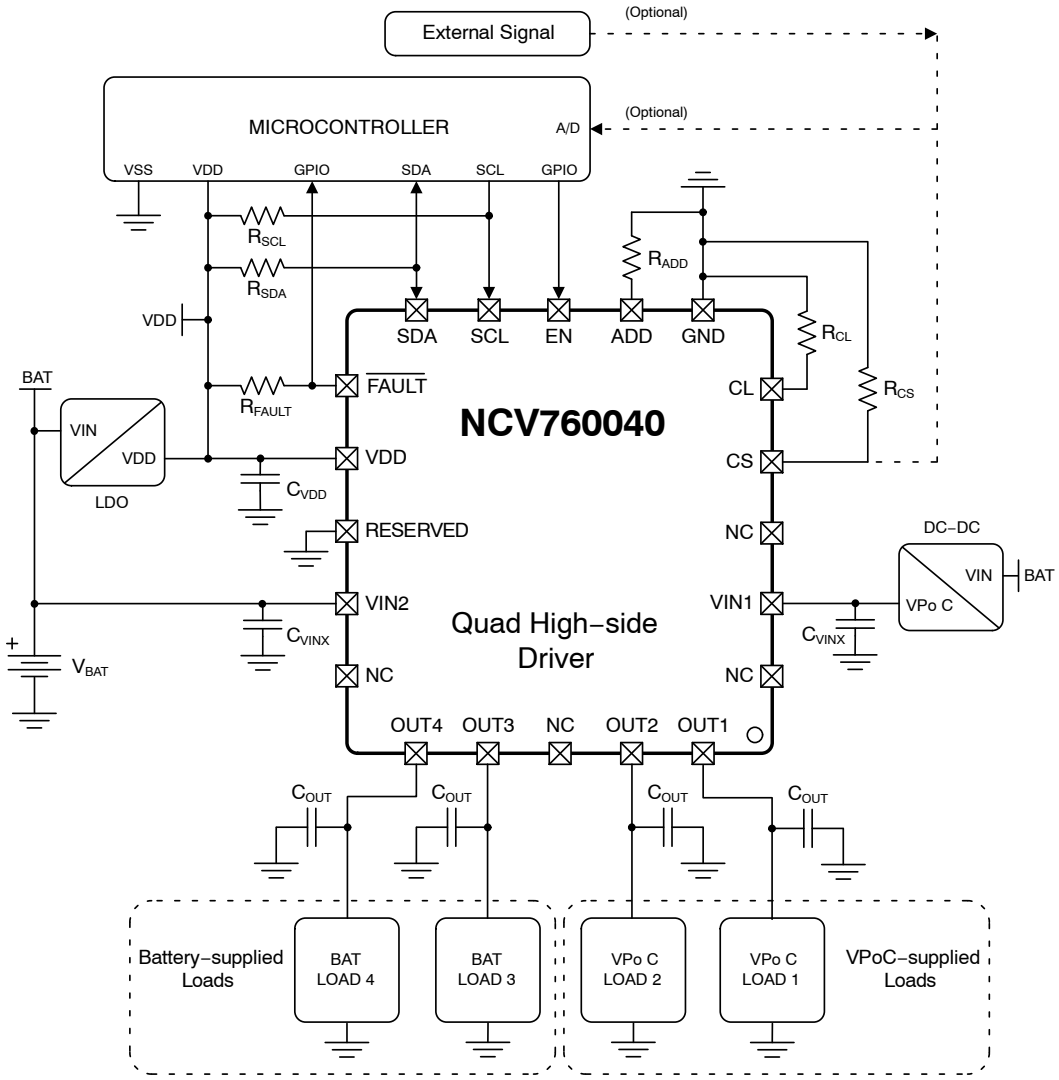


Figure 1. Typical Application

Table 1. RECOMMENDED EXTERNAL COMPONENTS

Reference	Pin	Value
C_{VINx}	VIN1, VIN2	10 μF // 0.1 μF
C_{VDD}	VDD	0.1 μF
R_{ADD}	ADD	470 Ω to 100.0 kΩ
R_{SDA}	SDA	4.7 kΩ
R_{SCL}	SCL	4.7 kΩ
R_{CS}	CS	330 Ω
R_{CL}	CL	2.5 kΩ to 30 kΩ
R_{FAULT}	FAULT	4.7 kΩ
C_{OUT}	OUT1 − 4	0.1 μF

Block Diagram

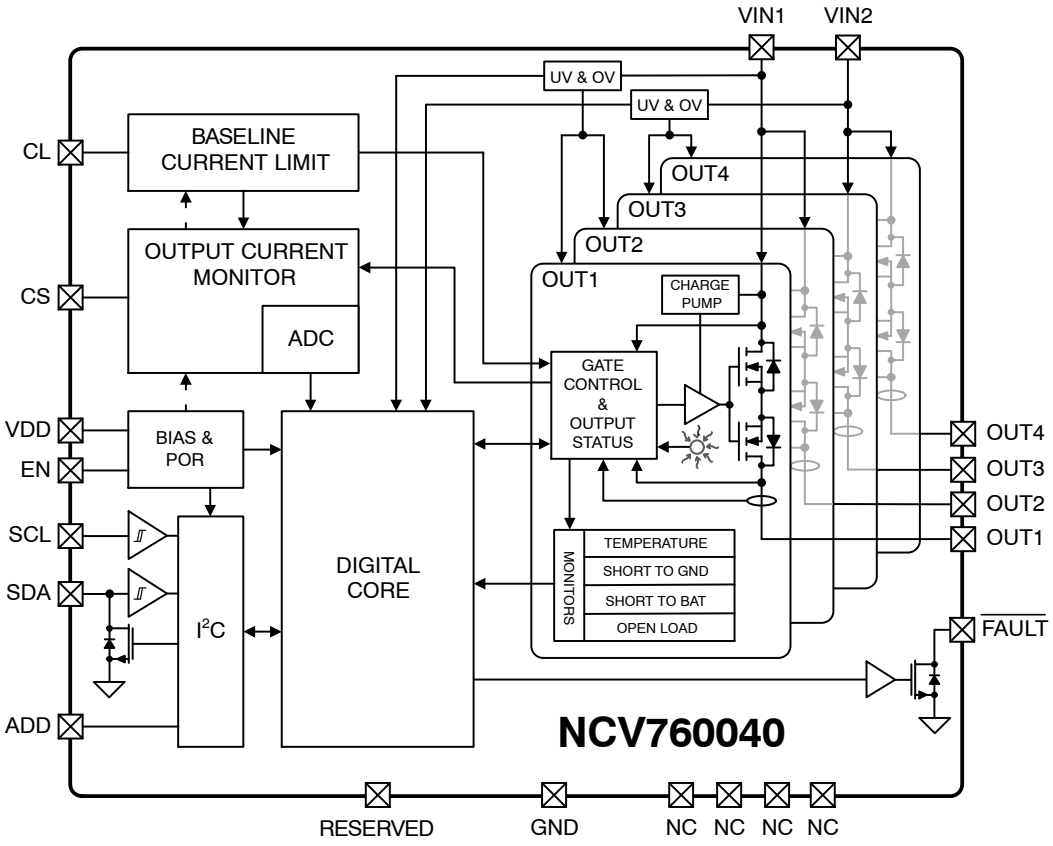


Figure 2. Block Diagram

QFNW20 Pinout Diagram

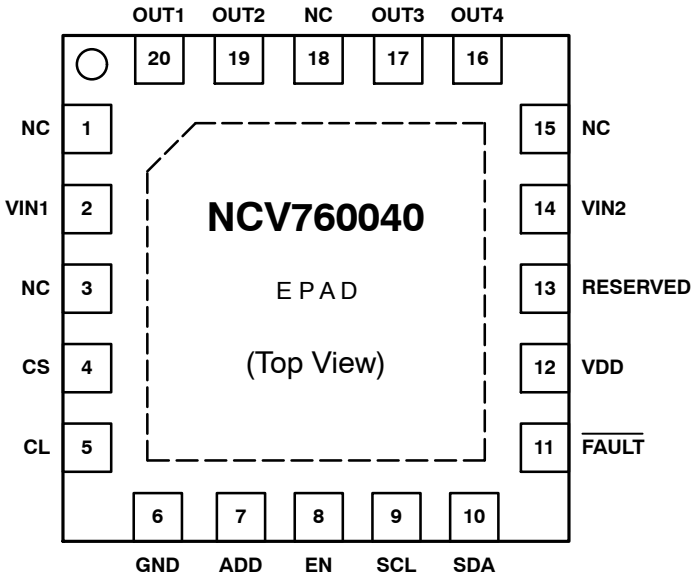


Figure 3. Pinout – QFNW20 (Top View)

Table 2. PIN FUNCTION DESCRIPTION

QFNW20	Symbol	Description
1	NC	No Connection. Leave floating or connected to GND.
2	VIN1	Power supply input for high−side outputs OUT1 and OUT2.
3	NC	No Connection. Leave floating or connected to GND.
4	CS	Current sense output. Connect a resistor to GND for ADC functionality.
5	CL	Baseline current limit setting. Connect a resistor to GND for ILIM functionality.
6	GND	Ground. Common reference node and VDD power supply return.
7	ADD	I^2C address selection. Connect a resistor to GND to set the target device I^2C address.
8	EN	Active−high enable input. Wakes the device from sleep mode and enables the I^2C bus.
9	SCL	I^2C clock input. Connect a pull−up resistor to VDD.
10	SDA	I^2C data input/open−drain output. Connect a pull−up resistor to VDD.
11	$\overline{\text{FAULT}}$	Active−low fault flag output. Connect a pull−up resistor to VDD; GND if unused.
12	VDD	Power supply input for analog and digital functionalities.
13	RESERVED	Reserved for factory use. This pin shall be connected to GND.
14	VIN2	Power supply input for high−side outputs OUT3 and OUT4.
15	NC	No Connection. Leave floating or connected to GND.
16	OUT4	High−side driver output 4.
17	OUT3	High−side driver output 3.
18	NC	No Connection. Leave floating or connected to GND.
19	OUT2	High−side driver output 2.
20	OUT1	High−side driver output 1.
EPAD	Exposed Pad	Leave floating or connect to GND or to spreader plane for best thermal performance.

Table 3. MAXIMUM RATINGS (Except as noted, voltages are with respect to GND.)

Rating		Symbol	Min	Max	Unit
VINx Pin Voltage AC: ISO 16750−2 § 4.6.4.2.3 Test B, 400 ms @ 25°C		VinxMax	−0.3	40	V
OUTx Pin Voltage	VINx = 0 V	VoutMax0	−0.3	40	V
	VINx > 5 V	VoutMax5	Internally Limited	40	V
VINx Pin to OUTx Pin Differential Voltage	VINx = 0 V	VrevMax0	−40	40	V
	VINx > 5 V	VrevMax5	Internally Limited		V
OUTx Pin Current		IoutMax	−	Internally Limited	A
VDD Pin Voltage		VddMax	−0.3	5.5	V
Logic Pin Voltage (SDA, SCL, EN, ADD, $\overline{\text{FAULT}}$)		VlogicMax	−0.3	5.5	V
Analog Pin Voltage (CL, CS)		VcxMax	−0.3	5.5	V
Logic Pin Current (SCL, EN, ADD, $\overline{\text{FAULT}}$)		IlogicMax	−10.0	2.0	mA
Logic Pin Current (SDA)		IioMax	−10.0	20	mA
Analog Pin Output Current (CL, CS)		IclMax	−10.0	2	mA
IcsMax: t ≤ Tlatch0		IcsMax	−10.0	12	mA
Operating Junction Temperature Range		Tj	−40	150	°C
Storage Temperature Range		Tstr	−55	150	°C
Peak Reflow Soldering Temperature: Pb−free 60 to 150 seconds at 217°C (Note 1)		−	−	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. See or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 4. ATTRIBUTES

Characteristic		Symbol	Value	Unit
Short Circuit Reliability Characterization per AEC − Q100−012		AECQ10x	Grade A	−
ESD Capability				
Human Body Model per AEC−Q100−002	VINx, OUTx	Vesd4k	≥ ±4.0	kV
	All Other Pins	Vesd2k	≥ ±2.0	kV
Charged Device Model per AEC−Q100−011		Vesd750	≥ ±750	V
Moisture Sensitivity Level		MSL	MSL1	−
Thermal Characterization Parameters				°C/W
Junction−to−Ambient	(Note 2)	$R_{\theta JA}$	22.3	
Junction−to−Board	(Note 2)	$R\psi_{JB-EPAD}$	2.2	

2. Based on a 4−layer, 1.6 mm thick PCB with 35 μm copper per layer using 9 thermal vias in exposed pad to internal layer 2 and to external layer 4 planes. Simulated for 0.4 W and 0.68 W per channel cases of simultaneous power dissipation.

Table 5. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	VINxOp	4.5	28	V
Digital Supply Input Voltage	VDDOp	3.15	5.25	V
Logic Low Input Level	VinI	–	0.8	V
Logic High Input Level	Vinh	2.0	–	V
Address Confirmation Time (EN L→H, Note 4, Note 6)	TADDconf	350	–	μs
Enable Release Time (EN H→L, Note 4, Note 7)	tENhl	–	250	μs
I2C SCL Frequency	SCLfreq	–	1.0	MHz
DC Output Current (Single Channel On, T_J < 150°C, Note 2)	IxOp	–	1.2	A
DC Output Current (All Channels On, $T_A \le 125°C$, Note 2)	IxOp125	–	529	mA
DC Output Current (All Channels On, $T_A \le 105°C$, Note 2)	IxOp105	–	710	mA
DC Output Current (All Channels On, $T_A \le 85°C$, Note 2)	IxOp85	–	854	mA
Operating Temperature	TaOp	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS
(−40°C ≤ T_J ≤ 150°C, 5 V ≤ VINx ≤ 18 V, 3.15 V ≤ V_{DD} ≤ 5.25 V, EN = V_{DD}, unless otherwise specified.) (Note 3)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
VDD Sleep Current	IqVDD	VDD = 5 V, EN = 0 V −40°C ≤ T_A < 125°C $T_A \ge 125°C$	- –	3.0 –	4.0 5.0	μA
VDD Active Current	IVDD	−40°C ≤ T_A ≤ 125°C VDD = EN = 5 V, RCL = 2.5 kΩ VIN1 = VIN2 = 13.2 V All Outputs On, I(OUTx) = 0	–	2.6	4.0	mA
VDD Power−on Reset Threshold	VDDpor_i	VDD Increasing	2.4	2.70	3.0	V
	VDDpor_d	VDD Decreasing	2.2	2.5	2.8	V
VDD Power−on Reset Hysteresis	VDDhys		50	–	–	mV
VINx Sleep Current	IqVINx125	VDD = EN = 0 V VIN1 = VIN2 = 13.2 V OUT1 = OUT2 = OUT3 = OUT4 = 0 V	–	1.0	5.0	μA
VINx Active Current	IqVINx_sb	EN = VDD, VIN1 = VIN2 = 18 V OUT1 = OUT2 = OUT3 = OUT4 = 0 V RCL = 2.5 kΩ, All Outputs Off	–	0.6	1.5	mA
VINx Undervoltage Threshold	VINxUV	VINx Decreasing	2.9	3.5	3.9	V
		VINx Increasing	3.1	3.7	4.1	
VINx Undervoltage Hysteresis	VINxUVHys		0.100	0.200	0.350	V
VINx Overvoltage Threshold	VINxOV	VINx Increasing	17.5	19.5	21.5	V
		VINx Decreasing	16.2	18	19.8	
VINx Overvoltage Hysteresis	VINxOVHys		0.5	1.5	2.5	V
DRIVER OUTPUT						
Output On−State Resistance	RDSonHS	VINx = 13.2 V, IOUT = 500 mA	–	0.5	1.0	Ω
Output Leakage Current	IoutLkg13.2	VINx = 13.2 V, OUTx = 0 V −40°C ≤ T_A ≤ 125°C T_A > 125°C	- –	– –	1.0 5.0	μA

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Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
DRIVER OUTPUT						
Reverse Blocking Leakage Current	IoutLkgRvs13.2	VINx = 0 V, OUTx = 13.2 V −40°C ≤ T_A ≤ 125°C T_A > 125°C	- –	– –	1.0 5.0	μA
Reverse Blocking Comparator Threshold	V_STB	VINx = 5 V, VOUTx − VINx, OUTx rising	90	300	1000	mV
		VINx = 5 V, OUTx falling	–	−500	–	mV
Reverse Blocking Deglitch Time	Tblnk	Delay from OUTx activation to enable short to battery detection	8.0	10.0	12.0	μs
	Tfltr1	OUTx crossing rising threshold to output deactivation	1.0	2.0	3.0	μs
	Tfltr2	OUTx crossing falling threshold to output reactivation	8.0	10.0	12.0	μs
VINx to OUTx Clamp	VCL_P	IL = 20 mA, VINx = 36 V VCL_P = ΔV = VINx − OUTx	42	46	54	ΔV
OUTx to GND Clamp	VCL_N	IL = 20 mA, VINx = 13.2 V	−25	−20	−16	V
DRIVER OUTPUT SWITCHING CHARACTERISTICS (Figure 4, RCL = 2.5 kΩ)						
Turn On Delay Time	Tdon	VINx = 13.5 V, R_L = 50 Ω	15	20	35	μs
Turn Off Delay Time	Tdoff	VINx = 13.5 V, R_L = 50 Ω	10	20	30	μs
Rise Time	Trise	VINx = 13.5 V, R_L = 50 Ω	20	40	60	μs
Fall Time	Tfall	VINx = 13.5 V, R_L = 50 Ω	30	50	70	μs
CURRENT SENSE AND CURRENT LIMIT						
Current Sense Ratio	K0	25 mA ≤ IOUT < 50 mA	−25%	200	+25%	–
Current Sense Ratio	K1	50 mA ≤ IOUT < 100 mA	−12%	200	+12%	–
Current Sense Ratio	K2	100 mA ≤ IOUT < 200 mA	−8%	200	+8%	–
Current Sense Ratio	K3	200 mA ≤ IOUT < 400 mA	−7%	200	+7%	–
Current Sense Ratio	K4	IOUT ≥ 400 mA	−6%	200	+6%	–
Current Limit Shutdown Time	Tlatch0	LATCH = 0	18	20	22	ms
	Tlatch1	LATCH = 1	18	20	22	μs
Current Limit Ratio (Note 4)	CLR		–	5000	–	–
Internal Voltage Reference	Vref		0.540	0.600	0.660	V
Current Limit Accuracy (Note 5)	CLacc1	R_{CL} = 30 kΩ	85	107	130	mA
	CLacc2	R_{CL} = 7.5 kΩ	368	400	432	mA
	CLaccExt	R_{CL} = 2.5 kΩ	1040	1155	1270	mA
Current Limit Shift (Note 4) R_{CL} = 7.5 kΩ	CLshift0	CL_SHIFT_x[1:0] = 0b00	–	0	–	%
	CLshift1	CL_SHIFT_x[1:0] = 0b01	–	30	–	%
	CLshift2	CL_SHIFT_x[1:0] = 0b02	–	60	–	%
	CLshift3	CL_SHIFT_x[1:0] = 0b03	–	100	–	%
THERMAL PROTECTION (Note 4)						
Thermal Warning	Twr		120	140	170	°C
Thermal Warning Hysteresis	TwHy		–	20	–	°C
Thermal Shutdown	Tsd		150	175	200	°C
Thermal Shutdown Hysteresis	TsdHy		–	20	–	°C

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(−40°C ≤ T_J ≤ 150°C, 5 V ≤ VINx ≤ 18 V, 3.15 V ≤ V_{DD} ≤ 5.25 V, EN = V_{DD}, unless otherwise specified.) (Note 3)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
OPEN LOAD DETECTION						
Off−state Open Load Detection Threshold	Vol	Diagnostic enabled, EN_OUTx = 0	3	3.3	3.6	V
Off−state Open Load Source Current	Iol_off	Diagnostic enabled, EN_OUTx = 0	25	50	100	μA
Off−state Open Load Detection Delay	Td_ol_off	OUTx = Vol, OL = 0 → 1	8	10	12	μs
I2C: SDA, SCL (Figures 5, 6)						
Clock High Time	Thigh		260	–	–	ns
Clock Low Time	Tlow		500	–	–	ns
Data Setup Time	Tset		50	–	–	ns
Bus Idle Time	Tbuf	Time between a STOP and a next START condition	500	–	–	ns
Input Threshold High	Vih_I2C	SCL, SDA increasing	1.0	1.2	1.4	V
Input Threshold Hysteresis	Vi_I2Chys	SCL, SDA	0.100	0.200	0.300	V
SDA Output Low Voltage	VolSDA	SDA active, I(SDA) = 20 mA	–	–	0.4	V
PIN CHARACTERISTICS						
Enable Input Pull−down Resistance	Rpdx	EN = VDD	50	120	190	kΩ
Enable Input Threshold	VthIn	EN increasing	1.1	1.4	1.9	V
Enable Input Hysteresis	VhysIn	EN	0.100	0.265	0.600	V
$\overline{\text{FAULT}}$ Low Voltage	FLTBv	$\overline{\text{FAULT}}$ active, I($\overline{\text{FAULT}}$) = 2 mA	–	–	0.4	V
$\overline{\text{FAULT}}$ Leakage Current	FLTBi	V($\overline{\text{FAULT}}$) = VDD	–	–	5	μA
INTERNAL ADC						
ADC Resolution	ADCres		–	8	–	bits
ADC Reference Voltage	ADCref		0.95	1.00	1.05	V
Integral Non−linearity (INL)	ADCinl	(Notes 4, 8)	−1.5	–	+1.5	LSB
Differential Non−linearity (DNL)	ADCdnl	(Notes 4, 8)	−1.5	–	+1.5	LSB
Offset Error	ADCoff	(Notes 4, 8)	−3	–	+3	LSB
Gain Error	ADCgain	(Notes 4, 8)	−2	–	+2	%
Conversion Time	ADCtconv	(Note 4, Figure 21)	–	12	–	μs
Initial Acquisition Delay	ADCblnk	EN_OUTx 0→1 (Note 4, Figure 21)	–	200	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Min/Max values are guaranteed by design, test, or statistical correlation, and are valid for the stated temperature range unless otherwise noted.
4. No production test.
5. Current limit accuracy is valid for saturation mode operation (short to ground and inrush/charging events).
6. The time required after EN L→H for the device to wake−up and confirm an I2C address selection (as per external resistor RADD) after which the device is ready for I2C communication.
7. The time required after EN H→L for the device to enter into sleep mode.
8. Measured as a deviation of the actual ADC transfer function from a best fit straight−line interpolation between 5% and 95% of the CS input Full−Scale Voltage, FSV = ADCref x ($1 - 2^{-ADCres}$).

Characteristic Timing Diagrams

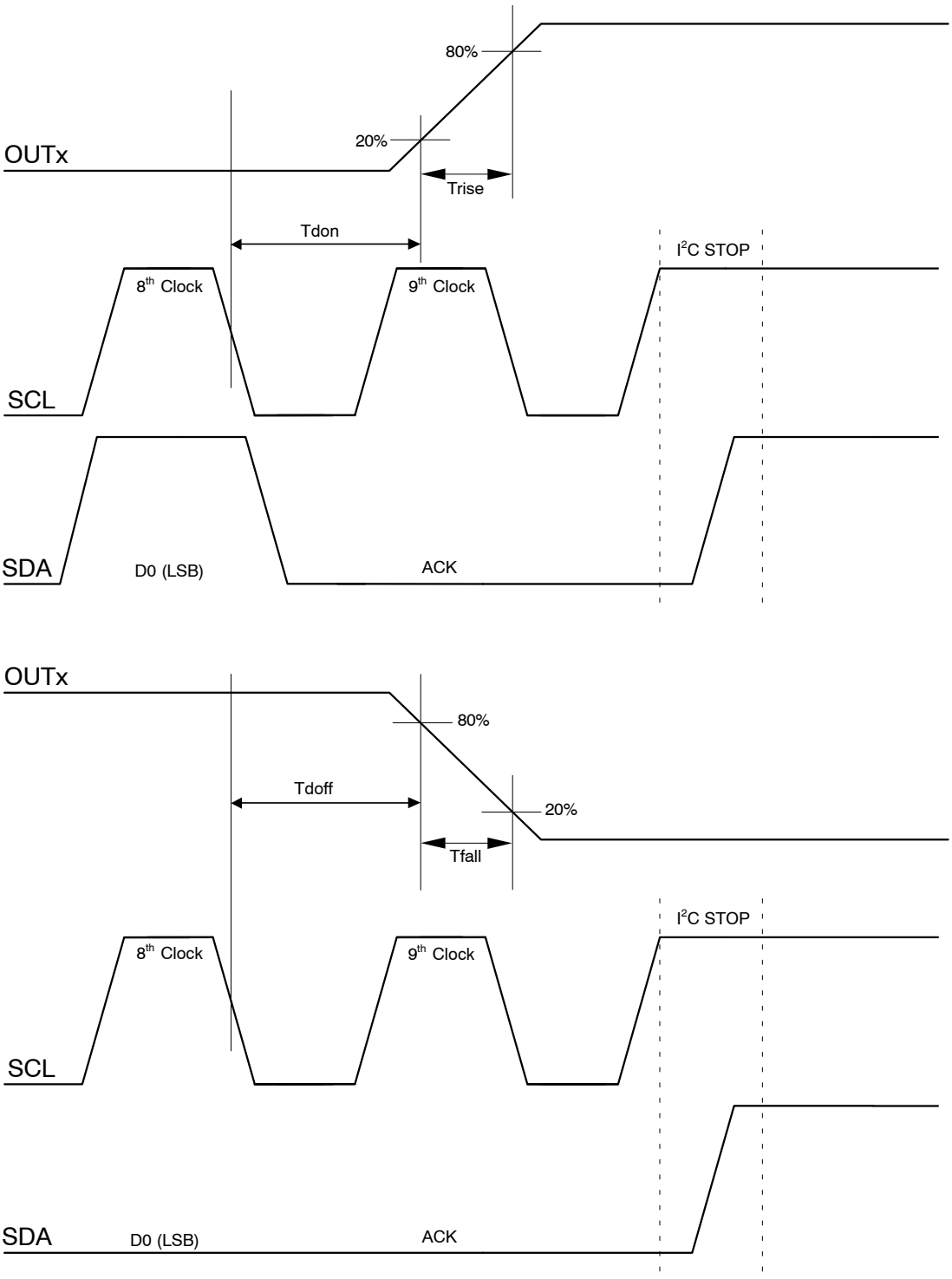


Figure 4. Detailed Driver Timing

Characteristic Timing Diagrams

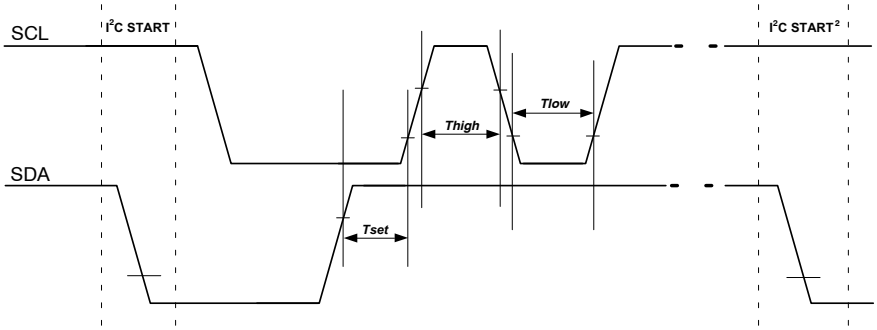


Figure 5. I²C Timing

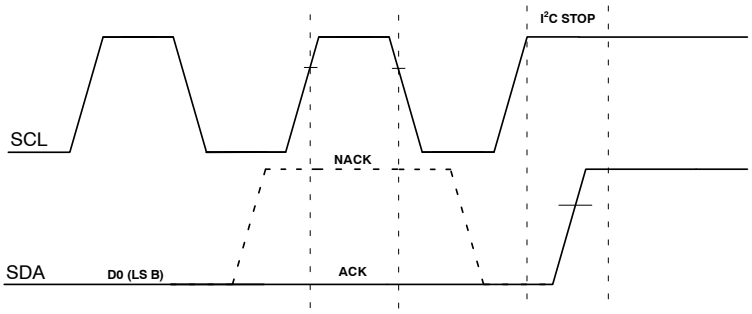


Figure 6. ACK/NACK + I²C STOP

Detailed Operating Description

General Overview

The NCV760040 is an I²C−enabled target device featuring four independent high−side outputs constructed using two back−to−back NMOS power transistors for true reverse current blocking capability. Each output is protected against short to battery, short to ground, and overtemperature faults. An off−state open load diagnostic supports system−level fault detection.

The product features a low quiescent current sleep mode under control of the device's EN pin. The device transitions from sleep mode to active mode when EN changes from low to high, allowing device configuration and control of the outputs via I²C interface. The device transitions from active mode to sleep mode when EN changes from high to low, disabling the outputs and resetting all device registers to their default state.

The four outputs are grouped in pairs and powered via one of two independent supply inputs VIN1 and VIN2 (Figure 2). These can be directly connected to a conditioned battery voltage bus or to a lower bus voltage (Figure 1) such as may be supplied via a DC−DC converter within an application. VIN1 and VIN2 are each separately monitored for overvoltage and undervoltage events. During an undervoltage event, the corresponding outputs are disabled. During an overvoltage event, the corresponding outputs normally remain active and can be optionally configured via I²C to be disabled during overvoltage.

Device configuration, output control, and diagnosis is done via the I²C interface at SCL rates up to 1 MHz. Target I²C addresses may be programmed via an external resistor R_{ADD} at the device's ADD pin, allowing up to eight NCV760040 target devices supporting up to 32 high−side outputs. The ADD pin may optionally be left open or connected to ground, providing the target with a defined ninth default 'fail−safe' I²C address, and supports target communication in the event of an open or shorted R_{ADD} resistor.

The product offers adjustable baseline current limit – programmed via an external resistor R_{CL} at the CL pin – as well as current limit shift functionality programmed via the I²C interface. Current limit shift allows for adjustments to the global baseline current limit on a per-channel basis. In the event of an open or shorted R_{CL} resistor, the baseline current limit defaults to defined levels.

An embedded 8−bit ADC converts the voltage at the CS pin – an external signal or a voltage developed via an internal current and an external resistor R_{CS} – for readout through I²C. The conversion range can be adapted to the programmed baseline current limit by adjusting the R_{CS} resistor. In the event of an open or shorted R_{CS} resistor, the ADC conversion range defaults to defined levels.

Conversion of the voltage developed via the R_{CS} resistor may also be done by connecting the CS pin to an external ADC. Conversion of an external signal via the internal ADC may be done by connecting the signal to the CS pin and by configuring the internal ADC accordingly.

An open−drain flag pin provides a means for immediate communication of faults to a host controller. Short to battery, short to ground, overtemperature, and open load fault types from all channels are grouped by type and selectively routed to the flag pin. Control over which fault types are routed to the pin is provided via the fault pin configuration register (Figure 15).

Device I²C Protocol

The NCV760040 is a target device compatible with the I²C−bus protocol, receiving and sending 8−bit transaction sequences via the SDA bus line synchronized to packets of 9 clock pulses on the SCL bus line. The clock pulses and the START and STOP conditions are always generated by a controller device. The NCV760040 does not employ any form of clock stretching. Refer to Figure 7 – Figure 10 for I²C transaction sequence examples.

For every transaction sequence, the first packet sent by the controller to a target begins with a START condition, defined by a high to low transition on SDA while SCL is held high. The final packet sent or received by the controller must be terminated by the controller with a STOP condition, defined by a low to high transition on SDA while SCL is held high.

During a write transaction sequence, the controller must release control of the SDA line after every byte sent to the target to allow the target to acknowledge (ACK) or not−acknowledge (NACK) receipt of the data. During a read transaction sequence, the target must release control of the SDA line after every byte sent to the controller to allow the controller to acknowledge (ACK) or not−acknowledge (NACK) receipt of the byte.

The ACK or NACK signal occurs during a packet's 9th SCL clock pulse. The ACK signal is defined by the target pulling SDA low while SCL is clocked. The NACK signal is defined by SDA remaining high while SCL is clocked. See the Figure 5 diagram for I²C and START timing and the Figure 6 diagram for ACK, NACK, and STOP timing.

The NCV760040 only accepts 8−bit data transactions that conform to the examples of Figure 7 – Figure 10 and have:

- 9 clock pulses per packet −and−
- a 1st packet containing a defined 7−bit target address with R/W = 0 −and−
- a 2nd packet containing a defined 8−bit register address.

If at any point within a transaction the controller's packet sequences do not conform to the target NCV760040's defined protocol, the target will ignore (NACK) the transaction, and the controller must abort the transaction and repeat it, if desired, by sending either:

- a STOP condition −or−

- a repeated START condition to begin a new transaction.

The defined target addresses are given in Table 7 and the defined register addresses are given in Table 8.

Target Device Address

Target I^2C addresses may be programmed via an external resistor R_{ADD} at the device's ADD pin, allowing up to eight NCV760040 target devices per standard 128−address I^2C bus. The ADD pin may optionally be left open or connected to ground, providing the target with a defined ninth default 'fail−safe' I^2C address, and supports target communication in the event of an open or shorted R_{ADD} resistor. A 1% initial tolerance resistor with 3% end−of−life tolerance or better is recommended for R_{ADD}.

The defined address assignments and corresponding R_{ADD} resistor values are summarized in Table 7. The general call address '0x00' is not supported. If a controller issues a general call address packet, the NCV760040 will ignore (NACK) the transaction.

Table 7. TARGET DEVICE I^2C ADDRESS ENUMERATION

Target Device I^2C Address	I^2C Address Hex Value	ADD Pin R_{ADD} Resistor Value*
Target Address 0	0x60	536 Ω
Target Address 1	0x61	1.24 kΩ
Target Address 2	0x62	2.80 kΩ
Target Address 3	0x63	5.62 kΩ
Target Address 4	0x64	11.5 kΩ
Target Address 5	0x65	27.4 kΩ
Target Address 6	0x66	59.0 kΩ
Target Address 7	0x67	133.0 kΩ
Target Address 8 (Fail−safe address)	0x68	ADD pin opened or shorted to ground

*A 1/8 W 1% initial tolerance resistor with 3% end−of−life tolerance or better, and with a 100 ppm/°C tempco or better is recommended.

The programmed target address is automatically enumerated upon transition from the sleep mode to the active mode via the EN pin, or upon power−on reset via the device's internal VDD monitor when EN is connected to VDD. Enumeration is completed and the target is ready for communication after the address acquisition time TADDconf. Except when grounding the pin, capacitive loading of the ADD pin can result in enumeration of an address different from that expected per the chosen R_{ADD} value.

I^2C Transactions

Several examples of I^2C transaction sequences conforming to the target NCV760040's defined protocol are provided in the following descriptions and figures.

Single−byte Write Sequence: (Figure 7) A START condition is sent, followed by a 7−bit target device address (Table 7) with the R/W bit = 0 to select write mode. Next, send the 8−bit register address (Table 8) to write to, followed by the data to write. Once the data have been written, the controller must send a NACK by pulling SDA high while SCL is clocked. A STOP sequence must then follow from the controller to end the transaction.

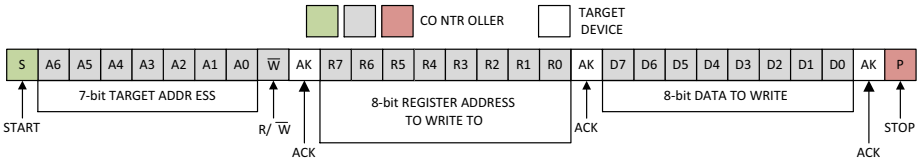


Figure 7. Write Transaction – Single−byte Sequence

Single−byte Read Sequence: (Figure 8) A first START condition is sent, followed by a 7−bit target device address with the R/W bit = 0 to select write mode. Next, send the 8−bit register address to read from. Then a second START condition is sent, followed by the same 7−bit target device address with the R/W bit = 1 to select read mode. The controller must now release control of the SDA line to receive the 8−bit data from the target NCV760040. After the data have been read, the controller must send a NACK by pulling SDA high while SCL is clocked. A STOP sequence must then follow from the controller to end the transaction.

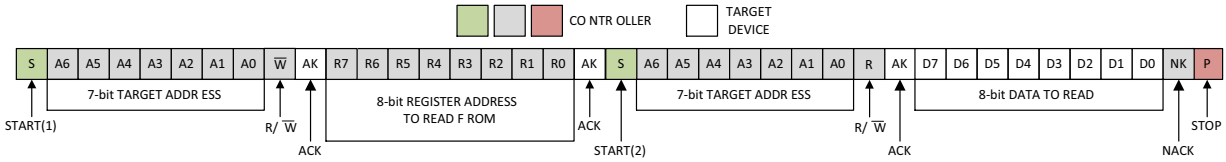


Figure 8. Read Transaction – Single−byte Sequence

Multi−byte Write Sequence: (Figure 9) A multi−byte write sequence is initially the same as a single−byte sequence, but following the first data byte sent, the controller does not send a STOP condition after receipt of the target's ACK signal. The controller instead continues to write target address and data byte pairs to the same target address – to the same or to another data register address – then sends a STOP condition after the target acknowledges receipt of the final byte pair sent.

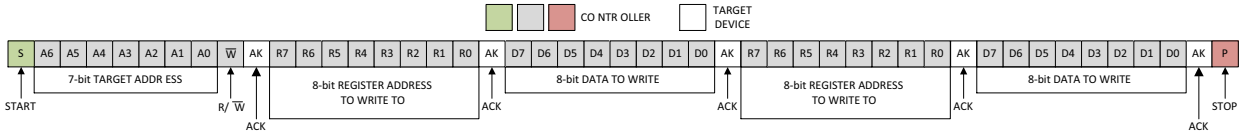


Figure 9. Write Transaction – Multi−byte Sequence

Multi−byte Read Sequence: (Figure 10) A multi−byte read sequence is initially the same as a single−byte sequence, but following the first data byte received from the target's register address 'N', the controller does not send a NACK signal. The controller instead sends an ACK signal and continues to receive and acknowledge additional data bytes from the same target address, and the target increments its register address to 'N+1'.

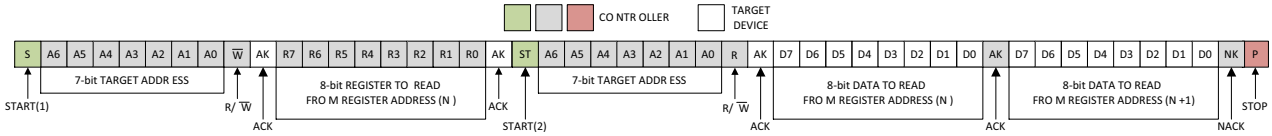


Figure 10. Read Transaction – Multi−byte Sequence

The initial register address 'N' can be any of the target's valid register addresses. Once the target's last register address has been read, the target will automatically loop back to the lowest register address and will continue to send data as long ACK signals continue to be received from the controller. The controller indicates its final read request from the target by sending a NACK signal followed by a STOP condition.

Register Structure

Target device control and configuration commands, device status data, ADC data, and fault diagnostic data are accessed via the twelve defined device register addresses as summarized in Table 8.

Table 8. DEVICE REGISTER SUMMARY

Function	Type	Alias	Address	Description
OUTPUT CONTROL	Read/Write	R0	0x11	Per−channel output enable/disable.
CONFIGURATION	Read/Write	R1	0x12	Per−channel ILIM latch−off time select; global OVLO enable/ disable; current sense ADC channel selection.
CURRENT LIMIT SHIFT	Read/Write	R2	0xA1	Per−channel ILIM shift selection.
CONFIGURATION 2	Read/Write	R3	0xA2	Global clear−on−read (COR) mode enable/disable; off−state open load diagnostic enable/disable.
ADC READOUT	Read Only	R4	0x21	Global ADC conversion data corresponding to the selected input source.
DIAGNOSTICS OUT1	Read/Clear	R5	0x31	Per−channel status and diagnostic data − output enabled/disabled; current limit (ILIM), thermal warning, and thermal shutdown status (TSD); short to battery (STB) and open load (OL) diagnostics.
DIAGNOSTICS OUT2	Read/Clear	R6	0x41	
DIAGNOSTICS OUT3	Read/Clear	R7	0x51	
DIAGNOSTICS OUT4	Read/Clear	R8	0x61	
GLOBAL DIAGNOSTICS	Mixed Read Only Read/Clear	R9	0x71	Global fault status (STB/OL/ILIM/TSD − any channel); VIN1 and VIN2 undervoltage (UV) /overvoltage (OV) status.
$\overline{\text{FAULT}}$ PIN CONFIGURATION	Read/Write	R10	0x81	Map selected status data to the $\overline{\text{FAULT}}$ pin: global VINx UV/OV; STB/OL/ILIM/TSD − any channel.
DEVICE ID	Read Only	R11	0x82	Hard−coded 3−bit device identification string.

R0 OUTPUT CONTROL Register

R0 − OUTPUT CONTROL (Read/Write)

Address: 0x11							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RB_BLK4	RB_BLK3	RB_BLK2	RB_BLK1	EN_OUT4	EN_OUT3	EN_OUT2	EN_OUT1

Mnemonic	Functional Description
RB_BLKx	Corresponding OUTx short to battery (STB) reverse blocking deglitch: 0 = blanking timer enabled (default) 1 = blanking timer disabled
EN_OUTx	Corresponding OUTx control: 0 = OUTx disabled (default) 1 = OUTx enabled

The 0x11.OUTPUT CONTROL register provides read/write access for configuration of the short to battery blanking timer via register bits D[7:4] and for control of the OUTx drivers via register bits D[3:0]. Selection of the several configuration options is done by writing to the corresponding register bits. Confirmation of the written configuration is returned by reading the same register bits. Default after VDD POR or WAKE: 0x11.D[7:0] = 0x00. Refer to § Short to Battery Protection for additional details about the STB functionality.

Using OUT1 as a focus example, Figure 11 shows the simplified register and output control topology. Basic control of the outputs is done by writing to the 0x11.EN_OUTx bits. Real−time status of the outputs is returned by reading the STATUS bit in the 0x31 DIAGNOSTICS OUTx register. If for example activation of OUT1 is desired, writing ‘1’ to the EN_OUT1 bit will enable activation of OUT1. If there are no fault conditions present, the output will turn on and its status can be confirmed by reading ‘1’ via the 0x31 STATUS bit.

The device’s fault protection and recovery, and its fault reporting and clearing functionalities work together with behaviors that are dependent upon the specific fault type. Further details about the embedded protections and their fault handling and status reporting behaviors are provided in the succeeding sections of this datasheet. A summary of the protections and behaviors is provided in Table 12.

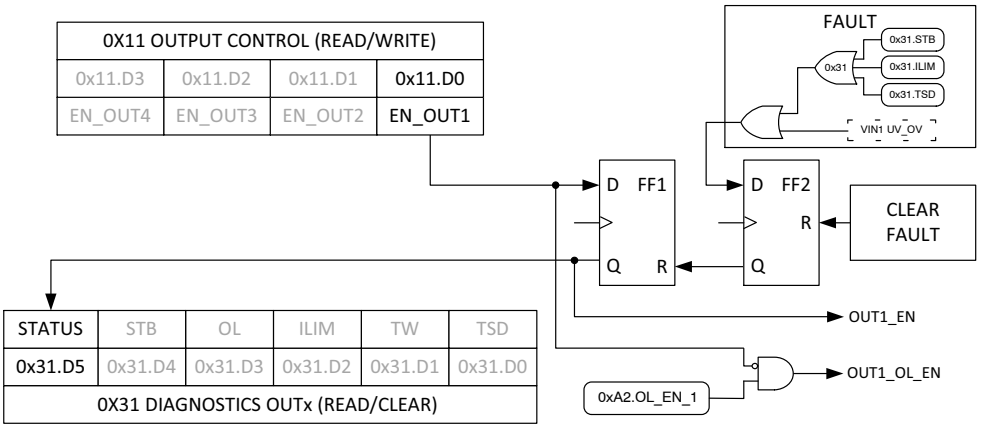


Figure 11. Output Control Overview (OUT1 focus)

R1 Configuration Register

R1 CONFIGURATION REGISTER (Read/Write)

Address: 0x12							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LATCH_1	LATCH_2	LATCH_3	LATCH_4	OVLO	SENSE_SELECT[2:0]		

Mnemonic	Functional Description
LATCH_X	Per−channel ILIM timer for corresponding OUTx: 0 = OUTx latches off after time *Tlatch0* (default) 1 = OUTx latches off after time *Tlatch1*
OVLO	Global VIN1 and VIN2 overvoltage lockout control: 0 = corresponding OUTx remain on during overvoltage (default) 1 = corresponding OUTx are disabled during overvoltage
SENSE_SELECT[2:0]	Channel selection for output current sensing via the internal ADC: 0b000 = current sense functionality and ADC disabled (default) 0b001 = ADC enabled; input is OUT1 sense current 0b010 = ADC enabled; input is OUT2 sense current 0b011 = ADC enabled; input is OUT3 sense current 0b100 = ADC enabled; input is OUT4 sense current 0b111 = ADC enabled; input is external signal at CS pin All other 3−bit combinations reserved.

The 0x12. CONFIGURATION register provides read/write access for per−channel configuration of the ILIM protection delay via register bits D[7:4], for configuration of the global overvoltage lockout control via bit D[3], and for configuration of the current sense and ADC functional blocks via bits D[2:0]. Selection of the several configuration options is done by writing to the corresponding register bits. Confirmation of the written configuration is returned by reading the same register bits. Default after VDD POR or WAKE: 0x12.D[7:0] = 0x00.

Upon detection of an overcurrent condition, the ILIM protection function latches off the affected output after expiration of a delay time *Tlatch0* (20 ms typ.) or *Tlatch1* (20 μs typ.) as selected via the 0x12.LATCH_X bits. The per−channel delay times can be configured along with the 0xA1.CL_SHIFT_X bits to help accommodate transient inrush/charging events such as when driving an incandescent lamp load, a large capacitor load, or a motor load's initial start−up/stall torque. Refer to § Current Limit and Current Limit Shift for details about the ILIM functionality.

Each of VIN1 and VIN2 is monitored for undervoltage and overvoltage conditions. Upon detection of a VINx undervoltage condition, the corresponding OUTx drivers are always disabled. Upon detection of a VINx overvoltage condition, the corresponding OUTx drivers are enabled or disabled according to the 0x12.OVLO bit. Refer to § VINx Voltage Monitoring for details about the OVLO functionality.

Current sense ('front−end') and ADC ('back−end') functional blocks (see Figure 18) are embedded to provide a readout of a channel's sensed output current (as a voltage developed via an external resistor) at the CS pin, or to provide a readout an external voltage applied directly to the CS pin. The 0x12. SENSE_SELECT bits are provided to select which front−end input signal (internal or external) will be routed to the ADC back−end, or to disable the embedded current sense and ADC blocks for reduced power consumption. Refer to § Current Sense and ADC for details about the ADC functionality.

R2 CURRENT LIMIT SHIFT Register

R2 – CURRENT LIMIT SHIFT (Read/Write)

Address: 0xA1							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CL_SHIFT_4[1:0]		CL_SHIFT_3[1:0]		CL_SHIFT_2[1:0]		CL_SHIFT_1[1:0]	

Mnemonic	Functional Description
CL_SHIFT_X[1:0]	Increase the baseline current limit on OUTx by the selected percentage: 0b00 = +0% (default) 0b01 = +30% 0b10 = +60% 0b11 = +100%

The 0xA1 CURRENT LIMIT SHIFT register provides read/write access for per−channel modification of the ILIM protection baseline current limit as set via an external resistor R_{CL}. Selection of the several configuration options is done by writing to the corresponding register bits. Confirmation of the written configuration is returned by reading the same register bits. Default after VDD POR or WAKE: 0xA1.D[7:0] = 0x00.

The per−channel shift level multiplies the baseline current limit according to the corresponding 0xA1.CL_SHIFT_X bits. The shift level can be configured along with the 0x12.LATCH_X bits to help accommodate transient inrush/charging events such as when driving an incandescent lamp load, a large capacitor load, or a motor load's initial start−up/stall torque.

A 'failsafe' limit functionality is embedded for the case of 1.) open/missing/out−of−range−high or 2.) shorted/short−to−GND/out−of−range−low R_{CL} resistor which bounds/defaults the current limit in the 'open' case to 100 mA nominal and in the 'short' case to 1.2 A nominal. The "current limit shift" multiplier functionality is disabled when either `open' or 'short' condition is detected.

For proper operation and parametric quality, the current limit shift functionality requires resistor R_{CL} to be in the range 2.5 kΩ ≤ R_{CL} ≤ 30 kΩ. Refer to § Current Limit and Current Limit Shift for details about the ILIM and CL_SHIFT functionalities.

R3 CONFIGURATION 2 Register

R3 – CONFIGURATION 2 (Read/Write)

Address: 0xA2							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
COR	–	–	–	–	OL_EN_X[2:0]		

Mnemonic	Functional Description
COR	Global Clear−On−Read (COR) mode for specific non−latched fault types (see also Table 12 summary): 0 = fault status bit(s) updated continuously (default) 1 = fault status bit(s) cleared after reading corresponding register
OL_EN_X[2:0]	Off−state open load diagnostic (current and detection) control: 0b000 = diagnostic disabled for all channels (default) 0b001 = OUT1 diagnostic enabled 0b010 = OUT2 diagnostic enabled 0b011 = OUT3 diagnostic enabled 0b100 = OUT4 diagnostic enabled All other 3−bit combinations reserved.

The 0xA2 CONFIGURATION 2 register provides read/write access for modification of the global Clear−On−Read (COR) functionality and for the off−state open load diagnostic functionality. Selection of the several configuration options is done by writing to the corresponding register bits. Confirmation of the written configuration is returned by reading the same register bits. Default after VDD POR or WAKE: 0xA2.D[7:0] = 0x00.

Non−latched driver output fault types – short to battery (STB), open load (OL), and thermal warning (TW) – and non−latched global VINx fault types undervoltage (UV) and overvoltage (OV) – are those that may temporarily disable the affected outputs while a fault is preset then re−enable it automatically when the fault resolves.

Real−time status of the driver output faults and of the global UV/OV faults is returned by respectively reading the

0x31−0x61.DIAGNOSTICS OUTx status bits and the 0x71.GLOBAL DIAGNOSTICS status bits. By default, these status bits are also non−latched and so a transient fault – which may cause momentary interruption of an output – can lead to a situation where the fault resolves and no status information about the fault is captured.

The COR bit can be used to modify the specific non−latched fault types so that their status information is latched into the DIAGNOSTICS OUTx and GLOBAL DIAGNOSTICS and is available during and after resolution of a non−latched fault type. Note that when enabled, the COR functionality affects all non−latched diagnostic bits. Refer to § Diagnostic Register Clearing for additional details about the COR functionality.

An embedded off−state open load (OL) diagnostic – using a single current source and a single comparator detection block – is implemented along with a multiplexer. The 0xA2 OL_EN_X bits are provided to select which one of the four OUTx is to be routed to the detection block. Refer to § Off−state Open Load for additional details about the OL diagnostic functionality.

R4 ADC READOUT Register

R4 – ADC READOUT (Read Only)

Address: 0x21							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SENSE[7:0]							

Mnemonic	Functional Description
SENSE[7:0]	Global 8−bit ADC conversion data corresponding to the input source selected via the register 0x12.SENSE_SELECT bits. (default: 0x21.D[7:0]= 0x00)

The 0x21 ADC READOUT register provides read−only access for retrieving conversion data from the embedded 8−bit ADC. The returned data represents the last conversion of the sampled ADC input source value as selected via the register 0x12.SENSE_SELECT bits. Default after VDD POR or WAKE: 0x21.D[7:0] = 0x00. Refer to § Current Sense and ADC for details about the ADC functionality.

R5 – R8 – DIAGNOSTICS OUTx Register

R5 – R8 – DIAGNOSTICS OUTx (Mixed Types: Read Only, Read/Clear)

R5 – OUT1 Address: 0x31 R6 – OUT2 Address: 0x41 R7 – OUT3 Address: 0x51 R8 – OUT4 Address: 0x61							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	STATUS	STB	OL	ILIM	TW	TSD

Mnemonic	Type	Functional Description
STATUS	Read Only	State of corresponding output: 0 = OUTx disabled (default) 1 = OUTx enabled
STB	Read/Clear	State of corresponding OUTx Short To Battery (STB) condition: 0 = STB condition not detected (default) 1 = STB condition detected
OL	Read/Clear	State of corresponding OUTx Open Load (OL) condition: 0 = OL condition not detected (default) 1 = OL condition detected
ILIM	Read/Clear	State of corresponding OUTx current vs. current limit (ILIM) condition: 0 = OUTx current < current limit (default) 1 = OUTx current > current limit
TW	Read/Clear	State of corresponding OUTx Thermal Warning (TW) condition: 0 = TW condition not detected (default) 1 = TW condition detected
TSD	Read/Clear	State of corresponding OUTx Thermal Shut Down (TSD) condition: 0 = TSD condition not detected (default) 1 = TSD condition detected

The 0x31 – 0x61 DIAGNOSTICS OUTx registers provide read only and read/clear access for retrieving output status and fault diagnostic status for each of the four driver channels. The real−time output STATUS bit indicates whether the corresponding OUTx driver is enabled or disabled. The fault status bits are either latched or non−latched types and indicate whether a driver fault has been detected. Default after VDD POR or WAKE: 0x31 – 0x61.D[7:0] = 0x00.

Figure 12 hows the basic register structure and output control topology. Latched driver output fault types – current limit (ILIM) and thermal shutdown (TSD) – are those that disable and latch the affected outputs off after a delay time (configurable for ILIM via the 0x12.LATCH_X bits) when a fault is detected and latch the event into the register's respective fault status bit. Non−latched driver output fault types – short to battery (STB), open load (OL), and thermal warning (TW) – are those that may temporarily disable the affected outputs while a fault is present then re−enable it automatically when the fault resolves.

Note that the device's global VINx_UV and VINx_OV voltage monitor bits can provide an additional non−latched fault type which – when modified by the overvoltage lockout bit (0x12.OVLO = 1) – can disable the outputs associated with the affected VINx path, and cause the STATUS bit to report `0' during an overvoltage event *without indicating any other condition within the DIAGNOSTICS OUTx register itself*. Refer to § VINx Voltage Monitoring § R1 CONFIGURATION Register and § R9 – GLOBAL DIAGNOSTCS Register for details about the overvoltage monitor functionality.

Non−latched fault bits provide real−time status of the driver output faults and so can be transient in nature, which can lead to a situation where a fault resolves and no status information about the fault is captured. The 0xA2.COR bit can be used to modify the non−latched fault types so that their status information is latched into the fault bits and is available during and after resolution of a non−latched fault type. In any case, merely reading the DIAGNOSTICS OUTx registers does not clear any fault bit states and does not re−enable a faulted driver output. Refer to § Diagnostic Register Clearing for additional details about the read/clear and COR functionalities.

For details about each of the STB, OL, ILIM, TW, and TSD functionalities, refer to their corresponding datasheet sections. For details about fault handling refer to § Device Modes and Fault Handling.

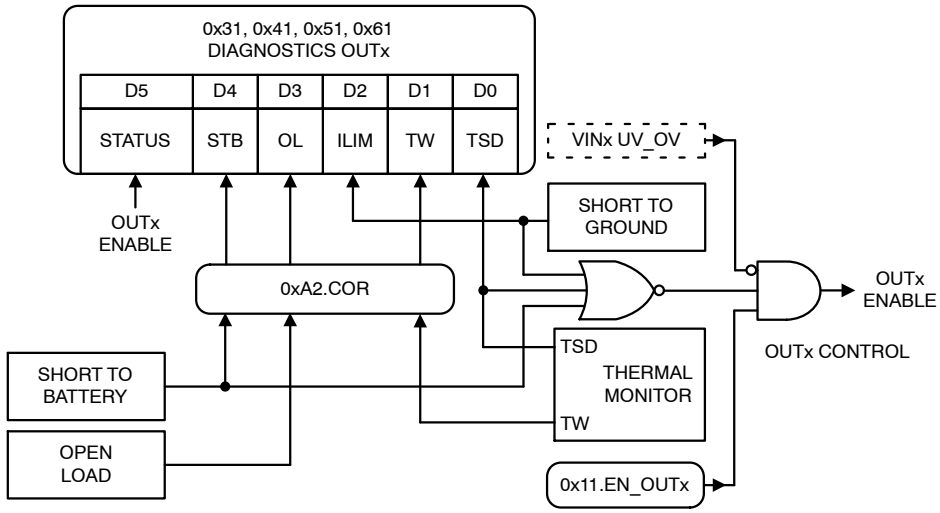


Figure 12. Per−channel Diagnostics Mapping and COR Configuration

R9 – GLOBAL DIAGNOSTICS Register

R9 – GLOBAL DIAGNOSTICS (Mixed Types: Read Only, Read/Clear)

Address: 0x71							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
GL_FAULT	–	–	–	VIN2_UV	VIN2_OV	VIN1_UV	VIN1_OV

Mnemonic	Type	Functional Description
GL_FAULT	Read Only	Driver fault condition detection (STB, OL, ILIM, TSD) 0 = no fault condition(s) detected (default) 1 = fault conditions(s) detected on one or more outputs
VIN2_UV	Read/Clear	VIN2 Undervoltage (UV) condition 0 = UV condition not detected (default) 1 = UV condition detected
VIN2_OV	Read/Clear	VIN2 Overvoltage (OV) condition 0 = OV condition not detected (default) 1 = OV condition detected
VIN1_UV	Read/Clear	VIN1 Undervoltage (UV) condition 0 = UV condition not detected (default) 1 = UV condition detected
VIN1_OV	Read/Clear	VIN1 Overvoltage (OV) condition 0 = OV condition not detected (default) 1 = OV condition detected

The 0x71 GLOBAL DIAGNOSTICS register provides read only and read/clear access for retrieving driver diagnostic status for all four driver channels and for retrieving global VINx undervoltage (UV) and overvoltage (OV) fault types. The global status bits comprise both latched and non−latched types. Default after VDD POR or WAKE: 0x71.D[7:0] = 0x00.

Figures 13 and 14 show the register structures and the basic output control topology. The 0x71. GL_FAULT bit is a ‘read only’ type and provides the combined fault states of all four driver channels. The 0x71.VINx_UV and 0x71.VINx_OV bits are read/clear types and provide fault states for each VINx voltage.

Note that the global VINx_UV and VINx_OV voltage monitor bits can provide an additional non−latched fault type which can disable the outputs associated with the affected VINx path, and cause the DIAGNOSTICS OUTx register STATUS bit to report ‘0’ during an undervoltage event − and optionally an overvoltage event − without indicating any other condition within the DIAGNOSTICS OUTx register itself.

Since OUTx STATUS bits are not mapped to the GLOBAL DIAGNOSTICS register’s GL_FAULT bit, occurrence of a VINx under/over voltage event will only be mapped to the global register’s VINx_UV and VINx_OV bits. Refer to § VINx Voltage Monitoring for details about the undervoltage and overvoltage functionalities.

The persistence of any of the bit states is dependent upon a particular fault’s behavior (transient or steady−state), and a particular fault bit’s reporting behavior (latched or non−latched) – which can be modified by the global Clear On Read (COR) functionality via the 0xA2.COR bit. Refer to § Diagnostic Register Clearing for details about the read/clear and the global COR functionalities.

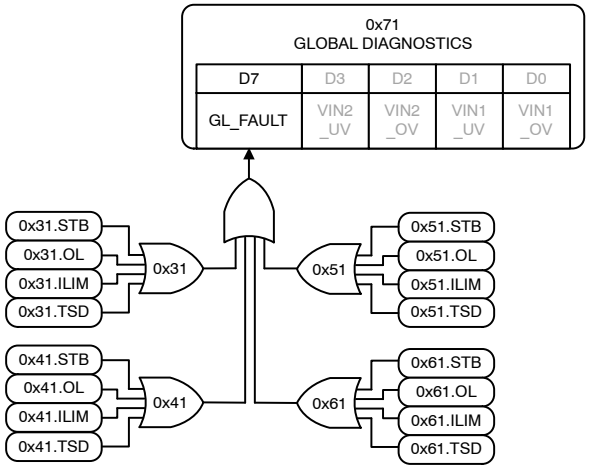


Figure 13. Global Diagnostics: Global Fault Mapping

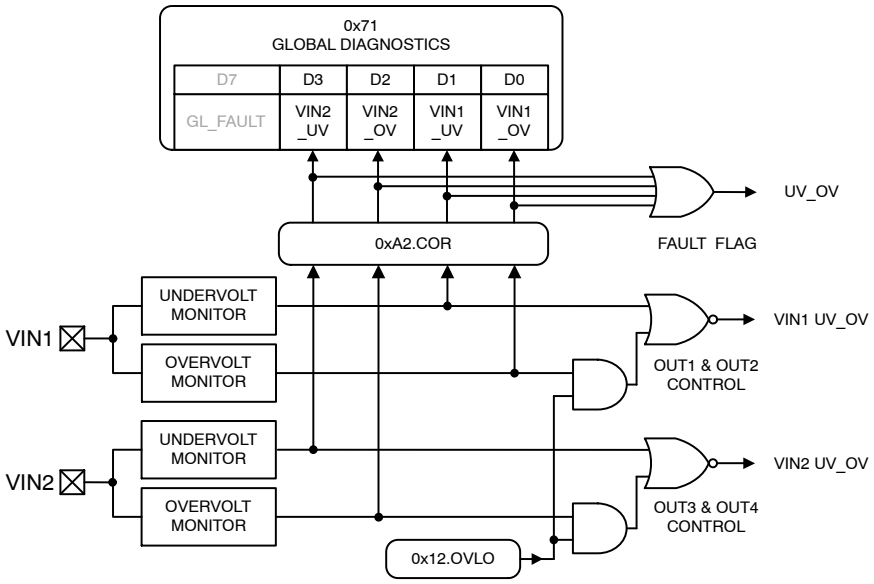


Figure 14. Global Diagnostics: Under/Over Voltage (UV/OV) Mapping and COR Configuration

R10 – FAULT PIN CONFIGURATION Register

R10 – FAULT PIN CONFIGURATION (Read/Write)

Address: 0x81							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	OV_UV	STB_ALL	OL_ALL	ILIM_ALL	TSD_ALL

Mnemonic	Functional Description
OV_UV	Global VIN1 and VIN2 Undervoltage (UV) or Overvoltage (OV) condition: 0 = UV/OV condition blocked from the flag pin (default) 1 = UV/OV condition passed to the flag pin
STB_ALL	Short To Battery (STB) condition for any/all OUTx: 0 = STB condition blocked from the flag pin (default) 1 = STB condition passed to the flag pin
OL_ALL	Open Load (OL) condition for any/all OUTx: 0 = OL condition blocked from the flag pin (default) 1 = OL condition passed to the flag pin
ILIM_ALL	Current limit (ILIM) condition for any/all OUTx: 0 = ILIM condition blocked from the flag pin (default) 1 = ILIM condition passed to the flag pin
TSD_ALL	Thermal Shutdown (TSD) condition for any/all OUTx: 0 = TSD condition blocked from the flag pin (default) 1 = TSD condition passed to the flag pin

The 0x81 FAULT PIN CONFIGURATION register provides read/write access for configuration of the global open−drain fault flag. Selection of the several configuration options is done by writing to the corresponding register bits. Confirmation of the written configuration is returned by reading the same register bits. Default after VDD POR or WAKE: 0x81.D[7:0] = 0x00 (all faults blocked).

The basic fault state−to−flag pin mapping scheme is shown in Figure 15. In contrast to the GLOBAL DIAGNOSTICS register – which combines and maps e.g. *any* driver output fault from *each* channel to the 0x71. GL_FAULT bit (see Figure 13) – the fault pin mapping scheme combines a specific driver fault type from *all* channels, the result of which can be either blocked from or passed to the fault pin via the corresponding (e.g. 'STB_ALL') fault type bit.

Similarly and also in contrast to the GLOBAL DIAGNOSTICS register – which maps the individual global VINx undervoltage (UV) and VINx overvoltage (OV) fault types to the corresponding 0x71.VINx_UV and 0x71.VINx_OV bits (see Figure 14) – the fault pin mapping scheme combines *any* UV or OV fault type from *either* VINx, the result of which can be either blocked from or passed to the fault pin via the single 'OV_UV' fault type bit.

The fault flag can signal a fault condition and provide a quick and comprehensive means for diagnosis of which fault type and condition. By selectively configuring the individual configuration bits to block or pass the several fault types, a general fault type can be identified. Once a general fault type is identified, the specific fault condition can be further diagnosed via the GLOBAL DIAGNOSTICS register and finally via the individual driver DIAGNOSTICS OUTx registers. An example illustrating the mapping and flag pin behavior when configuring for the STB fault type is:

"**IF** (STB = TRUE **AND** (STB_ALL = TRUE, OV_UV = FALSE, OL_ALL = FALSE, ILIM_ALL = FALSE, TSD_ALL = FALSE), **THEN** FLTB = LOW **ELSE** FLTB = Z".

Note that the behaviors of the various diagnostic bits – which originate from the four driver output channels and the global VINx monitors and comprise both latched and non−latched types – will be propagated to the fault flag. The persistence of any of the diagnostic bit states is dependent upon a particular event's behavior (transient or steady−state), and a particular diagnostic bit's reporting behavior (latched or non−latched/'real−time') – which can be modified by the global 0xA2.COR functionality. Refer to § Diagnostic Register Clearing for details about the read/clear and the global COR functionalities. Refer to § VINx Voltage Monitoring for details about the undervoltage and overvoltage functionalities.

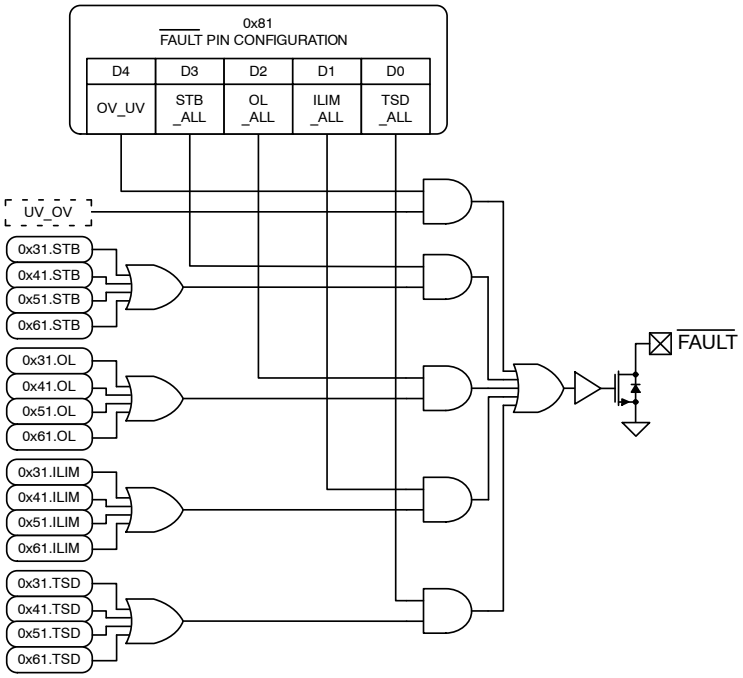


Figure 15. Fault Pin Configuration

R11 – DEVICE ID Register

R11 – DEVICE ID (Read Only)

Address: 0x82							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
–	–	–	–	–	ID[2:0]		

Mnemonic	Functional Description
ID[2:0]	Hard−coded device identifier string: 0b**010** = NCV760040 All other 3−bit combinations reserved

The 0x82 DEVICE ID register provides read−only access for retrieving the target device's hard−coded identifier string. Default after VDD POR or WAKE: 0x82.D[7:0] = specific device ID code.

In addition to providing a means for the target device identification, the non−zero ID code can be used during setup and debug of the I^2C physical bus application and device driver firmware layers, i.e. a read request by a controller to the target's 0x82 register should return the target's hard−coded device ID string.

Diagnostic Register Clearing

The NCV760040 outputs are protected against short to battery conditions (STB), short to ground conditions (ILIM), and excessive junction temperature conditions (TSD). Each channel provides independent diagnostics for these conditions. The outputs are also globally protected against abnormal input voltage conditions (VINx UV/OV) with provision for independent diagnostics of these conditions. For details about these embedded protections, refer to their corresponding datasheet sections.

Fault recovery is a multi−step process which may include

- determining whether the fault class is global or per−channel (read 0x71/R9);
- determining the specific fault type (read 0x31…0x61/R5…R8.D[5:0]);
- verifying the affected output's expected output state (read 0x11/R0.EN_OUTx);
- taking possible actions to resolve the fault's cause;
- clearing the corresponding diagnostic register bit (write 0x31…0x61/R5…R8.D[4:0]).

It is important to understand that diagnosis of a fault condition and recovery from a fault condition are two separate ideas which require different actions. Although it is quite difficult to disentangle the two ideas, this section mainly describes clearing of the diagnostic register bits which report a fault condition. For general information about normal device behaviors and about recovery from fault conditions refer to § Device Modes and Fault Handling.

Two sets of diagnostic registers separately provide global and per−channel status information: The GLOBAL DIAGNOSTICS register provides status information about all outputs and about the VINx voltage supplies. The DIAGNOSTICS OUTx registers provides status information about each output. The registers are comprised of mixed bit types which provide ‘read only’ or ‘read/clear’ access. The reporting behavior of some register bits may also be modified by the Clear On Read (COR) bit located in the 0xA2/R3 CONFIGURATION 2 register. Table 9 summarizes the diagnostic bits and their reporting and clearing behaviors.

Table 9. DIAGNOSTIC REPORTING AND CLEARING BEHAVIORS

Diagnostic Bit Name	Register Location	Condition Detected and Reported	Diagnostic Bit Clearing	
			0xA2.COR = 0	0xA2.COR = 1
GL_STATUS	R9	Global ILIM, TSD, TW, STB, OL	Read only	
STATUS	R5 – R8	OUTx enabled or disabled	Read only	
ILIM	R5 – R8	Overcurrent detected but only reported after OUTx latched off	Write Register Clear Command (RCC) after fault is removed	
TSD	R5 – R8	Overtemperature detected but only reported after OUTx latched off	Write Register Clear Command (RCC) after fault is removed	
TW	R5 – R8	OUTx Temperature Warning	Automatically cleared after fault is removed	Read register DIAGNOSTICS OUTx after fault removed
STB	R5 – R8	OUTx Short To Battery		
OL	R5 – R8	OUTx Open Load		
VINx_UV VINx_OV	R9	Global VINx Monitors Undervoltage or Overvoltage.		Read register GLOBAL DIAGNOSTICS after fault removed

In the case of detection of an output fault (ILIM, TSD, STB) or a global undervoltage fault (VINx UV), the affected output will be disabled. In the case of detection of a global undervoltage fault (VINx OV), the output will be disabled if 0x12/R1.OVLO = ‘1’. In any case, a disabled output’s state can be confirmed by reading STATUS = ‘0’ in its corresponding DIAGNOSTICS OUTx register. A disabled output’s specific fault type can be determined by reading the outputs corresponding DIAGNOSTICS OUTx register.

In the case of a ILIM or TSD fault, the output state is restored by first resolving the identified fault’s cause, then by clearing the indicated diagnostic bit via a Register Clear Command (RCC) to the output’s corresponding DIAGNOSTICS OUTx register after the fault is resolved. The Register Clear Command (RCC) is simply selectively writing ‘0’ to an output’s TSD or ILIM fault bit − or writing ‘0’ to all bits − in its corresponding DIAGNOSTICS OUTx register.

In the case of a STB, TW, UV, or OV fault, the output state is restored automatically after the fault is resolved. The indicated diagnostic bit may also be automatically cleared, or may be modified by the 0xA2/R3.COR bit so that the occurrence of an event causing a diagnostic bit to report is stored for later retrieval and clearing via the Clear−On−Read (COR) functionality.

Note that the behaviors of the various diagnostic bits will be propagated to the fault flag. The persistence of any of the diagnostic bit states is dependent upon a particular event’s behavior (transient or steady−state), and a particular diagnostic bit’s reporting behavior (latched or non−latched/‘real−time’) – which can be modified by the global 0xA2.COR functionality. Also note that when enabled, the COR functionality affects all non−latched diagnostic bits.

In any case, an output’s state depends on (and is restored to) its current EN_OUTx input bit state after fault resolution.

Current Limit and Current Limit Shift

Outputs are protected against short to ground faults and excessive inrush events are limited during output turn on. Each channel independently monitors its output current and provides diagnosis of output shutdown due to high current stress conditions. A channel’s sampled output current is continuously compared against a common baseline current limit reference value I_{LIM} which is programmed via an external resistor R_{CL} at the device’s CL pin.

To help accommodate transient inrush/charging events such as when driving an incandescent lamp load, a large capacitor load, or a motor load’s initial start−up/stall torque, a current limit shift functionality provides per−channel adjustment of the global baseline current limit via the I2C interface. Figure 16 shows the principal elements of the ILIM function.

A ‘failsafe’ functionality is embedded for the case of 1.) open/missing/out−of−range−high or 2.) shorted/short−to−GND/out−of−range−low RCL resistor which bounds the current limit in the ‘open’ case to nominally 100 mA and in the ‘short’ case to nominally 1.2 A. The “current limit shift” multiplier functionality is disabled when either ‘open’ or ‘short’ condition is detected.

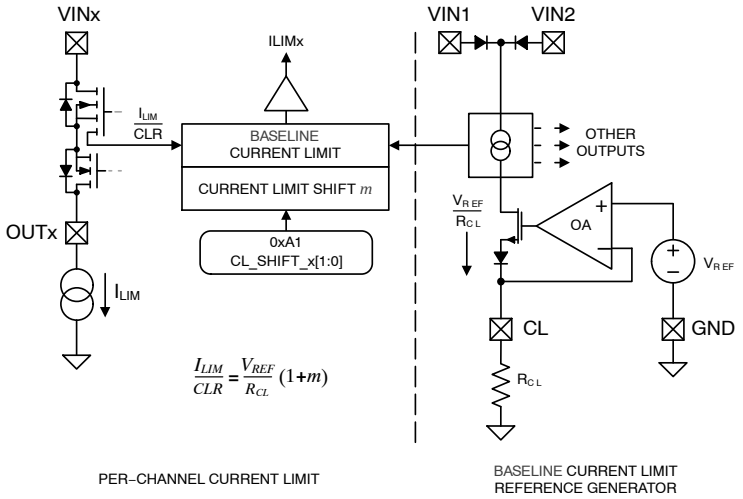


Figure 16. Current Limit Overview

The baseline limit reference I_{LIM} is used by all outputs and is generated via a nominal 1:5000 current sampling ratio *CLR*, a nominal 600 mV internal voltage reference V_{REF}, external resistor R_{CL}, and a limit shift multiplier value *m* (where *m* = 0 for baseline I_{LIM}) according to the equation:

$$I_{LIM} = \left(\frac{CLR \times V_{REF}}{R_{CL}}\right) \times (1 + m); \qquad \text{(eq. 1)}$$

$$m = \{0,\ 0.3,\ 0.6,\ 1.0\}$$

Provided that the CL pin is terminated with a resistor in the range 2.5 kΩ ≤ R_{CL} ≤ 30 kΩ, each channel's baseline current can be separately shifted by a factor 1+*m* with *m* as selected via the CL_SHIFT_X[1:0] bits in the 0xA2/R3 CURRENT LIMIT SHIFT register, resulting in a unique current limit threshold ILIMx for that channel. In the event of an open or shorted R_{CL} resistor, the baseline current limit defaults to defined levels. Table 10 summarizes the operational ranges of the current limit and Figure 17 shows the R_{CL} resistor value vs. the baseline current limit over the range of 100 mA ≤ ILIM ≤ 1.2 A according to:

$$R_{CL} = \frac{CLR \times V_{REF}}{I_{LIM}} = \frac{3000}{I_{LIM}} \qquad \text{(eq. 2)}$$

Table 10. CURRENT LIMIT AND CURRENT LIMIT SHIFT SUMMARY

CL Pin Condition	CL Shift	CL_SHIFT_X[1:0]	CL Shift Value	ILIM Value
Open/Float	Disabled	–	–	Fixed, ≥ 100 mA typ.
2.5 kΩ ≤ R_{CL} ≤ 30 kΩ	Enabled	00	m = 0.0	1.20 A ≥ ILIM ≥ 100 mA
		01	m = 0.3	1.56 A ≥ ILIM ≥ 130 mA
		10	m = 0.6	1.92 A ≥ ILIM ≥ 160 mA
		11	m = 1.0	2.40 A ≥ ILIM ≥ 200 mA
GND	Disabled	–	–	Fixed, ≤ 1.2 A typ.

Note that while the channels are capable of up to nominally 1.2 A baseline or 2.4 A shifted output currents, thermal limitations of the device's package together with the thermal design of the application must be considered in all cases.

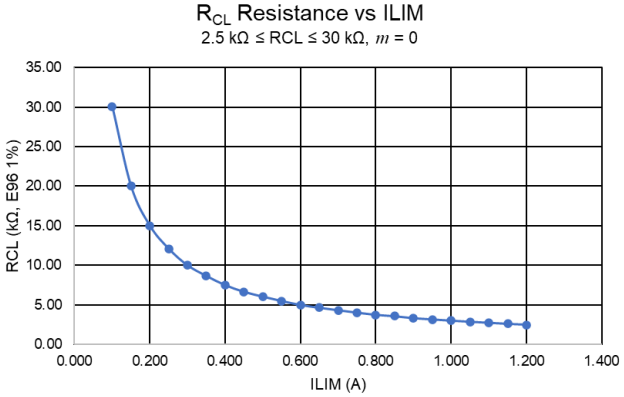


Figure 17. RCL Resistance vs. Baseline Current Limit

In operation, a channel's output current is sampled using a Current Limit Ratio *CLR* having a nominal value of 5000. The sampled I(OUTX) current is compared against the channel's unique reference current ILIMx. Whenever the channel's output current exceeds its limit current (i.e. I(OUTx) > ILIMx), a timer Tlatch(x) is started. Once started, the timer runs to completion.

The Tlatch(x) timeout interval for each channel also is separately selectable via the 0x12/R1 CONFIGURATION register's LATCH_X bits, allowing a nominal choice of 20 μs or 20 ms timeout. If the condition I(OUTx) > ILIMx exists when t ≥ Tlatch(x), an ILIM condition is detected, the output is disabled, and the channel's ILIM diagnostic bit is set to '1'. Refer to § Diagnostic Register Clearing for details about re−enabling the output.

The time t_{CHG} needed to charge the OUTx and load capacitances C_{OUT} is dependent upon the *VINx* voltage, the $R_{DS(ON)}$ of the back−to−back output switch, the load resistance R_L, and the I_{ILIM} value as modified by a CL_SHIFT value. During the time C_{OUT} is charging − up until the selected Tlatch(x) timeout − the output acts as a constant−current source. Assuming the capacitances have zero initial charge, the output voltage V_{OUT} rises according to:

$$V_{OUTX}(t) = \left(I_{ILIM} \times R_L\right)\left(1 - e^{-t/\tau}\right); \quad \text{(eq. 3)}$$

$$R = R_L + R_{DS(on)},$$

$$\tau = RC_{OUT}$$

To prevent the output from shutting down due to a capacitive inrush event, the condition t_{CHG} < Tlatch(x) must be satisfied. The time t_{CHG} can be estimated by re−arranging Equation 3 and substituting V_{INx} − scaled according to the $R_{DS(ON)}$ and load resistance R_L − for $V_{OUT(t = \infty)}$:

$$t_{CHG} = -\tau \times \ln\left(1 - \frac{V_{OUTX}(t)}{I_{ILIM} \times R_L}\right); \quad \text{(eq. 4)}$$

$$V_{OUTX}(t)\,|_{t=\infty} = VIN_X\left(\frac{R_L}{\left(R_L + R_{DS(on)}\right)}\right)$$

Substituting VINx = 9 V, ILIM = 450 mA, $R_{DS(ON)}$ = 0.5 Ω, R_L = 22 Ω, and C_{OUT} = 20.1 μF into Equation 4 yields $t_{CHG} \approx$ 920 μs and $V_{OUT} \approx$ 8.8 V. Since this solution results in t_{CHG} > Tlatch0 (i.e. 920 μs > 20 μs nominal), a channel operating under the given conditions must use Tlatch1 (20 ms nominal).

Current Sense and ADC

An 8−bit ADC converts a voltage at the current sense CS pin for readout via the 0x21/R4 ADC READOUT register. The ADC input voltage source is selected via the 0x12/R1 CONFIGURATION register bits SENSE_SELECT[2:0]. The voltage may be either an external signal or the sampled output current from one of the NCV760040's four channels. The current sense and ADC functionalities are disabled when 0x12/R1.SENSE_SELECT[2:0] = 0b000 (default).

Figure 18 shows the embedded functionality comprised of two basic circuit blocks: a 'front end' OUTx current sampling block with a single global 'back end' ADC block.

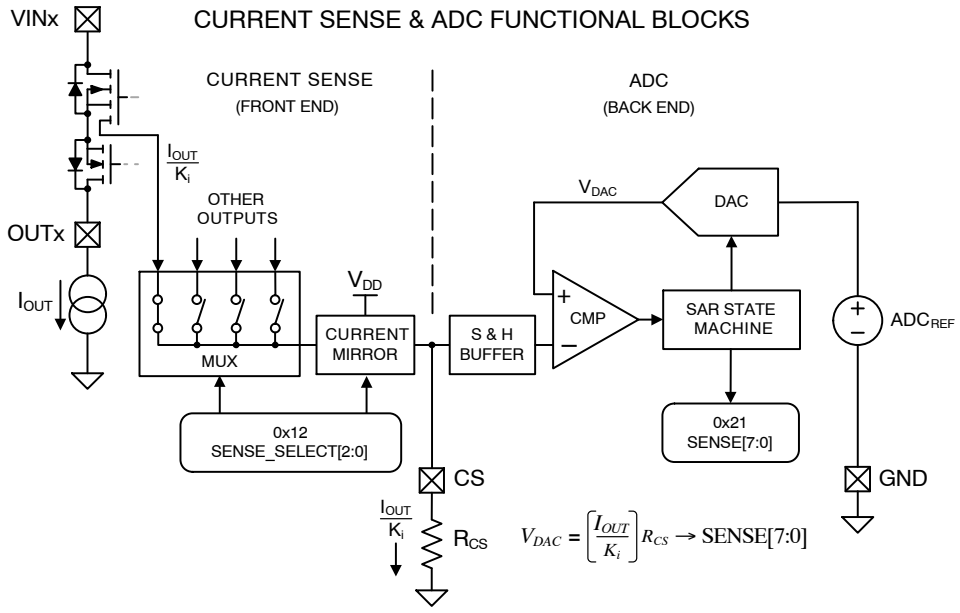


Figure 18. Current Sense and ADC Functional Blocks

The two blocks combine at the CS pin boundary where a portion of the output current I_{OUT} is sampled by a nominal 1:200 ratio K_i and converted to a voltage via an external resistor R_{CS}, which the ADC then samples, quantizes and digitizes for readout according to:

$$V_{DAC} = \left(\frac{I_{OUT}}{K_i}\right) \times R_{CS} \rightarrow SENSE[7:0] \quad \text{(eq. 5)}$$

The ADC's nominal Full−Scale Voltage (FSV) conversion range is 0 to 0.996 V. The ADC's output range

can be adapted to the programmed baseline current limit by adjusting the R_{CS} resistor value according to:

$$R_{CS} = \frac{K_i \times FSV}{I_{LIM}} = \frac{199.22}{I_{LIM}} \quad \text{(eq. 6)}$$

The equations for the R_{CL} (Equation 6) and R_{CS} (Equation 2) resistors are each referred to the I_{LIM} baseline current limit. The ratio of the two resistor values conveniently yields a constant value according to:

$$\frac{R_{CS}}{R_{CL}} = \frac{K_i \times FSV}{CLR \times V_{REF}} = 0.0664 \quad \text{(eq. 7)}$$

so that $R_{CS} = 0.0664 \times R_{CL}$, which simplifies the valuation of the R_{CS} resistor. Once an R_{CS} value is selected, the ADC's conversion sensitivity I_{LSB} can be determined according to:

$$I_{LSB} = \left(\frac{ADCref}{2^{ADCres}}\right)\left(\frac{K_i}{R_{CS}}\right) \quad \text{(eq. 8)}$$

The quantized value of the sampled I_{OUT} current can then be resolved using the corresponding I_{LSB} sensitivity and the digital value returned via the ADC READOUT register according to:

$$I_{OUT} = I_{LSB} \times (SENSE[7:0])_{10} \quad \text{(eq. 9)}$$

The R_{CS} resistor voltage may also be monitored by connecting the CS pin to an external ADC. An external signal can be converted via the internal ADC by connecting the signal to the CS pin and configuring the internal ADC accordingly via the configuration register SENSE_SELECT[2:0] bits. The external signal should be in the range $0\ V \le V_{CS} \le$ ADCref and must be bounded by the range of $0\ V \le V_{CS} \le VDD$. Refer to Figure 1 for these optional connections.

Figure 19 shows the values of R_{CS} vs. the baseline I_{LIM} current limit over the range of $100\ mA \le I_{LIM} \le 1.2\ A$. Per the equations for adjusting R_{CS} (Equations 6 and 7), this range of currents results in a corresponding R_{CS} range $2\ k\Omega \ge R_{CS} \ge 165\ \Omega$. Evaluating this R_{CS} range per the sensitivity equation yields an I_{LSB} sensitivity range $0.392\ mA \le I_{LSB} \le 4.7\ mA$ (Figure 20).

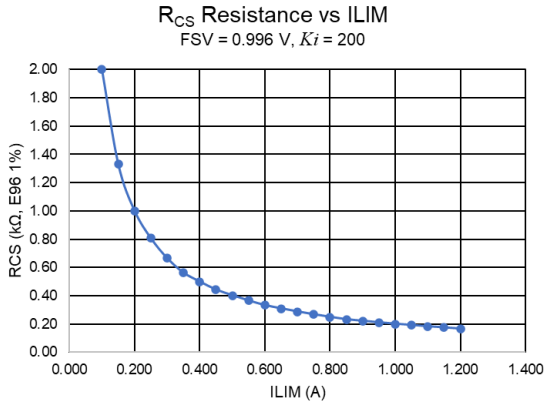


Figure 19. RCS Resistance Value vs. ILIM Baseline Current Limit Value

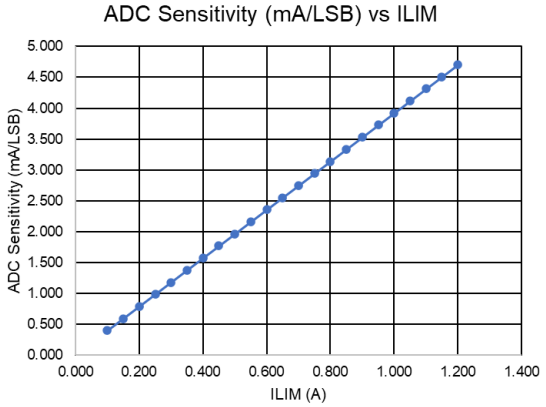


Figure 20. ADC Sensitivity vs. ILIM Baseline Current Limit Value

The 0x21/R4 ADC READOUT Register provides for retrieval of converted output current sense data or for retrieval of converted external signal data. The returned data represents the conversion of the last input source value sampled by the ADC. The desired ADC input source is selected via the 0x12/R1CONFIGURATION register. Once an input source is selected, the conversion process runs continuously. The nominal 12 µs conversion cycle time ADCtconv includes signal acquisition and quantization. The most recent conversion data is held for retrieval via I2C while the next conversion cycle is in process.

Table 11 summarizes the digitized 0x21 ADC READOUT register responses vs. the device state when the ADC input source is configured for internal current sense readout. The readout register response assumes (1) that 0x11.OUTx is the active channel and (2) that 0x12.SENSE_SELECT[2:0] multiplexer is pointing to the active OUTx. A 'failsafe' functionality is embedded such that in the event of a shorted or open R_{CS} resistor, the ADC SENSE[7:0] data defaults to defined static levels 0x00 and 0xFF respectively.

Table 11. ADC READOUT REGISTER 0x21 VALUE vs. DEVICE STATE

EN_OUTx State	OUTx State	CS Pin State	0x21 Value	Note
0	OFF	X	0x00 0x00 – 0xFF	9 10
1	ON	GND	0x00	11
1	ON	Open	0xFF	11
1	ON	R	0x00 – 0xFF	10, 12
1	ON: ILIM	R	0xFF	13, 16
	OFF: ILIM		0x00 – 0xFF	10, 14
1	OFF: STB	R	0x00 – 0xFF	10, 15

9. Default value after power−on reset.
10. Last value sampled by the ADC.
11. CS pin shorted to GND or CS resistor open.
12. Normal operation with resistor 'R' connected at the CS pin.
13. ILIM inrush during initial turn−on while t < Tlatch0|1.
14. ILIM short to GND event after t > Tlatch0|1.
15. Output is forced off during a short to battery event.
16. ADC value in transient state.

Figure 21 shows the ADC behavior when channel output current is selected as the ADC input signal source prior to enabling the output. When the output is enabled, a nominal 200 μs blanking timer ADCtblnk is started during which the 0x21 SENSE data is forced to 0x00 as the output begins to turn on. If the output was already enabled when selected as the ADC input source, the blanking timer does not run and the ADC conversion begins immediately. Note that 0x21 = 0x00 is a transient state that may not be observed.

If the output is connected to a purely resistive load, the current may quickly rise to its steady−state I_{LOAD} value. The ADC starts a first conversion cycle after the ADCtblnk time completes, and an I2C ADC READOUT read request will return the most recently converted load current data.

If the output is connected to a capacitive load, the current may initially rise above the I_{LIM} threshold level in which case an I_{LIM} condition is detected and a Tlatch timer will be started. Whenever an output is operating in an I_{LIM} condition, ADC SENSE data is forced to 0xFF. If the ADC starts a first conversion cycle (after ADCtblnk) while output current remains above the I_{LIM} threshold value, an I2C ADC READOUT read request may return the (forced) 0xFF data.

If the output current settles below the I_{LIM} threshold before the Tlatch timer expires, the output will remain on and an I2C ADC READOUT read request will return the most recently converted load current data. Otherwise, the output will be latched off due to an I_{LIM} fault condition and an I2C ADC READOUT read request will return 0x00.

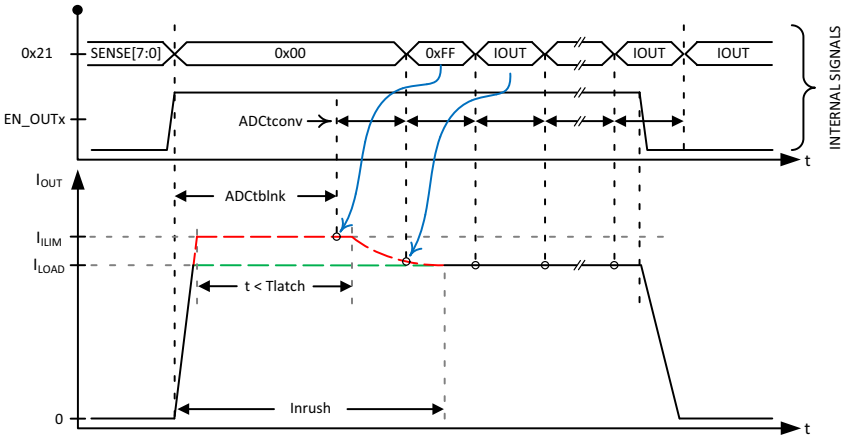


Figure 21. Channel Output Current Conversion Timing

When an external signal is selected as the ADC input source immediately after wake, conversion of the signal begins without delay. When the ADC input source is changed from one active channel to another, or is changed from an internal signal to an external signal, conversion of the previously selected input source will be completed, and conversion for the newly selected input source will begin immediately thereafter.

The ‘normal’ ADC input range of an internal or external signal is 0V ≤ V(CS) ≤ ADCref (i.e. 1.0 V) , and the ‘normal’ ADC digital output range is 0x00 ≤ SENSE[7:0] ≤ 0xFF. In the case of a shorted CS pin condition, the ADC readback data is forced to the defined static value 0x21 = 0x00. In the case of an open CS pin condition: if the ADC input is an internal signal, the ADC readback data is forced to the defined static value 0x21 = 0xFF; if the ADC input is an external signal, the readback data is undefined. In the case when the ADC is disabled (i.e., 0x12.SENSE_SELECT[2:0] = 0b000) the readback data represents the conversion of the last input source value sampled by the ADC.

The ADC readback data received is dependent upon the relative time between the last conversion (i.e., the most recently completed conversion) and the time when the I2C read request is received, after which the last conversion data is loaded from a shadow register into the I2C SDA output buffer for transmission to the requester. To assure accuracy of the received data in the case of an internal ADC input signal, its plausibility can be checked by confirming that the selected channel is enabled (i.e., 0x11.EN_OUTx = 1) and that no fault state has disabled the selected channel.

VINx Voltage Monitoring

The four outputs are grouped in pairs and powered via one of two independent supply inputs VIN1 and VIN2 (Figure 2). The supply inputs can be directly connected to a conditioned battery voltage bus or to a lower bus voltage such as may be supplied via a DC−DC converter within an application (Figure 1). The OUTx outputs are each mapped to their corresponding VINx inputs: OUT1 and OUT2 to VIN1; OUT3 and OUT4 to VIN2.

VIN1 and VIN2 are each separately monitored for overvoltage and undervoltage events. During an undervoltage event the corresponding outputs are disabled and the event is reported in the 0x71/R9 Global Diagnostics register VINx_UV bits. Outputs will automatically recover once the affected VINx voltage rises above the undervoltage threshold hysteresis.

During an overvoltage event, the corresponding outputs normally remain active and can be optionally configured to be disabled during overvoltage via the overvoltage lockout

bit 0x12/R1 OVLO. The event is reported in the 0x71/R9 Global Diagnostics register VINx_OV bits. Outputs will remain on if OVLO = 0, or will be disabled if OVLO = 1 and will automatically recover when VINx voltage falls below the over voltage threshold hysteresis.

Upon recovery from a monitored event, the 0x71/R9 VINx_UV and VINx_OV reporting bits are cleared automatically (0xA2/R3 COR = 0) or retain the recorded event for later retrieval (0xA2/R3 COR = 1). Refer to Figure 14 for an overview of under/over voltage (UV/OV) mapping and COR configuration. Refer to § R3 CONFIGURATION 2 Register for details about the COR bit.

Note that the device's global VINx undervoltage and overvoltage monitors can provide an additional non−latched fault type which – when *modified* by the overvoltage lockout bit (0x12.OVLO = 1) – can disable the outputs associated with the affected VINx path, and cause the DIAGNOSTICS OUTx STATUS bit to report '0' during an overvoltage event *without indicating any other condition within the DIAGNOSTICS OUTx register itself*.

Refer to § R5 − R8 DIAGNOSTICS OUTx Register and § R9 – GLOBAL DIAGNOSTICS Register for details about the individual OUTx diagnostic and the global diagnostic reporting functionalities. Refer to § Diagnostic Register Clearing for details about register clearing functionalities.

Temperature Monitoring

Each channel contains an independent thermal sensor responsible for providing Thermal Warning (TW) and Thermal Shutdown (TSD) functionalities. TW is activated when the junction temperature of an output crosses above the thermal warning threshold Twr. The output remains on during thermal warning, and the event is recorded in the affected output's diagnostic register TW bit.

The TW bit will be cleared automatically (0xA2/R3 COR = 0) after junction temperature falls by the thermal warning hysteresis value, or will retain the recorded event for later retrieval (0xA2/R3 COR = 1). Refer to § R3 CONFIGURATION 2 Register for details about the COR bit.

TSD is activated when the junction temperature of an output exceeds the thermal shutdown threshold Tsd. The output is immediately latched off upon crossing this threshold, and the event is recorded in the affected output's diagnostic register TSD bit. The output's diagnostic register must be cleared prior to re−enabling the output. Refer to § Diagnostic Register Clearing for details about diagnostic register clearing functionalities.

Short to Battery Protection

Short to Battery (STB) protection is separately provided for each output. Upon detection of a STB event, an affected output is disabled and its back−to−back output MOS block back feeding of the corresponding VINx supply input. The blocking action provided by the MOS transistors' body diodes suppresses STB fault propagation to an unaffected output. Figure 22 shows the basic STB detection topology.

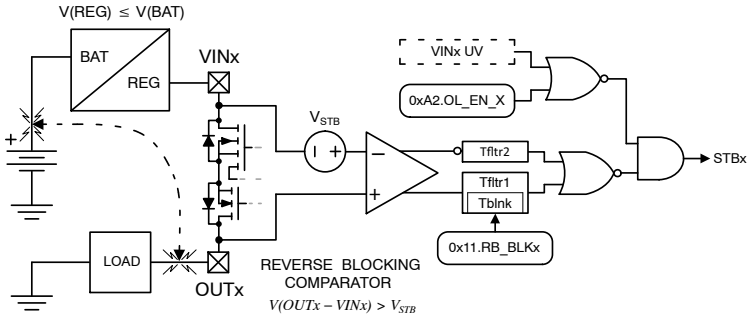


Figure 22. Short to Battery (STB) Detection and Reverse Blocking Principle

Detection is provided for each channel in both the on state and off state via a nominal 300 mV detection reference V_{STB} and a voltage comparator. The V_{STB} voltage is referenced to the appropriate VINx for its corresponding outputs. When an output's voltage exceeds its associated VINx voltage by the V_{STB} reference, an STB event is detected.

STB reporting is disabled for a channel when either an undervoltage condition is detected for its associated VINx voltage, or when a channel's off−state open load diagnostic functionality is enabled via 0xA2.OL_EN_X[2:0]. Refer to § VINx Voltage Monitoring and § Off−state Open Load for details about those functionalities.

The comparator's output is buffered via a Tblnk blanking timer and by Tflt1 and Tflt2 filter timers to suppress spurious outputs during output turn−on and to improve its noise margin after turn−on and recovery from a STB event. Turn−on blanking is enabled by default and can be disabled via each channel's 0x11/R0 RB_BLKx bit. Figure 23 shows evolution of the timers with Tblnk enabled.

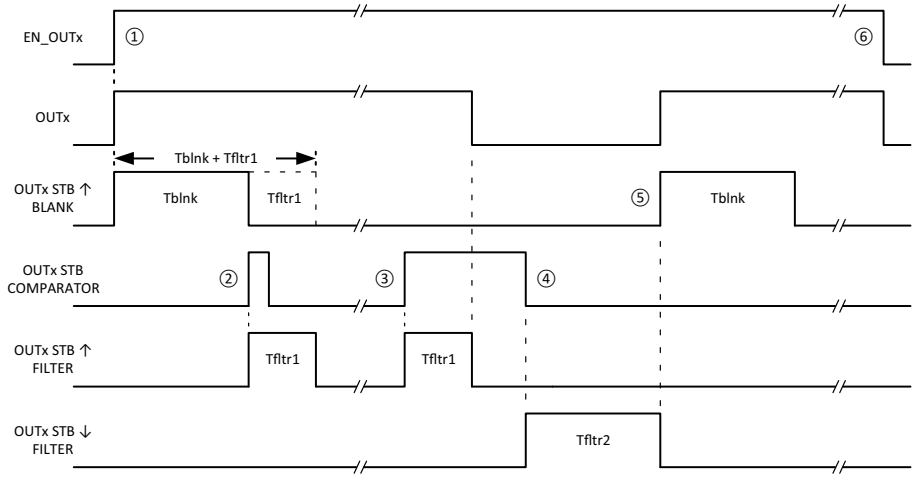


Figure 23. Short to Battery (STB) Deglitch: Blanking Timer and Filter Timer Sequence

At ①, turn−on via a channel's 0x11/R0 EN_OUTx bit starts Tblnk timer. An STB event coincident to Tblnk timeout is detected at ②, which starts a Tfltr1 timer thereby extending Tblnk by the Tfltr1 time. The event is shorter than Tfltr1, so the output remains enabled. The STB detection is unblocked after Tblnk + Tfltr1 timeout.

An STB event detected at ③ starts a Tfltr1 timer. The event is longer than Tfltr1 and so the output is disabled after Tfltr1 timeout. At ④, the STB condition is no longer detected and a Tfltr2 timer started. The output is re−enabled after the Tfltr2 timeout and a Tblnk turn−on blanking timer is started at ⑤. The STB detection is unblocked after Tblnk timeout. At ⑥ the output is disabled via the channel's 0x11/R0 EN_OUTx bit.

The timing sequences of Figure 23 are the same for Tfltr1 and Tfltr2 when turn−on blanking Tblnk is disabled. In the case of STB at an enabled output, the output will be disabled after a Tblk1 deglitch filter timeout. After the STB condition is removed, the output state will be automatically restored after a Tblk2 deglitch filter timeout.

In the case of STB at a disabled output, the output is prevented from being enabled while a STB event is persisting. In any case, an output's state depends on (and is restored to) its current EN_OUTx input bit state after STB resolution.

Short to battery events are reported via a STB bit within each output's DIAGNOSTICS OUTx register and also via the GL_FAULT bit within the GLOBAL DIAGNOSTICS register. The reporting STB bit will be cleared automatically after resolution of an STB condition (0xA2/R3 COR = 0), or will retain the recorded event for later retrieval (0xA2/R3 COR = 1). Reading the registers or attempting to clear an STB condition with a Register Clear Command will not cause the output to re−activate while a short to battery is still present at an output. Refer to § R3 CONFIGURATION 2 Register for details about the COR bit.

Off−state Open Load

An off−state open load (OL) diagnostic augments the embedded current sense ADC. The diagnostic is implemented using a single current source and voltage comparator detection block along with a multiplexer. The detection block is routed to one of the four outputs via the 0xA2/R3 CONFIGURATION 2 register's OL_EN_x[2:0] bits. Figure 24 shows the basic open load diagnostic topology.

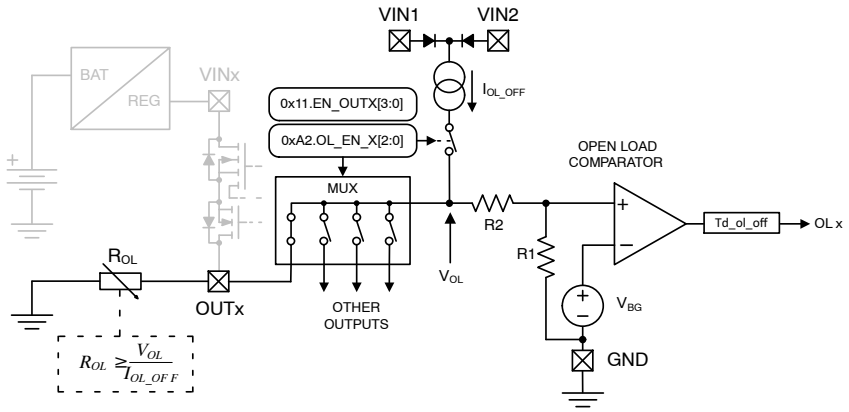


Figure 24. Off−state Open Load (OL) Detection Block

Once a channel has been selected, the diagnostic is enabled when that channel's output is disabled via the 0x11/R0 OUTPUT CONTROL Register's EN_OUTx bits. The diagnostic is automatically disabled when the selected output is re−enabled. If the OL_EN_X bits remain unchanged, the diagnostic is re−enabled for the same output when the output disabled.

Once the diagnostic is enabled, the selected OUTx output's voltage will rise to a level determined by the reference current and the load resistance at the output. An open load is detected and the channel's DIAGNOSTICS OUTx register OL bit will be set if the resistance is greater than the open load detection threshold, whose value R_{OL} is set by the ratio of the Vol reference voltage and the Iol_off reference current:

$$R_{OL} \geq \frac{Vol}{Iol\_off} \quad \text{(eq. 10)}$$

The minimum R_{OL} detection threshold is determined by the minimum voltage and maximum current references as specified in the Electrical Characteristics parametric tables:

$$\frac{Vol(min)}{Iol\_off(max)} \leq R_{OL} \quad \text{(eq. 11)}$$

Using for example Vol = 3.0 V and Iol_off = 100 μA, the detection threshold is 30 kΩ. Open load is guaranteed to be detected above this value, so OUTx loads must be less than the minimum R_{OL} value to avoid false open load detection.

Open load events are reported via the OL bit within each output's DIAGNOSTICS OUTx register and also via the GL_FAULT bit within the GLOBAL DIAGNOSTICS register. The reporting OL bit will be cleared automatically after resolution of an OL condition (0xA2/R3 COR = 0), or will retain the recorded event for later retrieval (0xA2/R3 COR = 1). Refer to § R3 CONFIGURATION 2 Register for details about the COR bit.

The OL diagnostic embeds a nominal filter time Td_ol_off which starts when the detection threshold is crossed. The OL bit is set after the filter's timeout if the comparator state is unchanged. The actual time delay required to wait before reading the OL bits is dependent upon the detection threshold and the external capacitance present on the output pin. The best case assumes a true open load, and the delay can be estimated by using the parametric maximum voltage and minimum current references together with the capacitance C_{OUT} at the output:

$$t_{D\_OL(MAX)} \approx C_{OUT}\frac{Vol(max)}{Iol\_off(min)} + Td\_ol\_off \quad \text{(eq. 12)}$$

Using for example Vol = 3.6 V, Iol_off = 25 μA, and C_{OUT} = 1 μF, the $t_{D\_OL(MAX)}$ detection delay time after the diagnostic current source is enabled is 144 ms (conveniently, the maximum delay is 144 ms per μF given C_{OUT} = 1 μF) plus Td_ol_off.

Loss of Ground Protection

The application is protected against loss of "module" ground connection. Figure 25 is representative of the NCV760040 in a module context. The "LDO" block represents a typical PMOS/PNP pass element LDO topology and is inclusive of reverse battery and transient protections. The resistor R_{VDD} represents additional VDD−supplied loads within the module.

In this context, the 760040 A0 behavior upon loss of 'module' GND is:

- all active OUTx are disabled;
- < 1 μA leakage is produced in the GND path of the combined output loads.

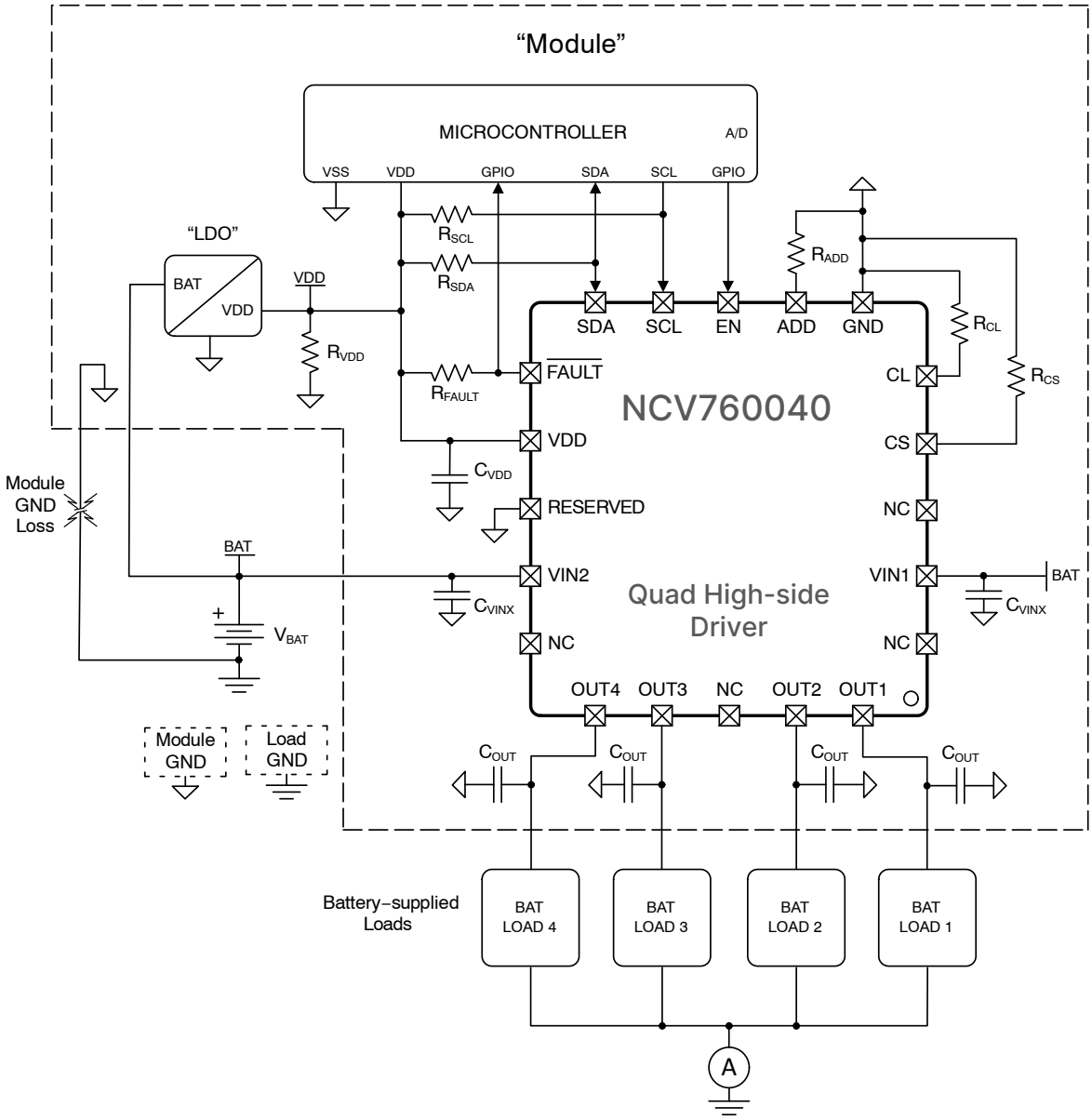


Figure 25. Module Loss of GND Scenario

OUTx Voltage Protection

Each OUTx pin is protected against negative transient voltages produced by the release of stored inductive energy. Simultaneous positive voltage at VINx and negative voltage at OUTx produces dynamic limiting of the OUTx voltage (VCL_N), and the VINx to OUTx difference voltage (VCL_P) which can safely exceed the maximum VinxMax rating. Figure 26 shows the typical clamping response characteristics.

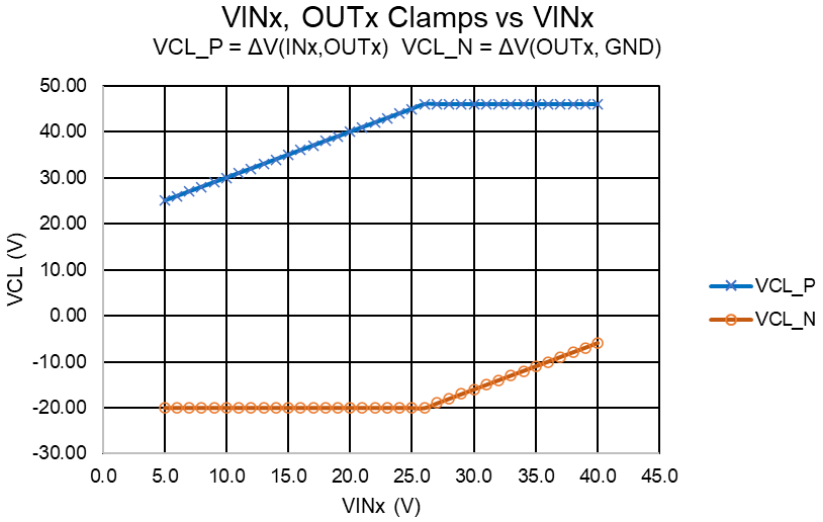


Figure 26. Transient Limiting for V(OUTx) Negative (VCL_N) and V(VINx, OUTx) Differential (VCL_P) Voltages

Figure 27 (left) shows the basic clamping topology. Clamping is dynamically controlled and requires 5 V ≤ VINx ≤ 40 V for proper operation. If it is anticipated that this requirement may not be met, an external protection such as a flyback diode must be added as shown in Figure 27 (right).

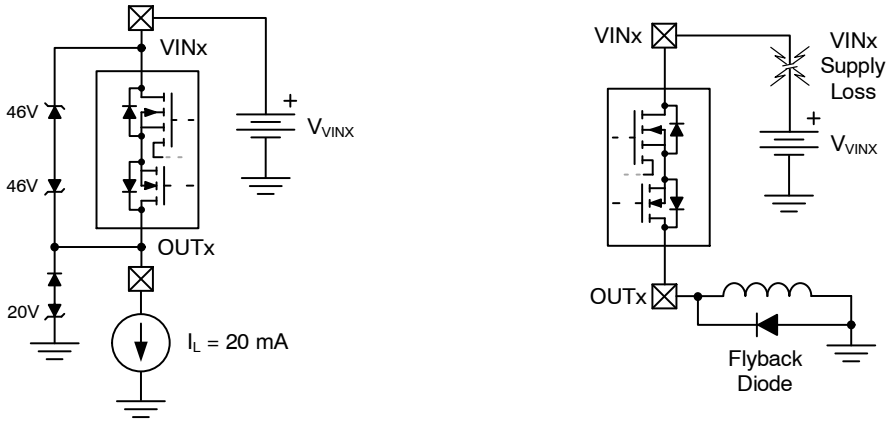


Figure 27. Left: Internal Transient Voltage Limiting Clamps for VINx and OUTx Pins – Simplified Schematic. Right: Flyback Diode in the Case of VINx Supply Interruption.

Device Modes and Fault Handling

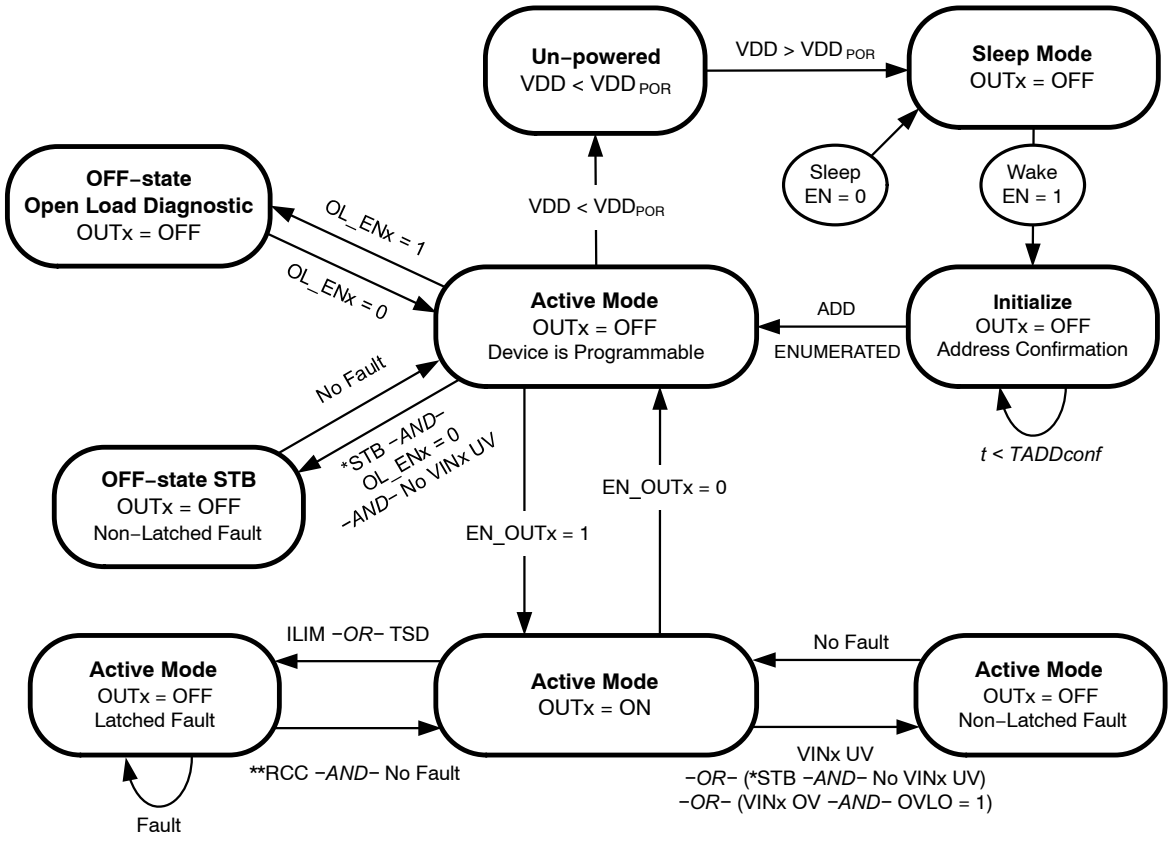
The NCV760040 outputs are protected against short to battery conditions (STB), short to ground conditions (ILIM), and excessive junction temperature conditions (TSD). Each channel provides independent diagnostics for these conditions. The outputs are also globally protected against abnormal input voltage conditions (VINx UV/OV) with provision for independent diagnostics of these conditions. For details about these embedded protections, refer to their corresponding datasheet sections.

It is important to understand that diagnosis of a fault condition and recovery from a fault condition are separate ideas which require different actions. This section mainly describes recovery from a fault condition. For general information about clearing of the diagnostic register bits which report a fault condition refer to § Diagnostic Register Clearing.

The NCV760040 has three primary operating modes:

- unpowered − VDD < VDDpor;
- sleep mode − VDD > VDDpor and EN = 0;
- active mode − VDD > VDDpor and EN = 1.

Figure 28 shows the primary modes and transition states between them under ‘normal’ and ‘fault’ conditions.



*STB reporting is disabled for a channel when either an undervoltage condition is detected for its associated VINx voltage, or when a channel’s off−state open load diagnostic functionality is enabled via 0xA2.OL_EN_X[2:0].

**Register Clear Comm and sent *AND* fault condition removed.

Figure 28. Device Modes and Fault Handling State Diagram

Fault recovery is a multi−step process which may include

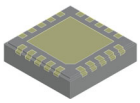
- determining whether the fault class is global or per−channel (read 0x71/R9)
- determining the specific fault type (read 0x31…0x61/R5…R8.D[5:0])
- verifying the affected output’s expected output state (read 0x11/R0.EN_OUTx)
- taking possible actions to resolve the fault’s cause
- clearing the corresponding diagnostic register bit (write 0x31…0x61/R5…R8.D[4:0])

Table 12 summarizes the fault handling and diagnostic reporting, and diagnostic report clearing steps for recovery from a fault condition and for restoring an output from a fault state to a normal state.

Table 12. FAULT HANDLING, DIAGNOSTIC REPORTING, AND DIAGNOSTIC BIT CLEARING SUMMARY

Fault Condition	Fault Handling: Output State vs. Fault Condition			Diagnostic Reporting	Diagnostic Bit Clearing		Note
	Before Fault	During Fault	After Fault		0xA2.COR = 0	0xA2.COR = 1	
OUTx Short to Ground	0x12.LATCH_X = 0 EN_OUTx = 1 = ON	OUTx remains ON in current limit mode; Current sense ADC reading increases to full scale.	OUTx latched OFF after Tlatch0 (20 ms).	OUTx ILIM reported after OUTx latched off.	Send Register Clear Command (RCC) after fault is removed		17, 18
	0x12.LATCH_X = 1 EN_OUTx = 1 = ON		OUTx latched OFF after Tlatch1 (20 µs).				
	EN_OUTx = 0 = OFF	OUTx remains OFF.	OUTx remains OFF.	N/A Detected in on state.	N/A		–
OUTx Overtemp	EN_OUTx = 1 = ON	Output latched OFF.	Output latched OFF.	OUTx TSD reported.	Send Register Clear Command (RCC) after fault is removed		17, 18
OUTx Temp Warning	EN_OUTx = 1 = ON	Output remains ON.	Output remains ON.	OUTx TW reported.	Cleared automatically after fault is removed.	Cleared by reading DIAGNOSTICS OUTx register after fault is removed	19
OUTx Short to Battery	EN_OUTx = 1 = ON	If OUTx >VINx OUTx is disabled and reverse path blocked	Output returns to programmed state.	OUTx STB reported and current sense decreases to zero.			19
	EN_OUTx = 0 = OFF	OUTx remains off and reverse path blocked.	Output remains OFF.	OUTx STB reported.			19
OUTx Open Load	EN_OUTx = 0 = OFF	Output remains OFF.	Output remains OFF.	OUTx OL reported.			19
VINx Undervolt	EN_OUTx = 1 = ON	Outputs are disabled during undervoltage.	Outputs return to programmed state	GLOBAL VINX_UV reported.		Cleared by reading GLOBAL DIAGNOSTICS register after fault is removed	19, 20
VINx Overvolt	0x12.OVLO = 0 EN_OUTx = 1 = ON	Outputs remain ON.	Outputs remain ON.	GLOBAL VINX_OV reported			19, 20, 21
	0x12.OVLO = 1 EN_OUTx = 1 = ON	Outputs are disabled during overvoltage.	Outputs return to programmed state.				

17. The affected output is latched off after a delay as programmed per each output via the CONFIGURATION register 0x12.LATCH_X bits.
18. See § Diagnostic Register Clearing for additional details about the Register Clear Command (RCC) protocol.
19. The state of the Clear−On−Read (COR) mode bit − selected via the CONFIGURATION 2 register bit 0xA2.COR − affects all non−latched fault types.
20. OUT1 and OUT2 are affected by VIN1 undervoltage/overvoltage, OUT3 and OUT4 are affected by VIN2 undervoltage/overvoltage.
21. The behavior of the affected outputs during a VINx overvoltage condition is programmed via the CONFIGURATION register 0x12.OVLO bit.



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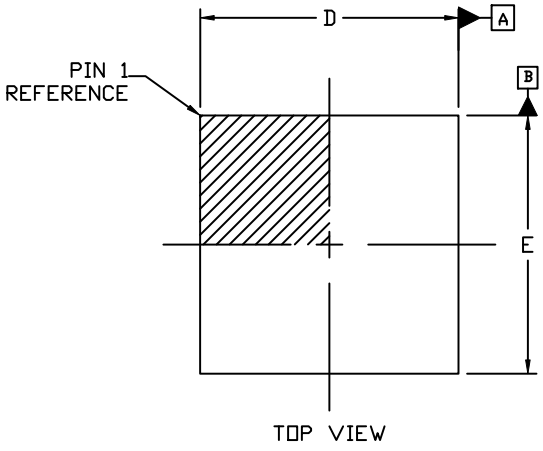
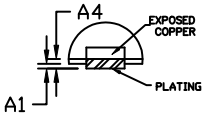
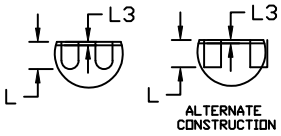


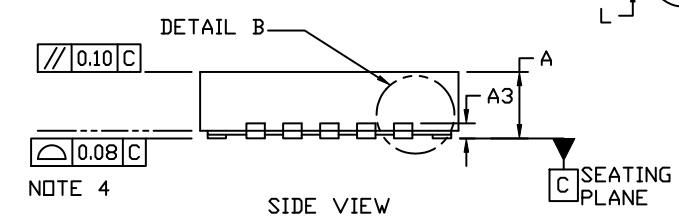


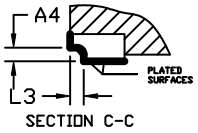


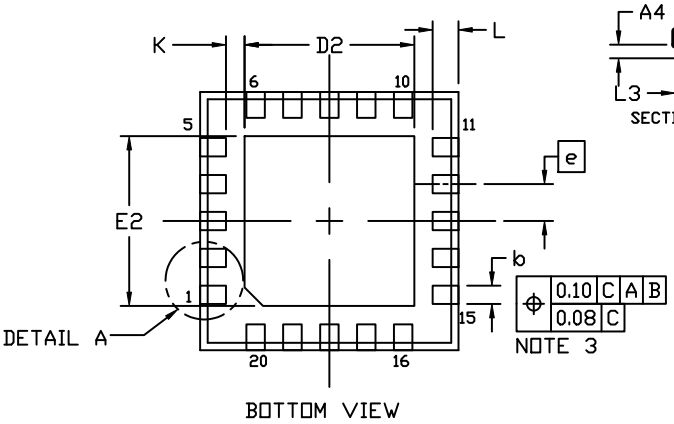
NOTES:

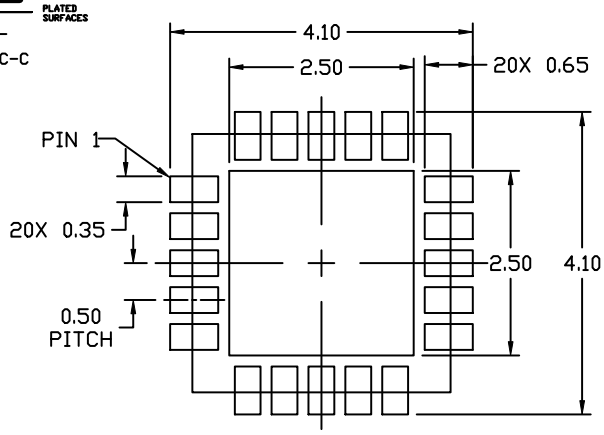
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	3.40	3.50	3.60
D2	2.20	2.30	2.40
E	3.40	3.50	3.60
E2	2.20	2.30	2.40
e	0.50 BSC		
k	0.25 REF		
L	0.25	0.35	0.45
L3	---	---	0.09









RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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