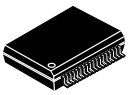
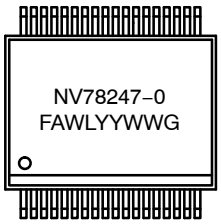
Series String Pixel Controller for Automotive (Front) Lighting

NCV78247



SSOP−EP
36 LEAD
CASE 940AB



NV78247−0 = Specific Device Code
F = Fab Indicator
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV78247DQ0AR2G	SSOP36 EP (P−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Introduction

The NCV78247 is a single−chip pixel controller with embedded switches to control the LEDs in a series LED string, designed for automotive lighting applications and it is in particular designed for high current LEDs. In order to make a pixel light solution, the LEDs needs to be powered by preference with a current source like the NCV78763 or NCV78723/713 or NCV78825 LED drivers. The NCV78247 pixel controller devices receive the pixel control parameters from the pixel light ECU which translates the required light pattern or light image into individual pixel dimming info.

One pixel controller device can control up−to 12 pixels of 1x or 2x or 3x or 4x 1A LEDs per pixel. The maximum LED string voltage has to be limited to 60 V.

If more than 12 pixels need to be controlled, then multiple pixel controllers can be combined in 1 system.

The 12 integrated switches are typically organized as 12 x 1 switch of 1 A, but can be organized in 6 x 2 switches in parallel to offer 6 x 1 switch of 2 A. Besides that a configuration of two strings of 6 LEDs can be supported too, also other variants are possible.

Features

- Single Chip
- Integrated Switches with Multiple Configuration Options
- Minimum of External Components
- Dimming Controller
- OV Detection
- Over Temp Protection
- Short/open Circuit Detection
- Open LED Failure Automatic Bypass
- Communication Interface to the Pixel Light ECU via SPI
- Switch Slew Rate Control
- Individual Open/Short LED Diagnostic Feedback
- PWM + Phase Shift Unit per Channel
- Efficient SPI Burst Data Transfer
- Synchronization between Multiple Devices
- This is a Pb−Free Device
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Typical Applications

- Static Advanced Front Lighting Functions
  - Glare−free High Beam
  - Static Swiveling
  - Beam Shaping
  - Light Power Adjustment
- Animated Welcome Functions on Signal Lights
- Wiping Blinker

© Semiconductor Components Industries, LLC, 2015

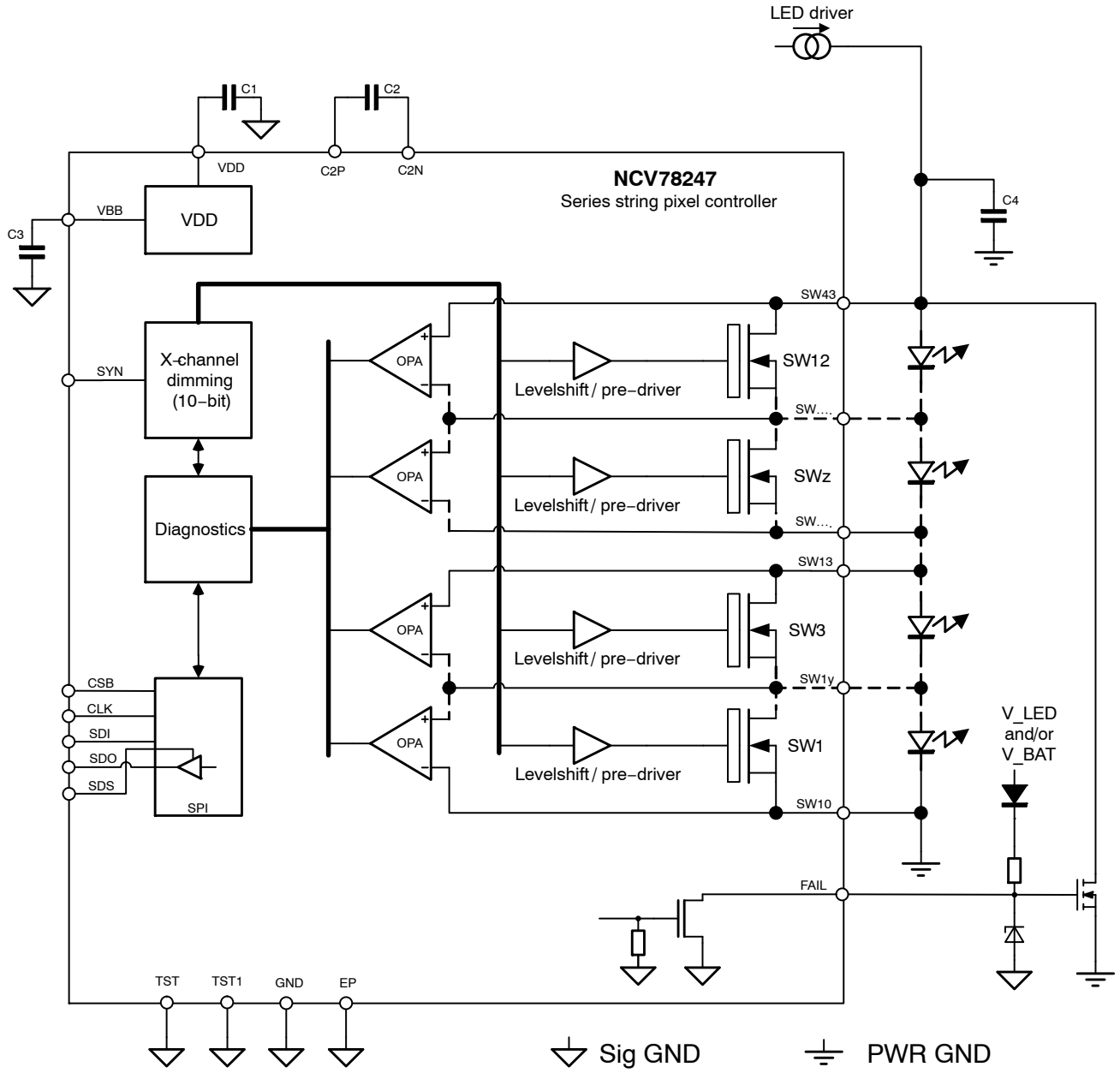


Figure 1. Block Diagram and Application Diagram

NOTE: Unused switches to be shorted externally. The switches should be grounded If a full section is not used.

Table 1. EXTERNAL COMPONENTS

Comp	Function	Min. Value	Typ. Value	Max. Value	Units
C1	Cap. for VDD regulator	300	470	1000	nF
	Cap. for VDD ESR			200	mΩ
C2	Cap. for switch control	150	220		nF
C3	VBB decoupling cap.		100		nF
C4	VLED decoupling cap.		10		nF

PACKAGE AND PIN DESCRIPTION

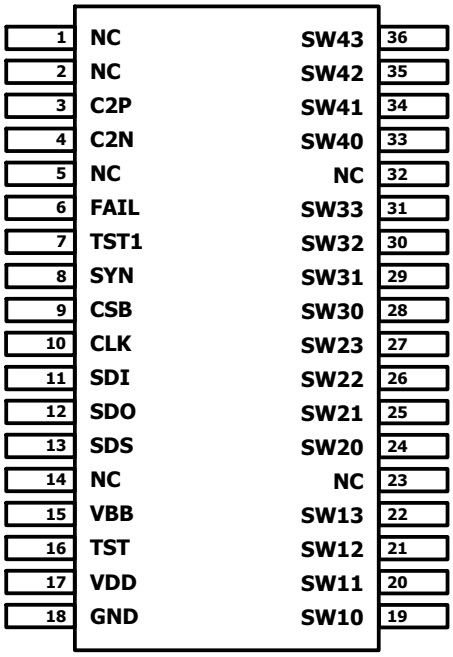


Figure 2. Pin Connections – SSOP36−EP (Top View)

Table 2. PIN DESCRIPTION

Pin No. SSOP36−EP	Pin Name	Description	I/O Type
1, 2	NC	Not used (to be left floating)	
3	C2P	Switch control capacitor connection	HV in/out
4	C2N	Switch control capacitor connection	HV in/out
5	NC	Not used (to be left floating)	
6	FAIL	Open drain output	HV60 out
7	TST1	Internal function. To be tied to GND or left floating	HV60 in/out
8	SYN	External clock for the dimming synchronization / synchronization between the chips	HV60 in/out
9	CSB	SPI chip select (chip select bar)	HV60 in
10	CLK	SPI clock	HV60 in
11	SDI	SPI data input	HV60 in
12	SDO	SPI data output, push−pull when active CSB otherwise in HiZ	HV60 out
13	SDS	External supply for SDO (can be tied to VDD)	HV60 supply
14	NC	Not used (to be left floating)	
15	VBB	Battery supply	HV60 supply
16	TST	Internal function. To be tied to GND	HV60 in
17	VDD	3V analog and logic supply	LV supply
18	GND	Ground	Ground
23,32	NC	Not used (to be left floating)	
19,24,28,33	SWx0	Power switch to short LED	HV in/out
20,25,29,34	SWx1	Power switch to short LED	HV in/out
21,26,30,35	SWx2	Power switch to short LED	HV in/out
22,27,31,36	SWx3	Power switch to short LED	HV in/out
EP	EP	To be tied to GND	

SYSTEM CONFIGURATION

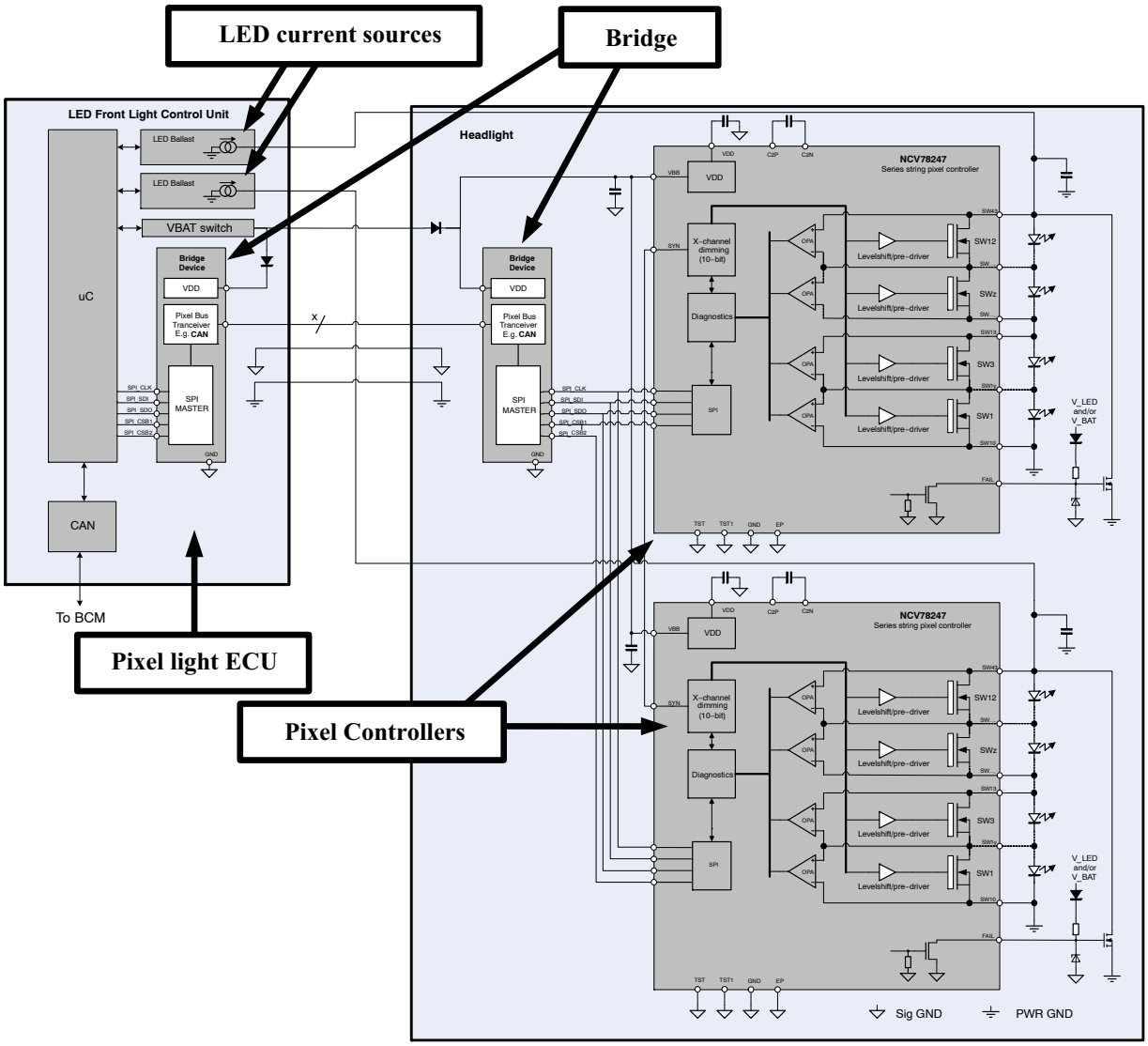


Figure 3. System Configuration Example

The above application diagram shows a set−up with 2 LED strings, controlled by 2 separate Pixel Control devices.

In this example, the Pixel light ECU includes the LED string current sources which power the LEDs. Alternatively, the current sources could also be included in the headlight. The Pixel light ECU calculates the required brightness (PWM duty cycle) for each pixel and sends the pixel control parameters to the NCV78247 pixel controllers.

Communication options:

1. If the system architecture allows, the communication from the Pixel light ECU to the pixel controllers can go directly via the SPI−bus and no bridge is needed in the headlight.
2. Our above application example shows a system design that requires an automotive qualified high speed bus transceiver and a bridge device that runs a proprietary pixel bus protocol over CAN−PHY on one side and a SPI master bus controller on the other side.
   The Pixel light ECU communicates to the LED drivers and stepper drivers (not shown in this drawing) in the headlights over one pixelbus through the bridge device. Each sub−module (separate PCB) in the headlight will be attached to the (one) pixelbus via a bridge controller.

SPI VOLTAGE OPTION

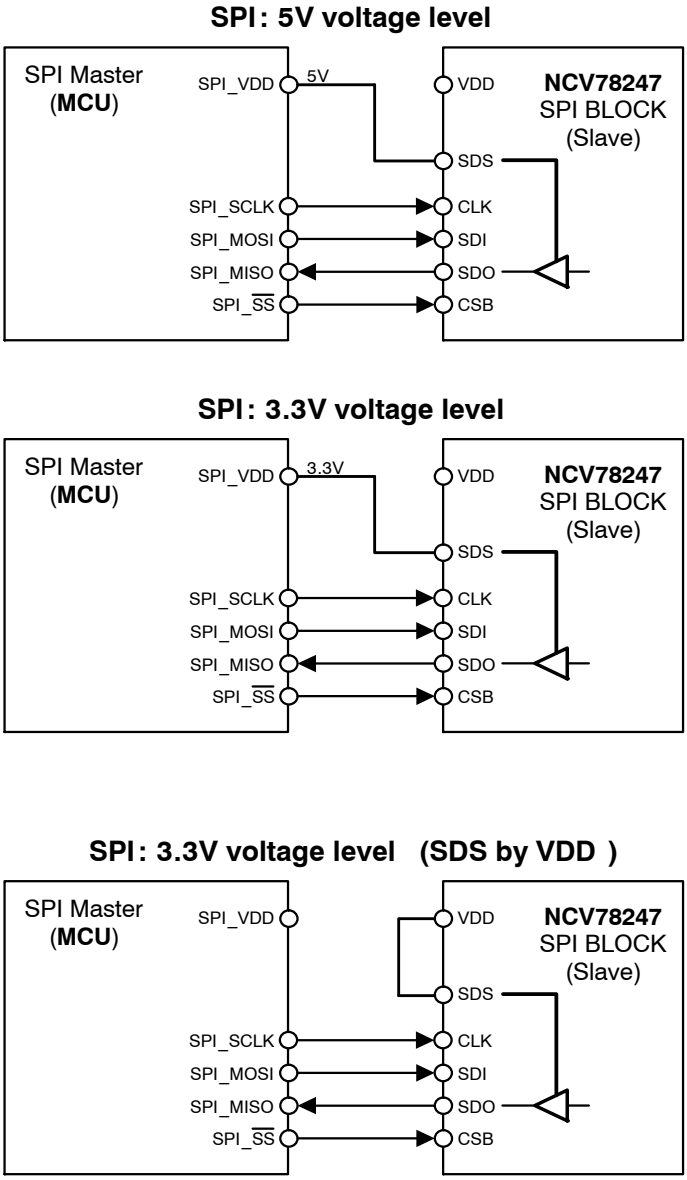


Figure 4. SPI Connection Scenarios

The above application diagrams show a possible SDO supply options between Master and Slave.

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage (Note 1)	V_{BB}	−0.3	60	V
Low voltage supply (Note 2)	V_{DD}	−0.3	3.6	V
High voltage control IO pins (Note 3)	I_{OHV60}	−0.3	60	V
High voltage IO pins (Note 4)	I_{OHV}	−0.3	68	V
Low voltage supply for switch control: V2 = C2P − C2N	V_2	−0.3	3.6	V
Switch differential voltage (Note 5)	V_{SWxx_DIFF}	−0.3	10	V
Storage Temperature (Note 6)	T_{strg}	−50	150	°C
Junction Temperature (Note 7)	$T_{junction}$	−45	170	°C
Electrostatic discharge on component level Human Body Model (Note 8)	V_{ESD_HBM}	−2	+2	kV
Electrostatic discharge on component level Charge Device Model (Note 8)	V_{ESD_CDM}	−500	+500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute maximum rating for pins: VBB, TST, TST1
2. Absolute maximum rating for pins: VDD
3. Absolute maximum rating for pins: SYN, CLK, CSB, SDI, SDO, SDS, FAIL
4. Absolute maximum rating for pins: C2P, C2N, SWxy for x={4÷1} & y={3÷0}
5. Absolute maximum rating for pins: SWx_(y+1) − SWxy for x={4÷1} & y={2÷0}
6. For limited time up to 100 hours. Otherwise the max storage temperature is 85°C.
7. The circuit functionality is not guaranteed outside the Operating junction temperature range. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
8. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114−B)
   ESD Charge Device Model tested per EIA/JESD22−C101−A
   Latch − up Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the device outside the operating ranges described in this section is not warranted. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4. RECOMMENDED OPERATING RANGES

Characteristic	Symbol	Min	Typ	Max	Unit
Battery supply voltage	V_{BB}	4.5		40	V
Switch differential voltage	V_{SW_DIFF}	0		10	V
LED string voltage	V_{STRING}			60	V
Buck switch output current	I_{SW}			1	A
External synchronization frequency	f_{SYN}	115		1100	kHz
Junction temperature	T_J	−40		150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. THERMAL CHARACTERISTICS

Rating	Symbol	Min	Typ	Max	Unit
Thermal resistance junction to exposed pad (Note 9)	R_{thjp}		3.5		°C/W

9. Includes also typical solder thickness under the Exposed Pad (EP)

Typical current derating curves shown on Figure 5 are calculated by values of Thermal resistance junction to exposed pad (R_{thjp}), LED string current (I_{SW}) and appropriate switch respectively section resistance (SW_1R, SW_3R). Both typical switches resistance and section of three switches resistance are depicted on Figure 6 and Figure 7. Different resistance of each individual switch is caused by internal metallization and wire bonds (see Figure 8).

TYPICAL CURRENT DERATING CURVES

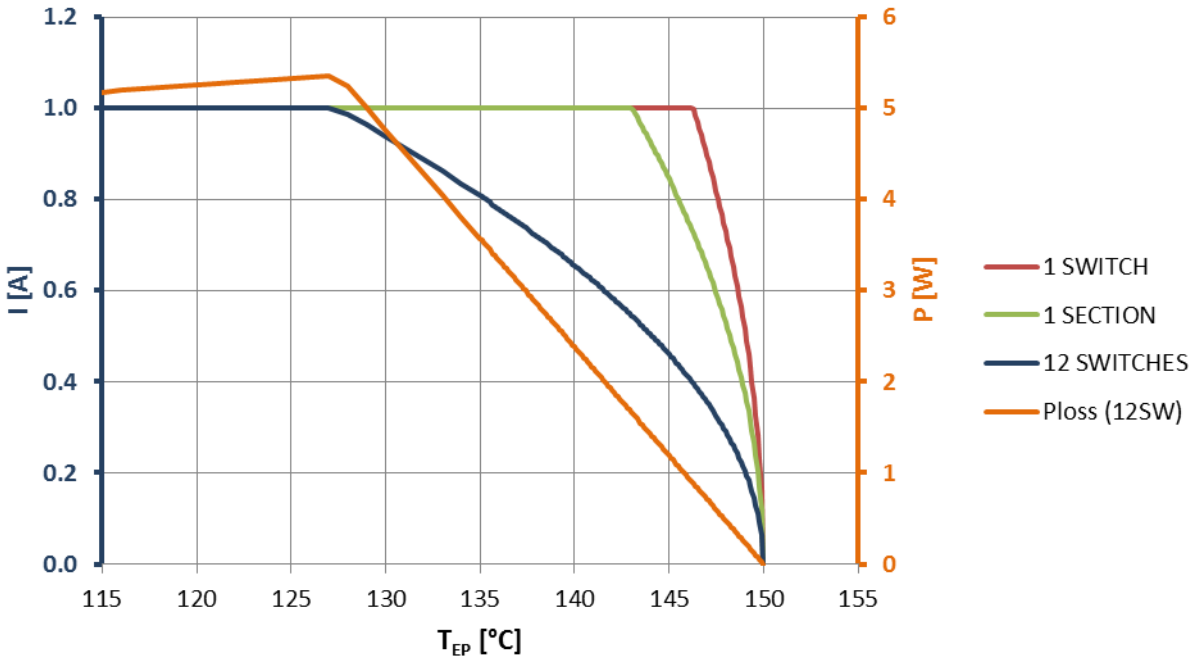


Figure 5. Current Derating Curves

TYPICAL SWITCHES RESISTANCE

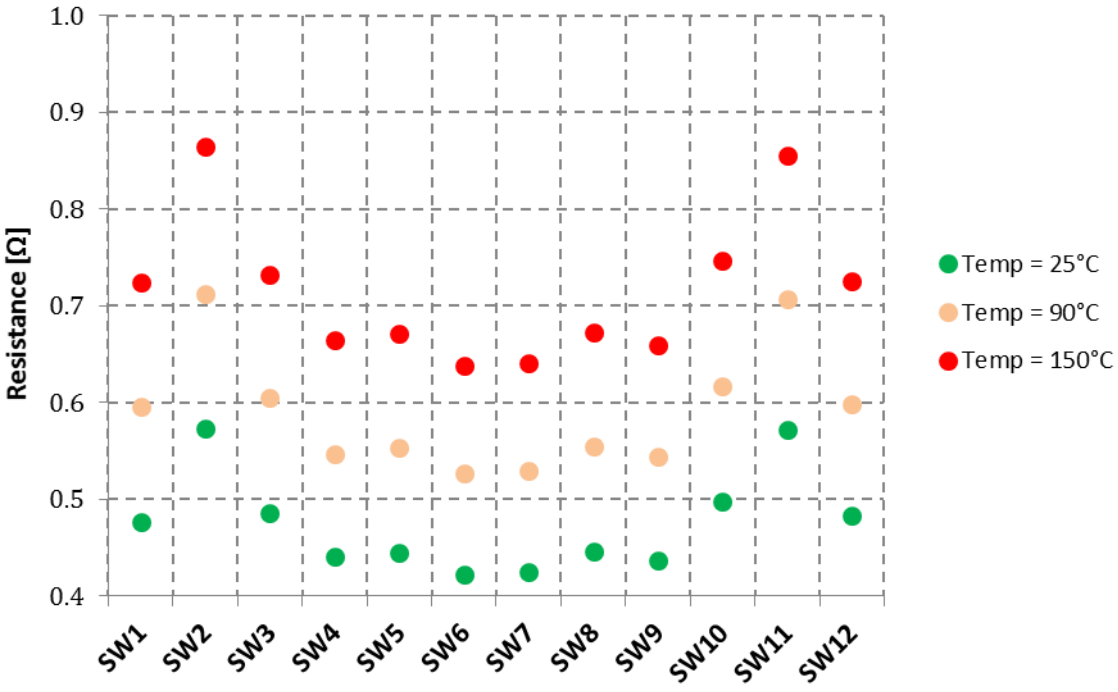


Figure 6. Typical Switches Resistance

TYPICAL SECTIONS RESISTANCE

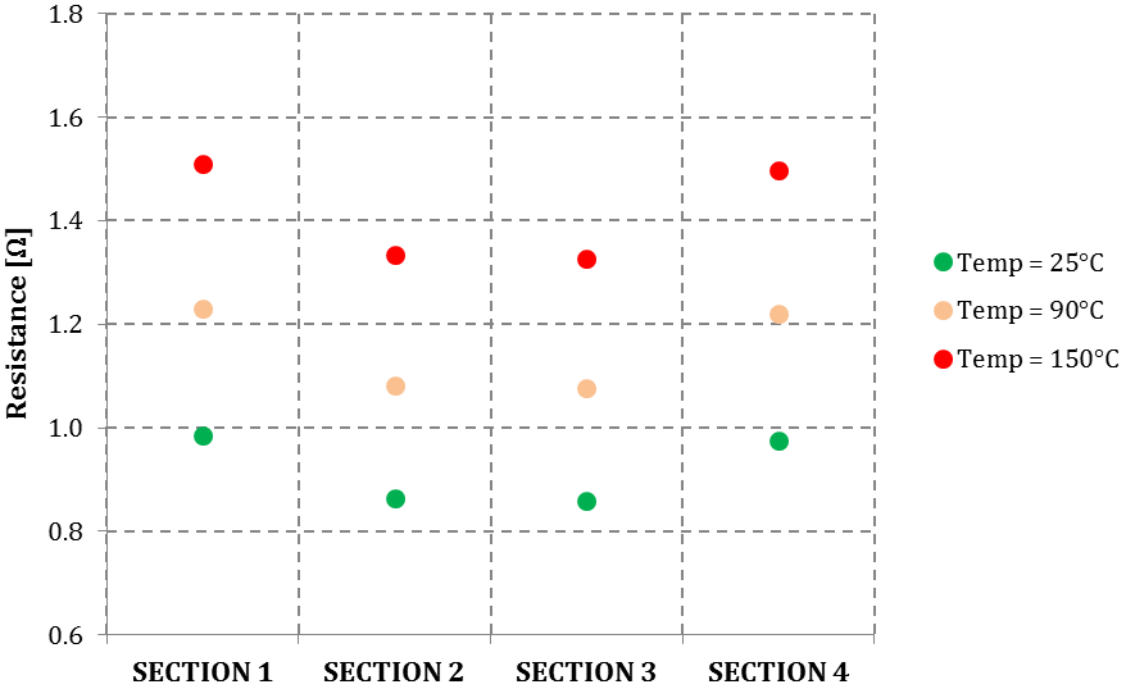


Figure 7. Typical Sections Resistance

EQUIVALENT SCHEMATICS

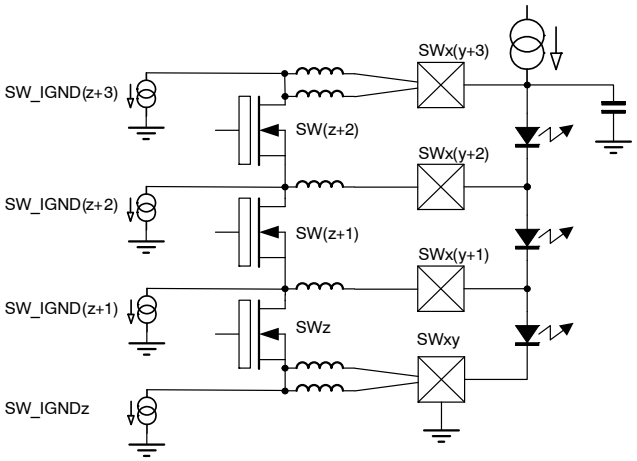


Figure 8. Pixel Switches

ELECTRICAL CHARACTERISTICS

DC Parameters

The DC parameters are guaranteed over junction temperature from −40 to 150°C and VBB in the operating range from 5 to 40 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY AND VOLTAGE REGULATOR							
I_{BB}		Total current consumption			6.5	10	mA
VDD		VDD regulator output voltage		3.15	3.45	3.6	V
VDD_ILIM		VDD regulator current limitation		30		150	mA
POR CHARACTERISTICS							
POR3V_H		VDD POR threshold, V_{DD} rising		2.7		2.95	V
POR3V_L		VDD POR threshold, V_{DD} falling		2.5		2.75	V
POR3V_HYST		VDD POR hysteresis			0.2		V
POR_VBB_H		VBB POR threshold, V_{BB} rising		3.8		4.3	V
POR_VBB_L		VBB POR threshold, V_{BB} falling		3.7		4.2	V
POR_VBB_HST		VBB POR hysteresis			0.1		V
SWITCH CONTROL							
CCH _UVH		V(C2) under voltage threshold, V(C2) rising		2.65	2.75	2.85	V
CCH_UVL		V(C2) under voltage threshold, V(C2) falling		2.6	2.72	2.85	V
CCH_UVHYS		V(C2) under voltage threshold hysteresis		5	30	90	mV
CCH_IBB		Current from VBB to charge C2 capacitor		2		15	mA
CCH_ILIM_RST		Current limitation from VDD (during start−up)		6	12	20	mA
CCH_ILIM		Current limitation from VDD		8	12	16	mA
CCH_VDROP		Voltage drop between VDD and V(C2)			120	270	mV
CCH_V2		V(C2) voltage after recharge CCH_V2 = VDD − CCH_VDROP			3.33		V
PIXEL SWITCHES							
SW_3R		R_{ON} from SWx3 to SWx0 pin (3 switches)			0.9	1.7	Ω
SW_1R		R_{ON} from SWxy to SWx(y−1) pin (1 switch)	Average from 12 switches		0.45		Ω
SW_IGND		Current from SWxy pin to GND (Figure 8)			55		μA
SSH_VTH		Switch Short detection voltage threshold		0.35		1	V
SOV_TH		Switch Overvoltage detection threshold		10		13.5	V
SGD_VIH		Switches string GND detection hi−level input voltage			1.2		V
SGD_VIL		Switches string GND detection low−level input voltage			1.2		V
OVD_VTH		LED string over voltage threshold		63	65.5	68	V
THERMAL WARNING & SHUTDOWN							
T_{tw}		Thermal warning		155	160	165	°C
T_{tsd}		Thermal shutdown		165	170	175	°C

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Conditions	Min	Typ	Max	Unit
TEMPERATURE COMPARATOR							
T_{tc0}		Temperature comparator threshold	<TEMP_THR[2:0]> = 0	70	80	90	°C
T_{tc1}		Temperature comparator threshold	<TEMP_THR[2:0]> = 1	80	90	100	°C
T_{tc2}		Temperature comparator threshold	<TEMP_THR[2:0]> = 2	90	100	110	°C
T_{tc3}		Temperature comparator threshold	<TEMP_THR[2:0]> = 3	100	110	120	°C
T_{tc4}		Temperature comparator threshold	<TEMP_THR[2:0]> = 4	110	120	130	°C
T_{tc5}		Temperature comparator threshold	<TEMP_THR[2:0]> = 5	120	130	140	°C
T_{tc6}		Temperature comparator threshold	<TEMP_THR[2:0]> = 6	135	140	145	°C
T_{tc7}		Temperature comparator threshold	<TEMP_THR[2:0]> = 7	145	150	155	°C
T_{tc_hyst}		Temperature comparator hysteresis			3		°C
5V TOLERANT DIGITAL INPUTS (CLK, CSB, SDI, SYN) (Note 10, 11)							
VINHI		High−level input voltage		2			V
VINLO		Low−level input voltage				0.8	V
RPULL		Input pull up/down resistor		40		160	kΩ
PUSH−PULL DIGITAL OUTPUT SDO							
SDO_VOLO		Low−level output voltage	I_{OUT} = 10 mA			0.4	V
SDO_ROLO		Equivalent output resistance	Low−side switch		30	80	Ω
SDO_VOHI		Hi−level output voltage		V_{SDS} − 0.4			V
SDO_ROHI		Equivalent output resistance			100	290	Ω
SDO_ILEAK		SDO pin leakage current in HiZ				8	μA
SDO_C		SDO pin capacitance			5		pF
PUSH−PULL DIGITAL OUTPUT SYN (Note 11)							
SYN_VOLO		Low−level output voltage	I_{OL} = 4 mA			0.4	V
SYN_ROLO		Equivalent output resistance			50	120	Ω
SYN_VOHI		High−level output voltage	I_{OH} = −4 mA	V_{DD} −0.4			V
SYN_ROHI		Equivalent output resistance			170	350	Ω
SYN_C		SYN pin capacitance			5		pF
60V TOLERANT OPEN−DRAIN DIGITAL OUTPUT FAIL							
FO_VOLO		Low−voltage output voltage	I_{OUT} = 15 mA			1	V
FO_ROLO		Equivalent output resistance	Low−side switch		20	65	Ω
FO_ILEAK		FAIL pin leakage current				8	μA
FO_C		FAIL pin capacitance			5		pF
FO_GRPD		Gate pull down resistor			75		kΩ
60V TOLERANT DIGITAL INPUTS (TST, TST1) (Note 12)							
VINHI		High−level input voltage		2.4			V
VINLO		Low−level input voltage				0.8	V
RPULL		Input leakage current	Pulldown resistance		40	70	kΩ

10. Direction of SYN pin is selected by <DIMSRC> register
11. Pull−down resistor for SYN, CLK and SDI pins, pull−up resistor to VDD for CSB pin
12. Pin TST, TST1 should be connected to ground

AC Parameters

The DC parameters are guaranteed over junction temperature from −40 to 150°C and VBB in the operating range from 5 to 40 V, unless otherwise specified.

Table 7. AC PARAMETERS

Symbol	Pin(s)	Parameter	Conditions	Min	Typ	Max	Unit
INTERNALL OSCILLATOR OSC10M							
FOSC_TR		System oscillator frequency		8.8	10	11.2	MHz
PIXEL SWITCHES							
SOV_DB		Overvoltage protection debounce time	<CMP_DEB> = 0		10		µs
			<CMP_DEB> = 1		15		µs
t_{SW_SLOT}		Time slot between switch activations	<T1_CONF[0]> = 0	8.4			µs
			<T1_CONF[0]> = 1	11.4			µs
SON_TSLOPE		Switch soft slope time (slope control)	<T1_CONF[0]> = 0		1		µs
			<T1_CONF[0]> = 1		4		µs
SON_TFALL		Switch on time (switching slope)	<T1_CONF[1]> = 0		1.1		µs
			<T1_CONF[1]> = 1		0.8		µs
SOF_TRISE		Switch off time	5 mA, without decap cap.		1.6		µs
PUSH−PULL DIGITAL OUTPUT SDO							
SDO_DL		CLK to SDO propagation delay	Low side switch activation/deactivation time			90	ns
PUSH−PULL DIGITAL OUTPUT SYN							
SYN_DL		CLK to SYN propagation delay				90	ns
60V TOLERANT OPEN−DRAIN DIGITAL OUTPUT FAIL							
FO_DL		CLK to FO propagation delay	2 kΩ to 5 V, 100 pF to GND, V(FAIL) goes below 1 V			90	ns

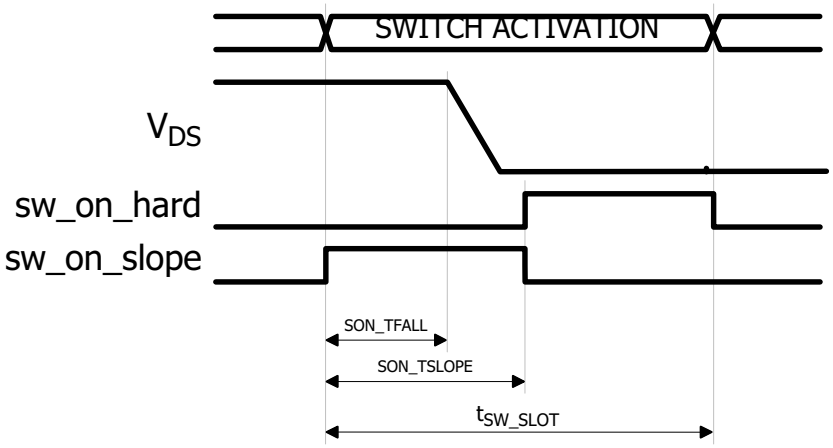


Figure 9. Switch Activation Time Slot

NOTE: Switch activation has two phases. First the gate capacitance of the switch is charged by current source during SON_TSLOPE time. Both the current source value by T1_CONF[1] bit and slope control time by T1_CONF[0] bit can be selected. After it the voltage source is used for charging gate capacitance.

Table 8. SPI INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	SPI clock low after CSB low	400			ns
t_{CLH}	SPI clock high time	125			ns
t_{CLL}	SPI clock low time	125			ns
f_{SPICLK}	SPI clock frequency			4	MHz
t_{EN}	SDO data available after falling SPI clock			70	ns
t_{SDI}	SDI data stable before rising SPI clock	25			ns
t_{HDI}	SDI data stable after rising SPI clock	25			ns
t_{HCS}	SPI clock high before CSB high	65			ns
t_{DIS}	SDO high impedance after CSB high			70	ns
t_{CSOFF}	CSB high time	400			ns
t_P	Pause time on CLK		6		µs

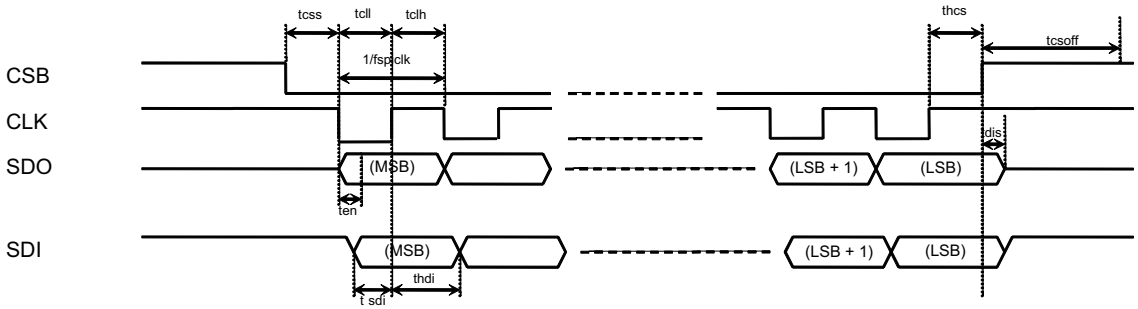


Figure 10. SPI Timing

DETAILED OPERATING AND PIN DESCRIPTION

SUPPLY CONCEPT IN GENERAL

Low operating voltages become more and more required due to the growing use of start stop systems. In order to respond to this necessity, the NCV78247 is designed to support power−up starting from VBB = 4.5 V.

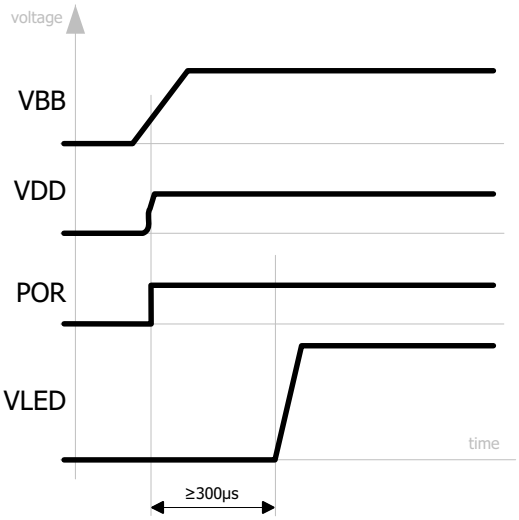


Figure 11. Power−up Sequence

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip and it takes its energy from VBB. VDD supply is foreseen to supply the internal analog and digital circuits. The POR−circuit is monitoring the VBB and VDD voltages.

POR SAFE STATE

All switches are in the OFF−state after POR. The open drain FAIL output remains in high impedance state after the POR until <MAPENA> bit is set to 1 and error flags are cleared.

INTERNAL CLOCK GENERATION

The clocks are fully internally generated without the need for any trimming by the user. The accuracy is guaranteed under full operating conditions and independent of external component selection. This internal clock is used for internal usage and also for the dimming reference if the internal PWM dimming clock is selected.

OSC10M Clock

The OSC10M clock is the system clock. All the internal timings as well as the internal PWM unit depend on OSC10M accuracy.

DIMMING CONTROLLER

Internal (built−in) dimming controller allows change of light intensity of individual LEDs in LED string by means of digital (PWM) dimming.

Dimming Control Parameters

The dimming for all switches is controlled from 1 common 10−bit counter. The ON and OFF events are programmable per channel, each with a 10 bit counter value.

100% duty cycle is generated when ON time is set to min. value (0) and OFF time is set to max value (1023).

0% duty cycle is generated when ON time is equal to OFF time.

Dimming frequency can be brought from internal or external source. The time of one dimming period takes 2^10 = 1024 DIMCLK pulses. The dimming frequency is the DIMCLK frequency divided by 1024. For DIMCLK frequency 1 MHz, the PWM frequency results in 976 Hz.

Dimming Modes

The NCV78247 incorporates two modes of operation – ON/OFF dimming mode and Direct mode.

- ON/OFF dimming mode – the NCV78247 controls the dimming duty cycle and phase shift for each switch individually. The time of ON event is set by means of <ONx[9:0]> register and the time of OFF event is set by means of <OFFx[9:0]> register.
- Direct mode –in addition to ON/OFF dimming mode, the state of the switches can be controlled directly by means of <SWx> register when <TR1[3:0]> = ”1110”

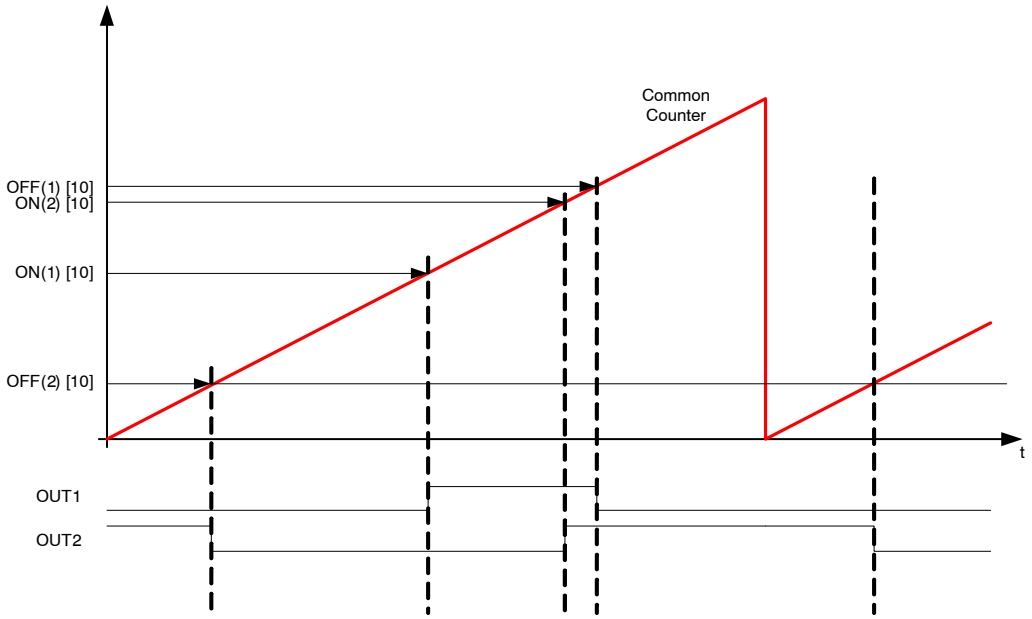


Figure 12. Dimming Operation (dimming ON/OFF event)

Dimming Block Diagram

The dimming shadow registers are loaded with the ON and OFF switching data via the SPI interface.

In ON/OFF dimming mode, the dimming shadow registers are loaded into the dimming controller and all switches change synchronously to the newly programmed ON/OFF times at the end of the actual dimming cycle (when common counter CTR[9:0] overflows, CTR[10] is high).

Note: MAP Enable <MAPENA> bit has to be set to update dimming controller register content from shadow registers.

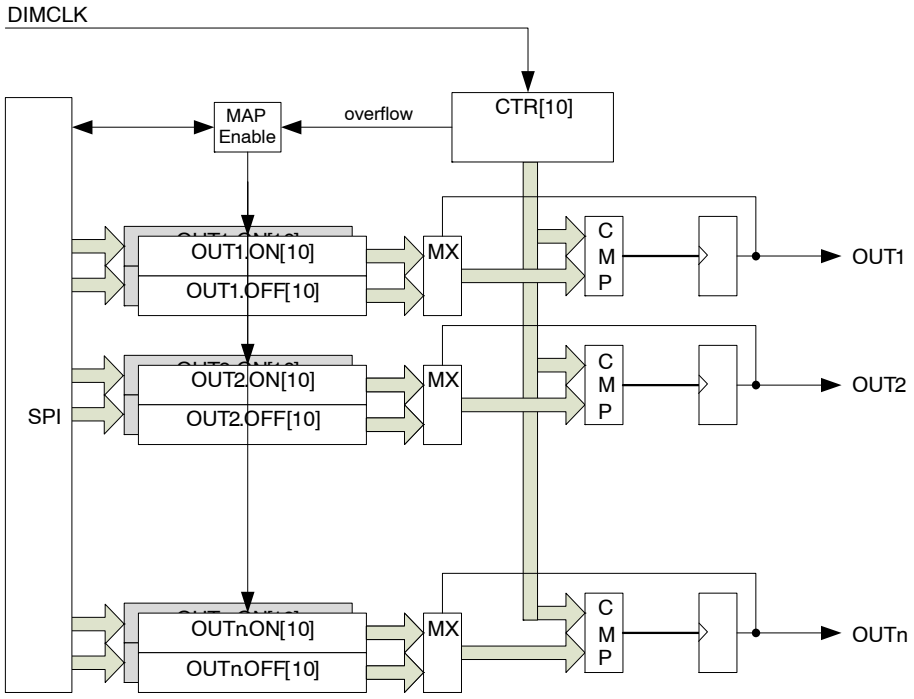


Figure 13. Dimming Block Diagram

Dimming Transition Vector Insertion

Transition Vectors are required in case of pattern changes (update of dimming settings) to avoid multiple switching events at the same time. Transition vector is prolonging the duration of ON or OFF value to the next PWM period by <TRx> x Time slot between switch activations (see Table 7). The example of transient vector insertion is shown on Figure 14. Duty cycle in only one period is affected.

Pattern is updated when common PWM counter overflows (CTR[10] = ‘1’) and <MAPENA> = ‘1’. It can happen that switch on event is required on more switches at the same time. However, overlapping switch on events are forbidden, the NCV78247 needs time slot between switch activations (see Table 7), for this reason Transient Vectors are incorporated. When overlapping multiple switch on events are despite this invoked, the <DIMERR> error is raised causing that all switches are switched off, open drain FAIL output goes to HiZ state and processing of invalid pattern is stopped. When overlapping switch off events occurs, the <DIMWARN> status bit is set and processing of this pattern continues. However, it has to be taken into account, that overlapping switch off events can cause big fluctuations of LED string voltage.

The NCV78247 contains 12 channels, so with unique settings of <TRx[3:0]> for each switch 12 different Transient Vector values are needed in the worst case (“0x0” to “0xB”). When <TRx[3:0]> = ‘0xF’, ‘0xE’, ‘0xD’ or ‘0xC, the <TRx[3:0]> is ignored and transition vectors are not applied. In this case the switch status from previous PWM period is kept unchanged until next ON or OFF event into opposite direction.

Value “0xE” (“1110”) in <TR1[3:0]> register is reserved for entrance into Direct switch control mode (more details in Dimming controller chapter).

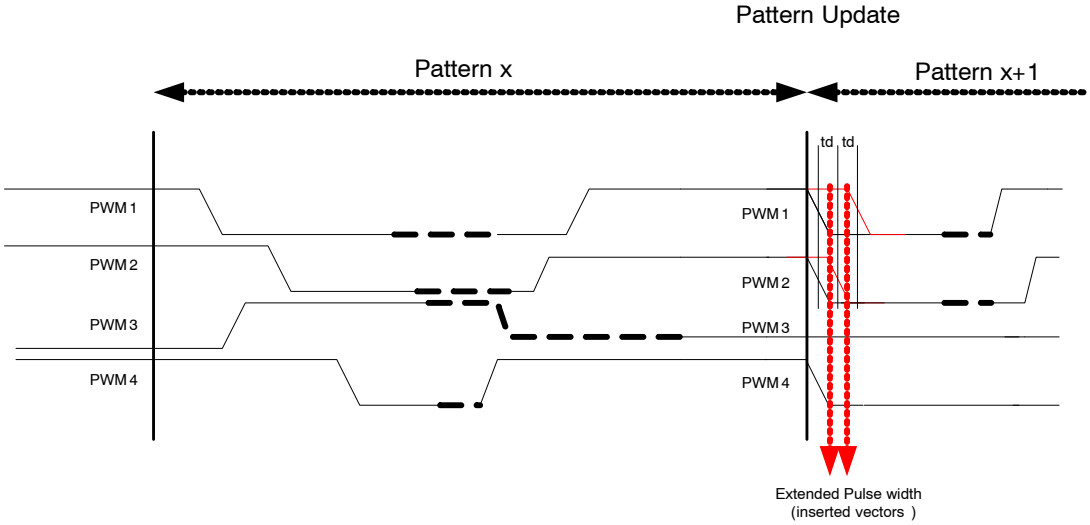


Figure 14. Dimming Transition Vector Insertion in Case of ON/OFF Dimming Mode

PWM dimming clock

Selection of external or internal dimming source is done by means of <DIMSRC> bit in SPI register.

When <DIMSRC> = ‘1’, internal dimming source is selected. When <DIMSRC> = ‘0’, external dimming source is selected.

Default POR value of <DIMSRC> is ‘0’ (external dimming source).

External PWM dimming clock

In case the external dimming source is selected, the pin SYN is configured as a digital input for the dimming clock. The dimming clock frequency can vary from 100 kHz to 1 MHz, providing a dimming frequency between 97 Hz and 976 Hz. Pin SYN is debounced with 100 ns debouncer.

Internal PWM dimming clock

In case the Internal dimming source is selected, the pin SYN is configured as a digital output and makes the dimming clock available for other (slave) devices. The dimming clock frequency can be selected, providing a dimming frequency between 122 Hz and 976 Hz.

<DIMFREQ[2:0]> register shall be used to select between the following dimming frequencies:

- 0x00 – f(PWM) = 122 Hz
- 0x01 – f(PWM) = 244 Hz
- 0x02 – f(PWM) = 488 Hz
- 0x03 – f(PWM) = 976 Hz

Default POR value of <DIMFREQ[2:0]> register is 0x00 (the lowest PWM frequency is selected).

SWITCH CONFIGURATIONS

The 12 integrated switches are typically organized as 12 x 1 switch of 1 A, but can be organized in 6 x 2 switches in parallel to offer 6 x 1 switch of 2 A. Besides that a configuration of two strings of 6 LEDs can be supported, also other variants are possible. Examples of switch configurations are shown on Figure 15.

Selection of the switch configuration is done by <CONF_SEL[3:0]> register. Detailed information about switch configuration is available in Table 9.

Table 9. SWITCH CONFIGURATIONS

CONF_SEL [3:0]	Conf. Code Name	Description
0000	1, 2, 3, 4	12 x PWM channels
0001	1+2, 3, 4	9 x PWM channels(PWM 1=2)
0010	1+2, 3+4	6 x PWM channels (PWM 1=2 & 3=4)
0011	1, 2+3, 4	9 x PWM channels(PWM 2=3)
0100	1, 2, 3+4	9 x PWM channels(PWM 3=4)
0101	1+2+3+4	3 x PWM channels(PWM 1=2=3=4)
0110	1+2+3, 4	6 x PWM channels(PWM 1=2=3)
0111	1, 2+3+4	6 x PWM channels(PWM 2=3=4)
1000	1+4, 2+3	6 x PWM channels (PWM 1=4 & 2=3)
1001	1+4, 2, 3	9 x PWM channels(PWM 1=4)
OTHERS	RESERVED	Same as 0000, 12 x PWM channels

In case of configurations with 2x, 3x, 4x current, PWM signals of sections with higher index are controlled with PWM signals from lower index sections. For example in case of configuration “0101”, which represents 4x current, the PWM signals of section 1 are controlling section 2, 3 and 4; control signals of section 2, 3 and 4 are ignored.

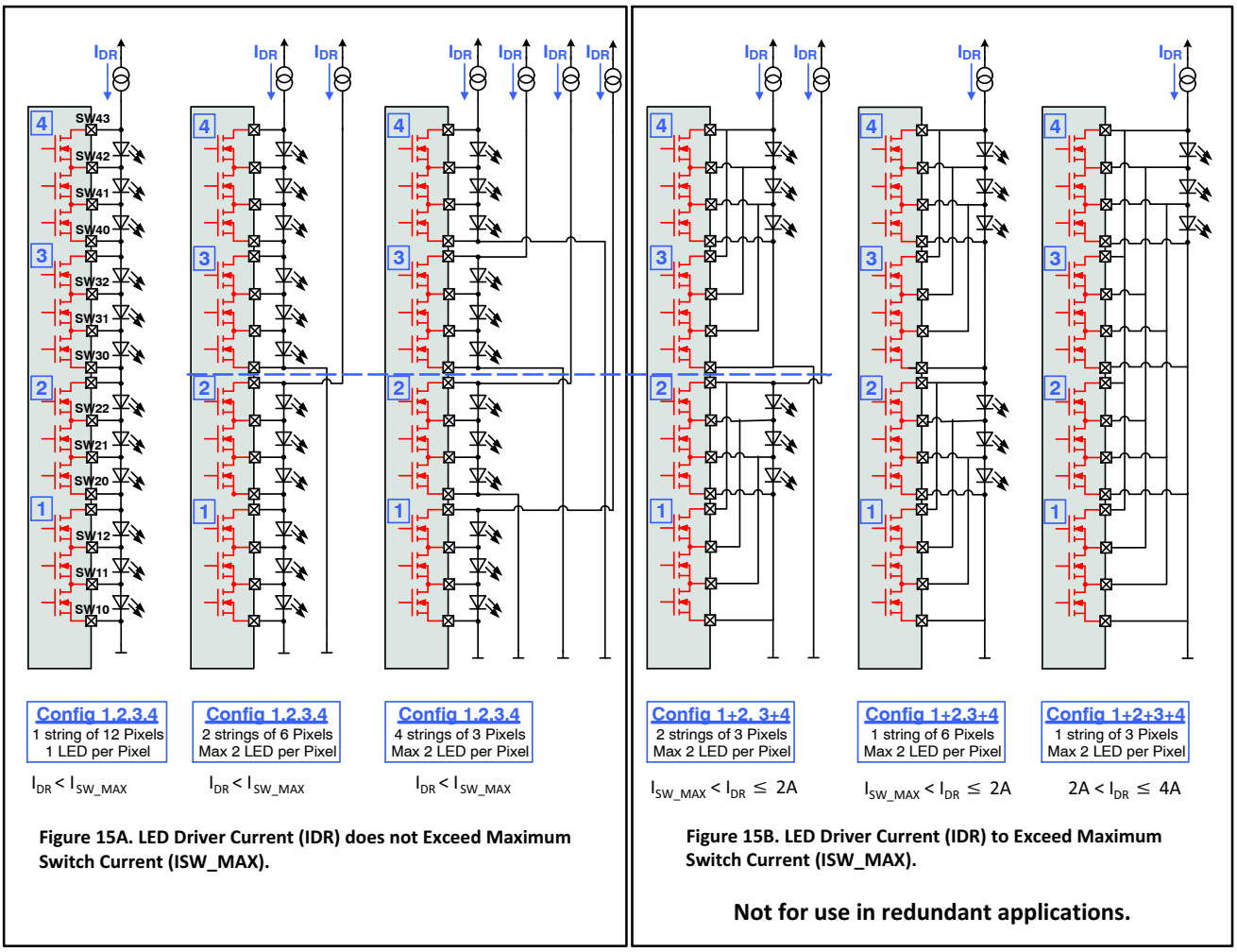


Figure 15A. LED Driver Current (IDR) does not Exceed Maximum Switch Current (ISW_MAX).

Figure 15B. LED Driver Current (IDR) to Exceed Maximum Switch Current (ISW_MAX).

Not for use in redundant applications.

Figure 15. Example of Switch Configurations

PIXEL SWITCHES

Switch ON Process

The switch is gradually opened with a defined slope during T1_CONF[1:0] time.

Short/Open Circuit Detection

Each switch is monitored by a voltage monitor. By monitoring the voltage, and comparing it with the activation status, the following error conditions can be detected:

- Switch OFF and SSH_VTH < V_{SW} < SOV_TH → OK_OFF
- Switch OFF and V_{SW} < SSH_VTH → NOK_SHORT switch is not connected to LED string or switch or LED is shorted.
- Switch OFF and V_{SW} > SOV_TH → NOK_OPEN LED string is opened or LED is broken. Then switch is automatically closed.

During the switching slopes, a blanking time is applied to the above detections of the respective switch in order to avoid false error messages.

The output of the overvoltage comparator is debounced with a debouncing time SOV_DB set by <CMP_DEB> register (see Table 7).

Switch Overvoltage Protection

If the LED pixel voltage is above SOV_TH threshold, the switch is automatically activated and the open switch status is set in the <SWx.STATUS> SPI register. This protects the switch and guarantees that the rest of the LED string still operates properly in case of a LED open failure. Switch is deactivated resp. controllable from PWM again only once open led flag (SWOPN) is cleared by dedicated clear request SPI command. The output of overvoltage comparator is debounced with debouncing time SOV_DB set by <CMP_DEB> register (see Table 7).

FAIL OUTPUT

The open drain FAIL output is forced to GND by the device and goes to HiZ state when the <TSD> is raised or when the device fails to operate (e.g. when V_{DD} supply does not work, etc...) or device is not powered. This guarantees that the LEDs in the LED string are not unintentionally switched on. An external FET must take care that it shorts the full string or that it interrupts the current to the LED string. In the latter case, pre−cautions must be taken to avoid that the self inductance voltage from the current source (typically a buck regulator) does not destroy the circuit.

SPI INTERFACE

SPI interface allows external microcontroller (MCU) to communicate with the device to set and update operating parameters and read−out status information.

The NCV78247 SPI transfer packet size is 32 bit. During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the serial data lines: SDO signal (output from the Slave) and SDI signal (output from Master). If an NCV78247 is not selected by active low slave select line (CSB), SDO is in high impedance state. NCV78247 clocks data out on the falling edge and samples data in on rising edge of CLK clock.

Multiple NCV78247 chips can be connected to MCU by means of star connection (one individual CSB per Slave, while SDI, SDO, CLK are common).

SPI Protocol

Data on SDI and SDO pins are shifted with MSB first. All SPI commands (to SDI pin of NCV78247) from the master consist of one “read and write address byte” (RDADDR[3:0] and WRADDR[3:0]) and three “data bytes” (WRITE_REG_DATA[23:0]).

Each nibble of “read and write address byte”, RDADDR[3:0] and WRADDR[3:0], is pointing to space of 16 registers.

It is possible to write value to a register and read value from another one (or old value of currently written) by one SPI command. Data to be written to WRADDR address are contained in WRITE_REG_DATA[23:0] bytes. Address of data to be read is in RDADDR, data bytes have no meaning in this case.

To perform read−only operation the read−only register (0x0D, 0x0E or 0x0F) has to be selected by WRADDR.

SPI messages sent by NCV78247 to the master consist of “status information” (0x0F.BYTE[6:0]) and parity bit (over the following three data bytes) and three “data bytes” (READ_REG_DATA[23:0]). The data bytes contain content of the register addressed by RDADDR[3:0] in SPI command message. Automatically returned status flags in 1st byte are not cleared. To clear the status flags, register 0x0F has to be read−out explicitly**.**

The <SPIERR> is set when SPI frame contains less than (or more than) expected number of data bits (number of bits other than 32) during active CSB or when SPI CRC error is detected.

SPI Common Address Space

To make possible to update register values in more NCV78247 devices connected in star connection at one time the SPI Common address space feature is included and can be used by means of <CMAENA> bit. When this bit is high, the NCV78247 device accepts the <MAPENA> and <SWENA> bit set to ‘1’ (both or just one of them) also when CSB for the device is not active. How to use this feature is explained in more detail at SPI address map – <CMAENA> bit description.

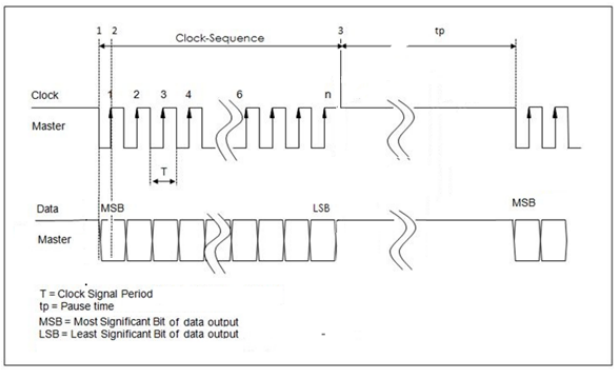


Figure 16. Timing of Common Address Space SPI Operation

When CLK is detected high for time longer then t_p, SPI bit counter is cleared (initialized to 0x00).

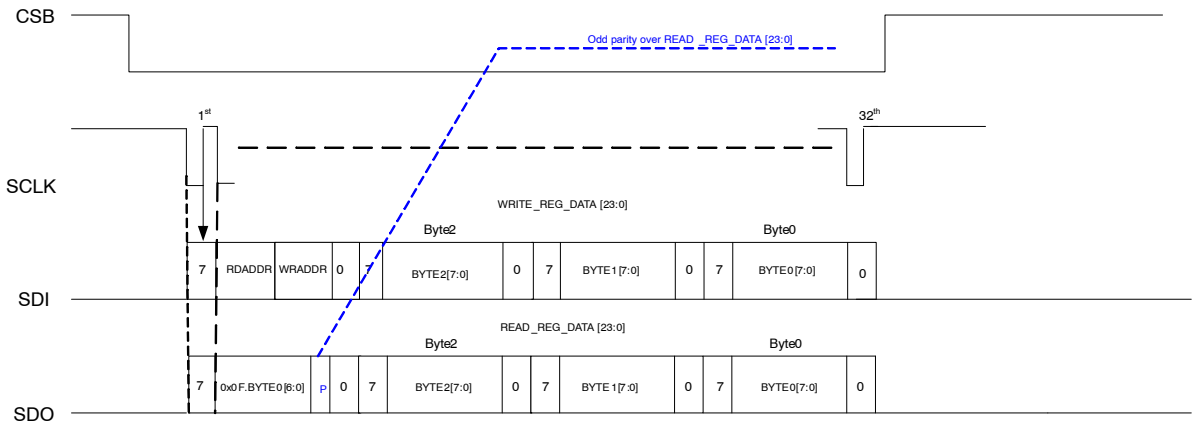


Figure 17. SPI Frame Format

LEGEND:

- RDADDR – SPI Read register address
- WRADDR – SPI Write register address
- WRITE_REG_DATA[23:0] – data to be written into the WRADDR SPI register (data are written into register once rising edge of CSB is detected internally and SPIERR is not detected.
- READ_REG_DATA[23:0] – data read from RDADDR SPI register (READ_REG_DATA[23:0] are captured once reception of bit RDADDR[0] is finished)
- P – parity bit over READ_REG_DATA[23:0]
- 0x0F.BYTE[6:0] – contains HW, SPIERR, DIMERR, DIMWARN, GSWERR, TSD and TW status bits

SPI Address Map

Table 10. SPI ADDRESS MAP

ADDR	R/W	BYTE2[7:0]								BYTE1[7:0]								BYTE0[7:0]							
0x00	R/W	ON1.9	ON1.8	ON1.7	ON1.6	ON1.5	ON1.4	ON1.3	ON1.2	ON1.1	ON1.0	OFF1.9	OFF1.8	OFF1.7	OFF1.6	OFF1.5	OFF1.4	OFF1.3	OFF1.2	OFF1.1	OFF1.0	TR1.3	TR1.2	TR1.1	TR1.0
0x01	R/W	ON2.9	ON2.8	ON2.7	ON2.6	ON2.5	ON2.4	ON2.3	ON2.2	ON2.1	ON2.0	OFF2.9	OFF2.8	OFF2.7	OFF2.6	OFF2.5	OFF2.4	OFF2.3	OFF2.2	OFF2.1	OFF2.0	TR2.3	TR2.2	TR2.1	TR2.0
0x02	R/W	ON3.9	ON3.8	ON3.7	ON3.6	ON3.5	ON3.4	ON3.3	ON3.2	ON3.1	ON3.0	OFF3.9	OFF3.8	OFF3.7	OFF3.6	OFF3.5	OFF3.4	OFF3.3	OFF3.2	OFF3.1	OFF3.0	TR3.3	TR3.2	TR3.1	TR3.0
0x03	R/W	ON4.9	ON4.8	ON4.7	ON4.6	ON4.5	ON4.4	ON4.3	ON4.2	ON4.1	ON4.0	OFF4.9	OFF4.8	OFF4.7	OFF4.6	OFF4.5	OFF4.4	OFF4.3	OFF4.2	OFF4.1	OFF4.0	TR4.3	TR4.2	TR4.1	TR4.0
0x04	R/W	ON5.9	ON5.8	ON5.7	ON5.6	ON5.5	ON5.4	ON5.3	ON5.2	ON5.1	ON5.0	OFF5.9	OFF5.8	OFF5.7	OFF5.6	OFF5.5	OFF5.4	OFF5.3	OFF5.2	OFF5.1	OFF5.0	TR5.3	TR5.2	TR5.1	TR5.0
0x05	R/W	ON6.9	ON6.8	ON6.7	ON6.6	ON6.5	ON6.4	ON6.3	ON6.2	ON6.1	ON6.0	OFF6.9	OFF6.8	OFF6.7	OFF6.6	OFF6.5	OFF6.4	OFF6.3	OFF6.2	OFF6.1	OFF6.0	TR6.3	TR6.2	TR6.1	TR6.0
0x06	R/W	ON7.9	ON7.8	ON7.7	ON7.6	ON7.5	ON7.4	ON7.3	ON7.2	ON7.1	ON7.0	OFF7.9	OFF7.8	OFF7.7	OFF7.6	OFF7.5	OFF7.4	OFF7.3	OFF7.2	OFF7.1	OFF7.0	TR7.3	TR7.2	TR7.1	TR7.0
0x07	R/W	ON8.9	ON8.8	ON8.7	ON8.6	ON8.5	ON8.4	ON8.3	ON8.2	ON8.1	ON8.0	OFF8.9	OFF8.8	OFF8.7	OFF8.6	OFF8.5	OFF8.4	OFF8.3	OFF8.2	OFF8.1	OFF8.0	TR8.3	TR8.2	TR8.1	TR8.0
0x08	R/W	ON9.9	ON9.8	ON9.7	ON9.6	ON9.5	ON9.4	ON9.3	ON9.2	ON9.1	ON9.0	OFF9.9	OFF9.8	OFF9.7	OFF9.6	OFF9.5	OFF9.4	OFF9.3	OFF9.2	OFF9.1	OFF9.0	TR9.3	TR9.2	TR9.1	TR9.0
0x09	R/W	ON10.9	ON10.8	ON10.7	ON10.6	ON10.5	ON10.4	ON10.3	ON10.2	ON10.1	ON10.0	OFF10.9	OFF10.8	OFF10.7	OFF10.6	OFF10.5	OFF10.4	OFF10.3	OFF10.2	OFF10.1	OFF10.0	TR10.3	TR10.2	TR10.1	TR10.0
0x0A	R/W	ON11.9	ON11.8	ON11.7	ON11.6	ON11.5	ON11.4	ON11.3	ON11.2	ON11.1	ON11.0	OFF11.9	OFF11.8	OFF11.7	OFF11.6	OFF11.5	OFF11.4	OFF11.3	OFF11.2	OFF11.1	OFF11.0	TR11.3	TR11.2	TR11.1	TR11.0
0x0B	R/W	ON12.9	ON12.8	ON12.7	ON12.6	ON12.5	ON12.4	ON12.3	ON12.2	ON12.1	ON12.0	OFF12.9	OFF12.8	OFF12.7	OFF12.6	OFF12.5	OFF12.4	OFF12.3	OFF12.2	OFF12.1	OFF12.0	TR12.3	TR12.2	TR12.1	TR12.0
0x0C	R/W	T1_CONF[1:0]		STRING_GND_DET_ENA[3:0]				1	0	CTRL_FAIL_B	CMP_DEB	DIMFREQ[2:0]			TEMP_THR[2:0]			CONF_SEL[3:0]				CMAENA	MAPENA	DIMSRC	SWENA
0x0D	R	SW8.STATUS[2:0]			SW7.STATUS[2:0]			SW6.STATUS[2:0]		SW5.STATUS[2:0]			SW4.STATUS[2:0]			SW3.STATUS[2:0]			SW2.STATUS[2:0]			SW1.STATUS[2:0]		
0x0E	R	0x00								0x00		PWMCNTOVF	TEMPOUT		SW12.STATUS[2:0]			SW11.STATUS[2:0]			SW10.STATUS[2:0]			SW9.STATUS[2:0]	
0x0F	R	REVID7	REVID6	REVID5	REVID4	REVID3	REVID2	REVID1	REVID0	0	SYNCLOSS	CAP_UV	STRING_OV_DET	STRING_GND_LOSS[3:0]				0	HW	SPIERR	DIMERR	DIMWARN	GSWERR	TSD	TW

SPECIAL CASES OF 0x00 REGISTER:

SWx – Direct Control of the Switches

ADDR	R/W	BYTE2[7:0]								BYTE1[7:0]								BYTE0[7:0]							
0x00	R/W	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	SW12	SW11	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	1	1	1	0

SWOPN – Dedicated SWITCH OPEN Flag Clear Request

ADDR	R/W	BYTE2[7:0]								BYTE1[7:0]								BYTE0[7:0]							
0x00	R/W	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Default value of all SPI registers after POR is 0x00 if not specified explicitly.

Switches Mapping

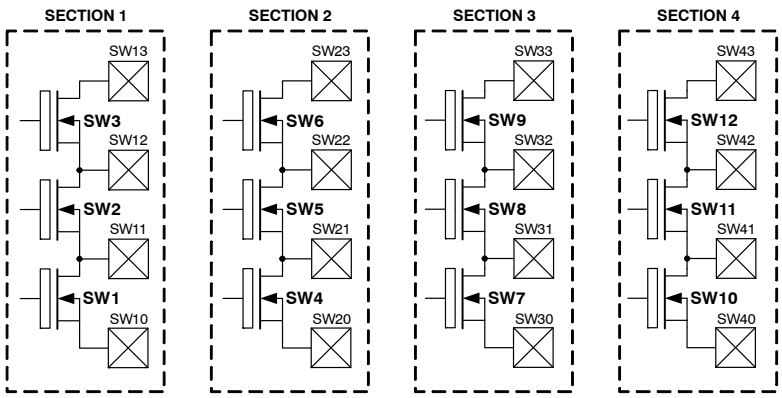


Figure 18. Switches Mapping

Register Description

ONx[9:0] – time of ON event.

OFFx[9:0] – time of OFF event.

TRx[3:0] – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> x Time slot between switch activations (see Table 7). It is applied in case of pixel pattern update (when the common PWM counter overflows (CTR[10] = ‘1’) and <MAP_ENA> = ‘1’). When <TRx[3:0]> = ‘0xF’, ‘0xE’, ‘0xD’ or ‘0xC, the <TRx[3:0]> is ignored and transition vectors are not used. <TRx[3:0]> setting is unique for each switch. Transition vectors are applied only in case of 100% or 0% duty cycle when rising edge is detected on <SWENA> register or when duty cycle change from negative pulse (ON time > OFF time) to positive pulse (ON time < OFF time) resp. from positive pulse (ON time < OFF time) to negative pulse (ON time > OFF time) is detected. If <TRx[3:0]> is not applied, switch status from previous PWM period is kept unchanged until next ON resp. OFF event into opposite direction.

T1_CONF[1:0] – configuration of switch on time.

T1_CONF[0] bit configures the switch soft slope time (slope control), see parameter Switch soft slope time in Table 7).

T1_CONF[1] bit defines the switch on time (switching slope), see parameter Switch on time (switching slope) in Table 7).

Configuring of <T1_CONF[1:0]> register while <SWENA> = ‘1’ should be avoided.

STRING_GND_DET_ENA[3:0] – these bits are enabling/disabling the GND loss detection for the four switch strings. When <STRING_GND_DET_ENA[x]> = ‘1’, GND loss detection is enabled for selected string<x>, otherwise GND loss detection for string<x> is disabled.

CTRL_FAIL_B – when <CTRL_FAIL_B> = ‘0’, open drain FAIL output goes to HiZ state and all switches are switched off and <SWENA> = ‘0’ independently of indicated failures. Open drain FAIL output goes to HiZ state immediately. Forcing of open drain FAIL output to GND is delayed by one full PWM period to avoid LED flickering during start−up or recovery from HW error.

CMP_DEB – defines the over−voltage (SOV_DB) comparator debounce times. Typical debounce time is 10 μs (“0”) and 15 μs (“1”). Configuring of <CMP_DEB> register while <SWENA> = ‘1’ should be avoided.

DIMFREQ[2:0] – defines the DIMCLK frequency when DIMSRC = ‘1’, encoding is as defined below:

0x0 – 125 kHz
0x1 – 250 kHz
0x2 – 500 kHz
0x3 – 1 MHz

<DIMFREQ[2]> is spare, it is reserved for future extensions.

Configuring of <DIMFREQ[2:0]> register while <SWENA> = ‘1’ should be avoided.

TEMP_THR[2:0] – temperature thresholds can be configured via register, encoding is as defined in Table 6.

CONF_SEL[3:0] – selects the switch configuration. NCV78247 supports the switch configurations listed in Table 9.

Update of <CONF_SEL[3:0]> is possible only when <SWENA> = ‘0’.

CMAENA – SPI Common address space enable. When this bit is high, the NCV78247 device accepts the <MAPENA> or <SWENA> bit update also when CSB for the selected device is not active. Only <MAPENA> and <SWENA> bit update in SPI register 0x0C is possible being in SPI Common address space access mode (SPI write operation with inactive CSB and <CMAENA> = ’1’). SDO response is sent only by the device with active CSB (CSB = ’0’). <CMAENA> bit has to be set prior the SPI operation updating the <MAPENA> or <SWENA> bit in SPI Common address space mode.

MAPENA – SPI MAP Enable. When this bit is set and common PWM counter overflow is detected (CTR[9:0] overflows; CTR[10] is high), the bit is cleared and <ONx[9:0]>/<OFF[9:0]>/<TRx[3:0]> SPI registers data are copied into PWM control registers.

DIMSRC – when <DIMSRC> is ’0’, the SYN pin is configured as input and is used as dimming clock source. When <DIMSRC> is ’1’, internally generated clock signal is used as dimming clock (dim. clock freq. is defined by the <DIMFREQ[2:0]> register), SYN pin is configured as output and the clock signal is available on the SYN pin for other (slave) devices.

Configuring of <DIMSRC> register while <SWENA> = ‘1’ should be avoided.

SWENA – when <SWENA> = ’1’, SWx control from PWM logic is enabled. When <SWENA> = ’0’, all switches are switched off, PWM counter (CTR[9:0]) is synchronously reset and SWx dimming control registers (<ONx[9:0]>, <OFFx[9:0]> and <TRx[3:0]>) are cleared.

SWxSTATUS – reflects status of internal SWx flags:

“000” – OFF
“001” – SHORT
“010” – OPEN
“011” – reserved
“100” – reserved
“101” – reserved
“110” – reserved
“111” – ON

PWMCNTOVF – when PWM counter overflows, flag is set to ’1’. It is clear by read flag. It should be used to detect that PWM control (PWM counter) is running/functional.

TEMPOUT – output of temperature comparator (controlled by <TEMPTHR[2:0]>). TEMPOUT is high when Tj is above <TEMP_THR[2:0]>.

REVID[7:0] – NCV78247 revision ID to track silicon mask version.

<REVID[7:4]> – Full Mask Version

<REVID[3:0]> – Metal Mask Version

SYNCLOSS – bit is set when jitter above limit or deviation of dimming clock period is detected on external clock (<DIMSRC> = '0'). Result is debounced over 4 dimming clock periods. Following limits are implemented:

- Jitter limit: ±200 ns (with typical oscillator frequency)
- Frequency limit: > f_{SYN} min value (see Table 4)

The above mentioned processing is performed after <SWENA> rising edge. It is clear by read flag.

CAP_UV – status bit identifying that charging process of external capacitor C2 failed. It is clear by read flag. When this bit is set, the <GSWERR> flag is set to '1', open drain FAIL output goes to HiZ state and all switches are switched off.

STRING_OV_DET – overvoltage detection for four switch strings. It is clear by read flag. When this bit is set, the <GSWERR> flag is set to '1', open drain FAIL output goes to HiZ state and all switches are switched off and <SWENA> bit is cleared.

STRING_GND_LOSS[3:0] – these bits are identifying the GND loss for switch strings<4:1>. When <STRING_GND_DET_LOSS[x]> = '1', the string<x> GND loss was detected, otherwise GND connection for string<x> is OK resp. GND loss detection is disabled by <STRING_GND_DET_ENA[x]>. These flags are cleared by read. When any of these bits is high, the <GSWERR> flag is set to '1', open drain FAIL output goes to HiZ state, all switches are switched off and <SWENA> bit is cleared.

HW – HW flag is set after POR. It is clear by read flag.

SPIERR – SPI framing error (invalid number of CLK pulses detected during frame transfer) or SPI CRC error. It is clear by read flag.

DIMERR – it is set when overlapping ON events are detected during active PWM pattern. When this situation is detected (<DIMERR> status flag is set), open drain FAIL output goes to HiZ state, all switches are switched off, <SWENA> bit is cleared and processing of invalid pattern is stopped. It is clear by read flag.

DIMWARN – It is set when overlapping OFF events are detected during active PWM pattern. Processing of invalid pattern continues. It is also set when SYNCLOSS is detected. It is clear by read flag.

GSWERR – Global SW ERROR flag. <GSWERR> = or_all (<SWx.SHR>) OR or_all (<SWx.OPN>) OR or_all (<SWx.OVC>) OR (<STRING_GND_LOSS[x]> AND <STRING_GND_DET_ENA[x]>)$_{x=<3:0>}$ OR <CAP_UV> OR <STRING_OV_DET>.

TSD – Thermal shutdown flag – when flag is set, open drain FAIL output goes to HiZ state, all switches are switched off and <SWENA> bit is cleared. <TSD> flag is set when T_J above Thermal Shutdown Threshold is detected. It is clear by read flag.

TW – Thermal warning flag. <TW> flag is set when Tj above Thermal Warning Threshold is detected. It is clear by read flag.

CRC[7:0] – cyclic redundancy check over SWC to SW1 when <TR1[3:0]> = "1110". CRC initial seed is 0x9C, CRC polynomial = $x^8 + x^5 + x^4 + x^3 + 1$.

SWx – direct control of the switches when <TR1[3:0]> = "1110".

SWOPN – dedicated SWITCH OPEN flag clear request command has <WRADDR > = 0x00 and <WRITE_REG_DATA[23:0]> = 0x4000C. By sending this command an external MCU may request normal operation of switches automatically closed as OPEN LED bypass <SWx.STATUS> = "010" OPEN. Such switches start to behave accordingly to the ONx, OFFx and TRx setting again.

Warning, Error Detection and Diagnostics Feedback

The NCV78247 offers a wide range of device−integrated diagnostic features. Their description follows.

Thermal Warning and Shutdown

Thermal warning is trimmed in production to 160°C. Thermal Warning (TW) detects a junction temperature which is very close to the Thermal Shutdown level. When Thermal Warning is detected (<TW> = '1'), the SPI register <TW> is set. SPI <TW> register is cleared once it has been read−out by SPI Master.

Thermal shutdown is trimmed in production to 170°C (±5°C). Thermal Shutdown (TSD) detects that a junction temperature has reached the Thermal Shutdown level. When Thermal Shutdown is detected (TSD = '1'), the TSD flag is latched in the SPI <TSD> register and stays set until the SPI <TSD> register is read by the SPI Master and condition for thermal shutdown disappear.

When Thermal Shutdown is detected, open drain FAIL output goes to HiZ state and all switches are switched off. Normal operation is restored when temperature decreases below thermal warning level and <TW> and <TSD> flags are cleared, hereby providing hysteresis for TSD recovery process.

On−chip Temperature Measurement

On top of the TSD and the TW there is available temperature comparator output observable via SPI <TEMPOUT> flag. Temperature thresholds for this comparator can be configured via <TEMP_THR[2:0]> register. All possible settings of temperature thresholds are summarized in Table 6.

SPI Framing Error

The SPIERR is raised when SPI frame contains less than (or more than) expected number of data bits (number of bits other than 32) during active CSB or when SPI CRC error is detected.

Overlapping Switch ON/OFF Events

Overlapping switch on events is forbidden, the NCV78247 needs time slot between two switch on events (see Table 7). Superior system has to ensure that overlapping switch on events do not present in patterns.

When overlapping switch on events are despite this invoked, the NCV78247 incorporates protective feature, in which the <DIMERR> error is raised causing that open drain FAIL output goes to HiZ state, all switches are switched off and processing of invalid pattern is stopped.

When overlapping switch off events occur, the <DIMWARN> status bit is set and processing of this pattern continues. However, it has to be taken into account, that overlapping switch off events can lead to big fluctuations of LED string voltage.

Pixel Switches Diagnostic

Embedded diagnostic covers a wide range of possible failure situations on switches. Each switch contains two comparators – short comparator and over voltage comparator. With the help of these two comparators a several fail situations can be detected and distinguished on each switch individually, for more detail description see chapter PIXEL SWITCHES.

Overall status of switches errors is indicated by Global Switch Error <GSWERR> status flag, which is sent automatically in "status information" section of outgoing messages. When <GSWERR> error is raised, open drain FAIL output goes to HiZ state and all switches are switched off.

Status of individual switches (whether switch is ON or OFF) can be read in Switch Status <SWx.STAT> flag.

The failure state of the individual switches (Short, Open) is indicated by corresponding status in <SW.STATUS[2:0]> register.

String GND Loss

Connection of any of the four LED strings to ground can be checked by means of <STRING_GND_LOSS[3:0]> status register. This detection is enabled by appropriate bit in <STRING_GND_DET_ENA[3:0] register. These flags are cleared by read. When any of these bits is high, the <GSWERR> flag is set to '1', open drain FAIL output goes to HiZ state, all switches are switched off and <SWENA> bit is cleared.

LED String Overvoltage

The device is checking for LED string overvoltage on four switch strings. If overvoltage on any LED string is detected, the < STRING_OV_DET> bit is set. It is cleared by read flag. When this bit is set, the <GSWERR> flag is set to '1', open drain FAIL output goes to HiZ state and all switches are switched off and <SWENA> bit is cleared.

PWMCNTOVF

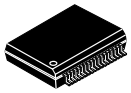
When PWM Counter overflows, <PWMCNTOVF> flag is set to '1'. It is clear by read flag. It should be used to detect that PWM control (PWM counter) is running/functional.

CAP_UV

<CAP_UV> status bit identifies that charging process of external capacitor C2 failed. It is clear by read flag. When this bit is set, the <GSWERR> flag is set to '1', open drain FAIL output goes to HiZ state and all switches are switched off.

Power−on Reset

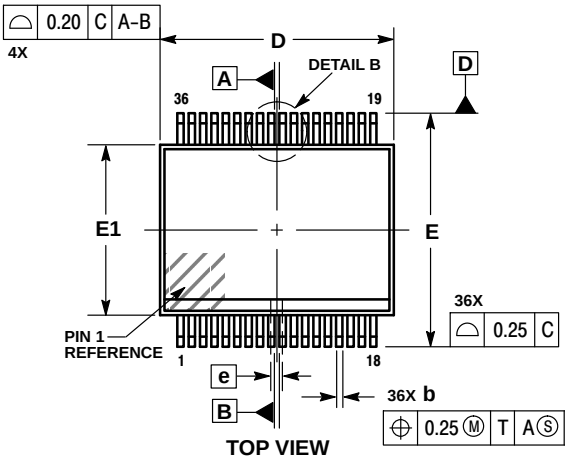
After a power−on a flag <HW> in the SPI register is set.



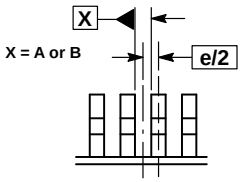
SCALE 1:1

SSOP36 EP
CASE 940AB
ISSUE A

DATE 19 JAN 2016



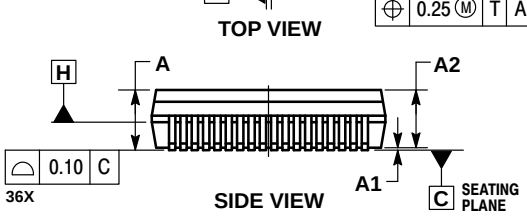
TOP VIEW



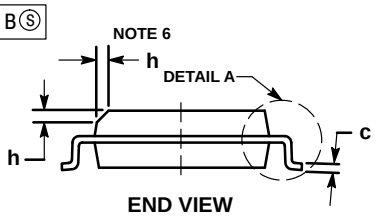
DETAIL B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICATED AREA.

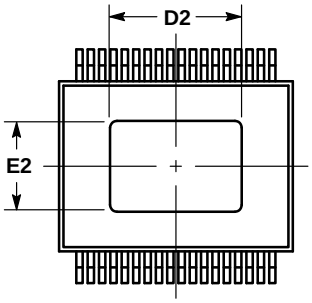
	MILLIMETERS	
DIM	MIN	MAX
A	---	2.65
A1	---	0.10
A2	2.15	2.60
b	0.18	0.30
c	0.23	0.32
D	10.30 BSC	
D2	5.70	5.90
E	10.30 BSC	
E1	7.50 BSC	
E2	3.90	4.10
e	0.50 BSC	
h	0.25	0.75
L	0.50	0.90
L2	0.25 BSC	
M	0°	8°
M1	5°	15°



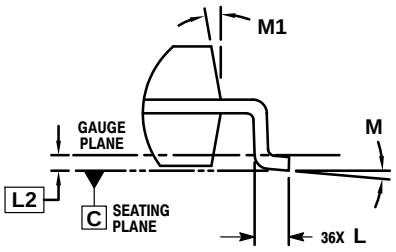
SIDE VIEW



END VIEW

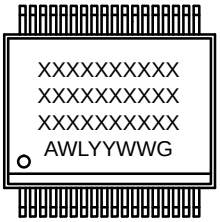


BOTTOM VIEW



DETAIL A

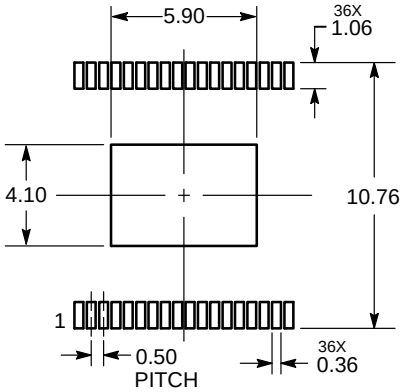
GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON46215E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SSOP36 EXPOSED PAD**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2011

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales