Self-Protected Low Side Driver with Temperature and Current Limit

NCV8401A, NCV8401B

NCV8401A/B is a three terminal protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

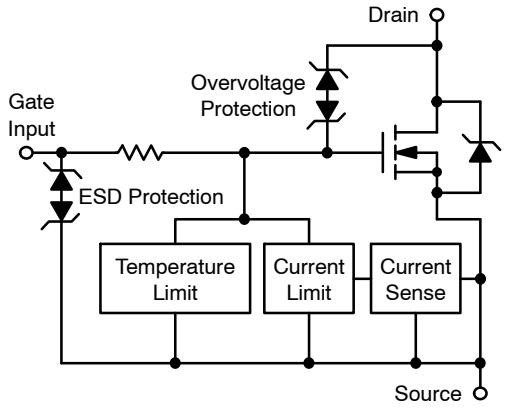
- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

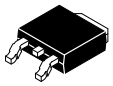
Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

V_{DSS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX (Limited)
42 V	23 mΩ @ 10 V	33 A*

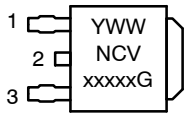
*Max current may be limited below this value depending on input conditions.





DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM



Y	= Year	1	= Gate
WW	= Work Week	2	= Drain
xxxxx	= 8401A or 8401B	3	= Source
G	= Pb−Free Package		

ORDERING INFORMATION

Device	Package	Shipping†
NCV8401BDTRKG	DPAK (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 1)

NCV8401ADTRKG	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

© Semiconductor Components Industries, LLC, 2016

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	V
Drain−to−Gate Voltage Internally Clamped (R_{GS} = 1.0 MΩ)	V_{DGR}	42	V
Gate−to−Source Voltage	V_{GS}	±14	V
Drain Current − Continuous	I_D	Internally Limited	
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.1 2.0	W
Thermal Resistance, Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.6 110 60	°C/W
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 3.65 Apk, L = 120 mH, R_G = 25 Ω, T_{Jstart} = 150°C) (Note 3)	E_{AS}	800	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_I = 2.0 Ω, R_L = 3.0 Ω, t_d = 400 ms)	V_{LD}	65	V
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Minimum FR4 PCB, steady state.
2. Mounted onto a 2″ square FR4 board
   (1″ square, 2 oz. Cu 0.06″ thick single−sided, t = steady state).
3. Not subject to production testing.

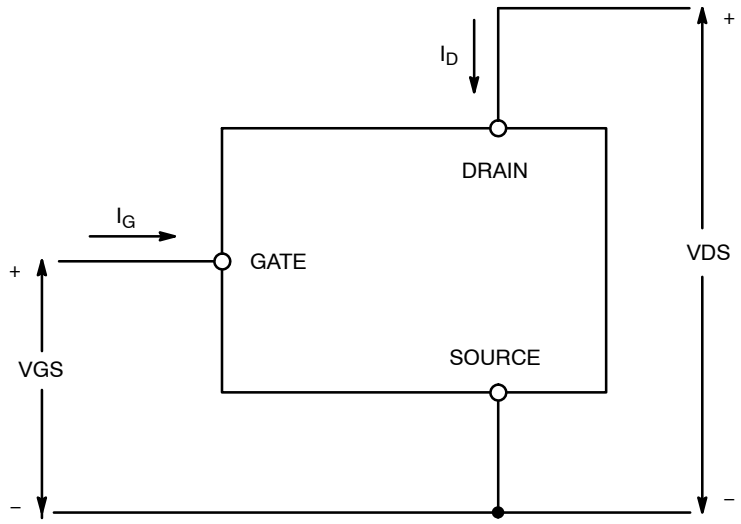


Figure 1. Voltage and Current Convention

Share Feedback
Your Opinion Matters

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = 150°C) (Note 4)	$V_{(BR)DSS}$	 42 42	 46 44	 50 50	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 4)	I_{DSS}	 	 1.5 6.5	 5.0 	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSSF}		50	100	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.2 mAdc) Threshold Temperature Coefficient	$V_{GS(th)}$	1.0	1.8 5.0	2.0	Vdc –mV/°C
Static Drain–to–Source On–Resistance (Note 5) (V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J @ 150°C) (Note 4)	$R_{DS(on)}$	 	 23 43	 29 55	mΩ
Static Drain–to–Source On–Resistance (Note 5) (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J @ 150°C) (Note 4)	$R_{DS(on)}$	 	 28 50	 34 60	mΩ
Source–Drain Forward On Voltage (I_S = 5 A, V_{GS} = 0 V)	V_{SD}		0.80	1.1	V

SWITCHING CHARACTERISTICS (Note 4)

Turn–ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 5 V, V_{DD} = 25 V I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		41	50	μs
Turn–OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		129	150	
Turn–ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 10 V, V_{DD} = 25 V, I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		16	25	
Turn–OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		164	180	
Slew–Rate ON (80% V_{DS} to 50% V_{DS})	V_{in} = 0 to 10 V, V_{DD} = 12 V, R_L = 4.7 Ω	$-dV_{DS}/dt_{ON}$		1.27	2.0	V/μs
Slew–Rate OFF (50% V_{DS} to 80% V_{DS})		dV_{DS}/dt_{OFF}		0.36	0.75	

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Current Limit	V_{GS} = 5.0 V, V_{DS} = 10 V V_{GS} = 5.0 V, T_J = 150°C (Notes 4, 6)	I_{LIM}	25 11	30 16	35 21	Adc
	V_{GS} = 10 V, V_{DS} = 10 V V_{GS} = 10 V, T_J = 150°C (Notes 4, 6)		30 18	35 25	40 28	
Temperature Limit (Turn–off)	V_{GS} = 5.0 V (Notes 4, 6)	$T_{LIM(off)}$	150	175	200	°C
Thermal Hysteresis	V_{GS} = 5.0 V	$\Delta T_{LIM(on)}$		15		°C
Temperature Limit (Turn–off)	V_{GS} = 10 V (Notes 4, 6)	$T_{LIM(off)}$	150	165	185	°C
Thermal Hysteresis	V_{GS} = 10 V	$\Delta T_{LIM(on)}$		15		°C

GATE INPUT CHARACTERISTICS (Note 4)

Device ON Gate Input Current	V_{GS} = 5 V I_D = 1.0 A	I_{GON}		50	100	μA
	V_{GS} = 10 V I_D = 1.0 A			400	700	
Current Limit Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GCL}		0.1	0.5	mA
	V_{GS} = 10 V, V_{DS} = 10 V			0.7	1.0	
Thermal Limit Fault Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GTL}		0.6	1.0	mA
	V_{GS} = 10 V, V_{DS} = 10 V			2.0	4.0	

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 4)

Electro–Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	 4000 400			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Not subject to production testing.
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

Share Feedback
Your Opinion Matters

TYPICAL PERFORMANCE CURVES

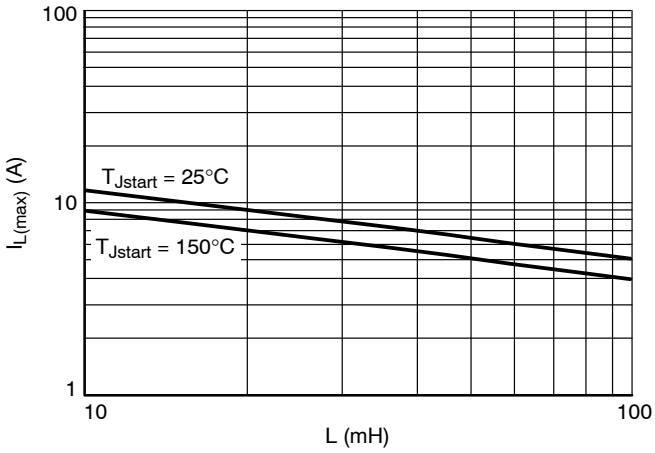


Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance

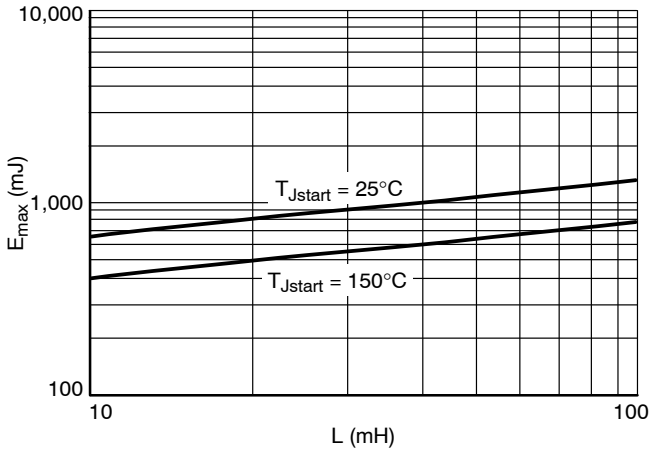


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

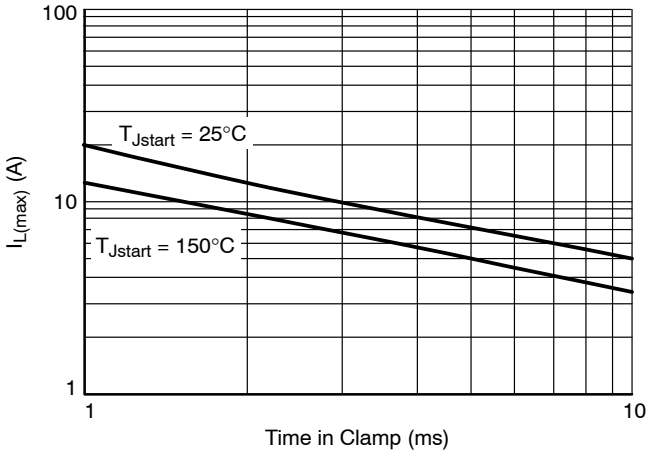


Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp

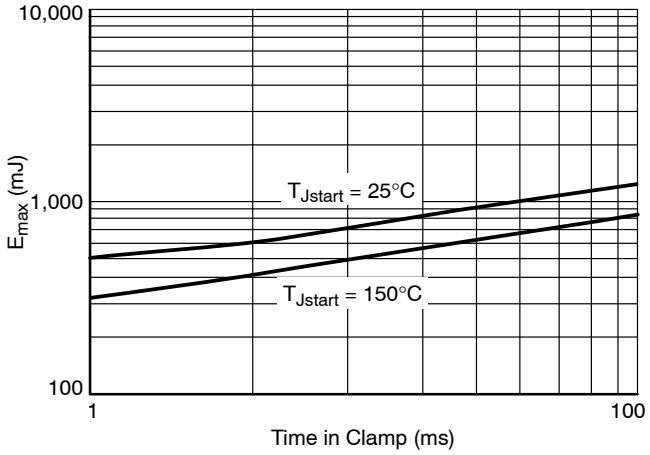


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

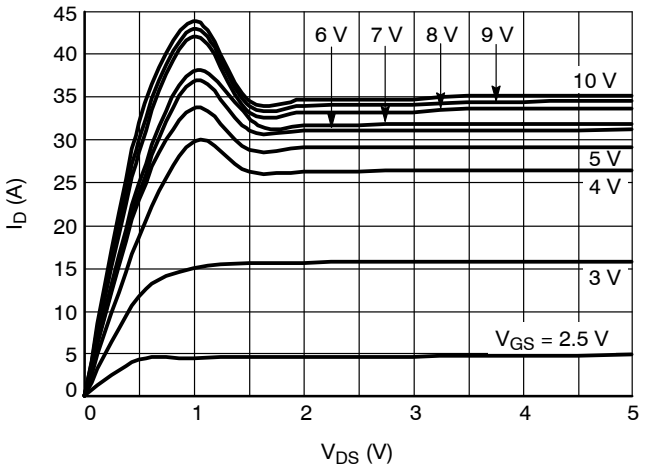


Figure 6. On−state Output Characteristics at 25°C

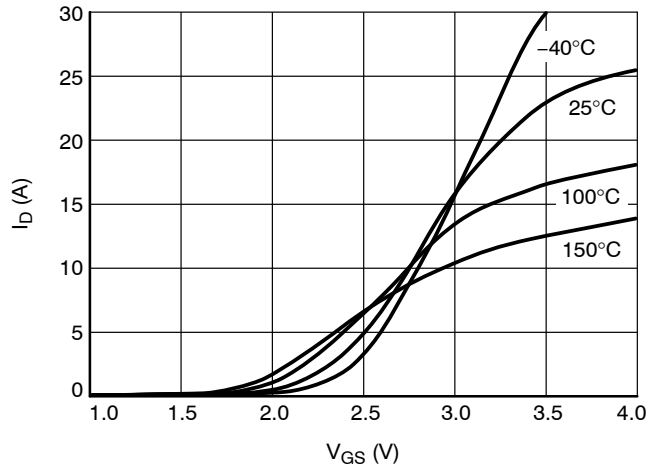


Figure 7. Transfer Characteristics (V_{DS} = 10 V)

Share Feedback
Your Opinion Matters

TYPICAL PERFORMANCE CURVES

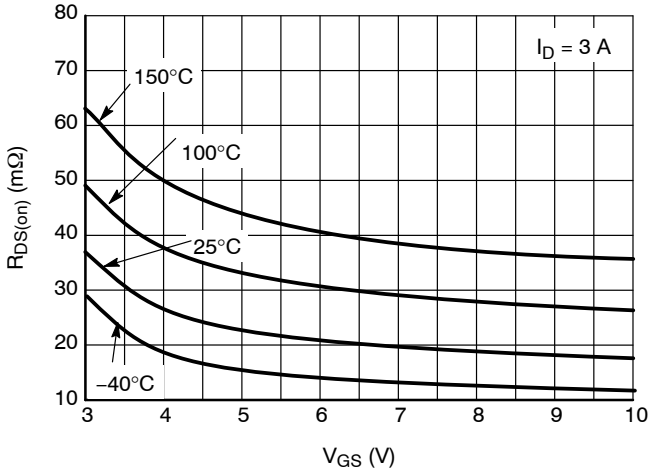


Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage

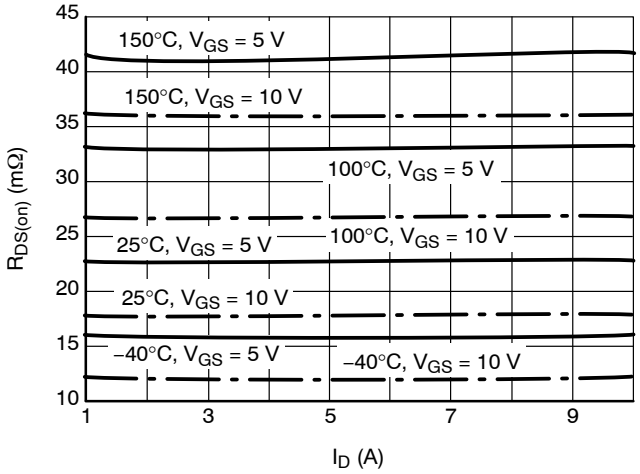


Figure 9. $R_{DS(on)}$ vs. Drain Current

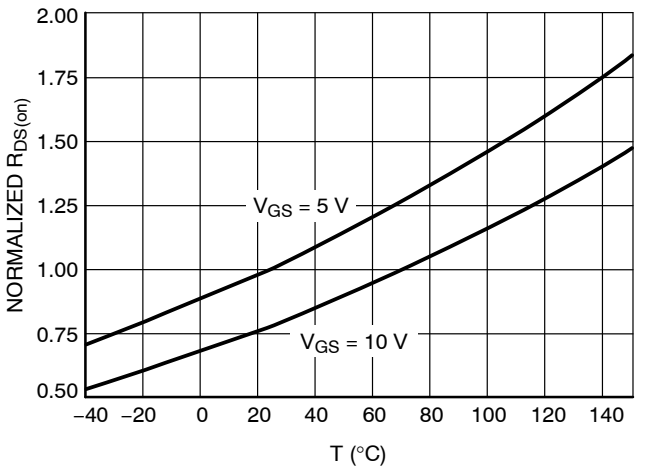


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature (I_D = 5 A)

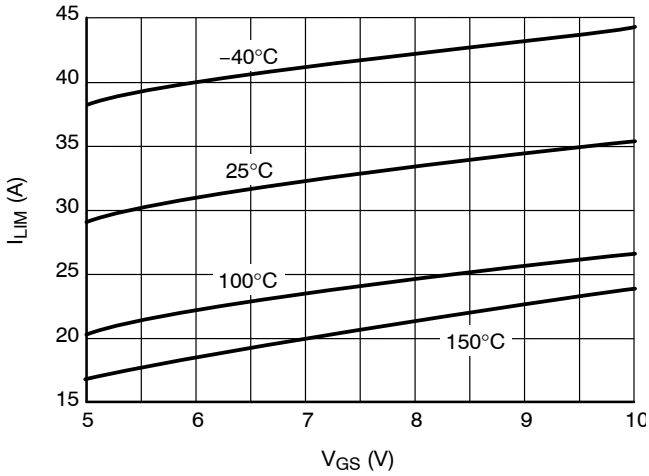


Figure 11. Current Limit vs. Gate−Source Voltage (V_{DS} = 10 V)

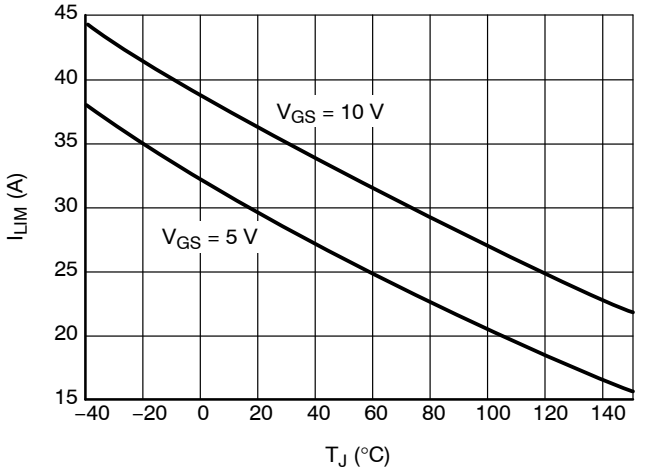


Figure 12. Current Limit vs. Junction Temperature (V_{DS} = 10 V)

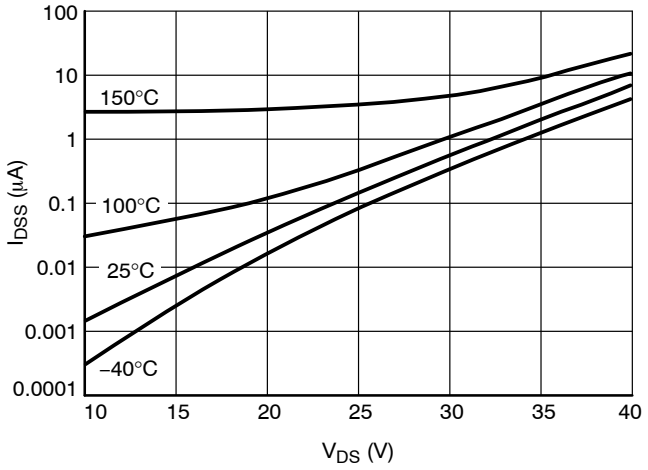


Figure 13. Drain−to−Source Leakage Current (V_{GS} = 0 V)

Share Feedback
Your Opinion Matters

TYPICAL PERFORMANCE CURVES

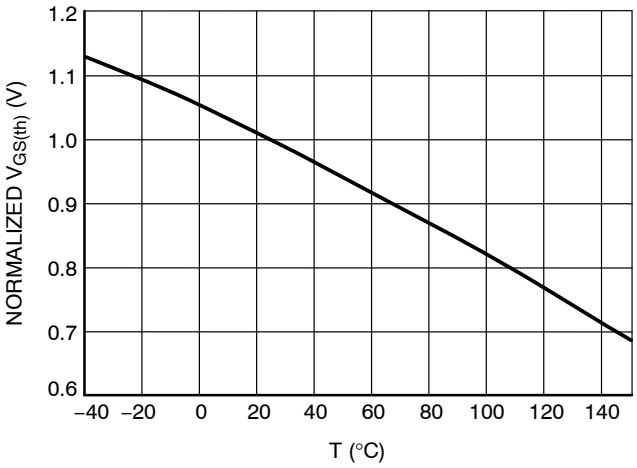


Figure 14. Normalized Threshold Voltage vs. Temperature (I_D = 1.2 mA, V_{DS} = V_{GS})

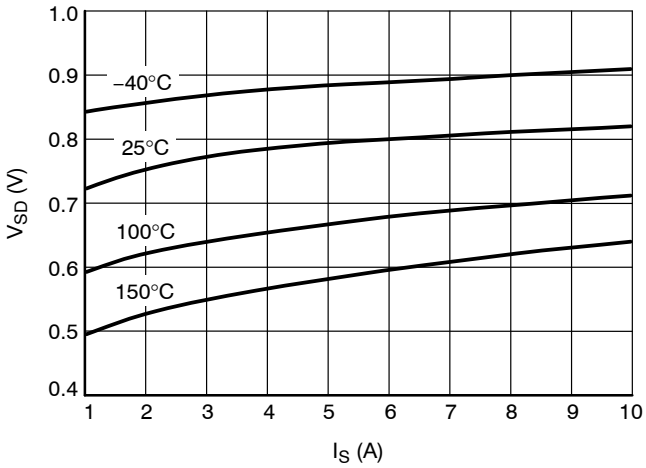


Figure 15. Source−Drain Diode Forward Characteristics (V_{GS} = 0 V)

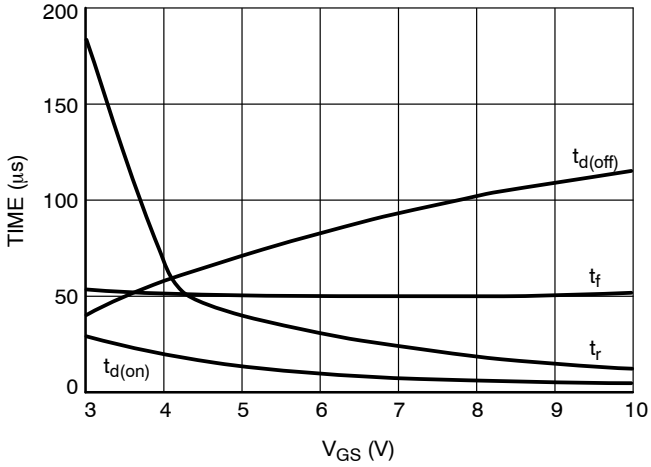


Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage (V_{DD} = 25 V, I_D = 5 A, R_G = 0 Ω)

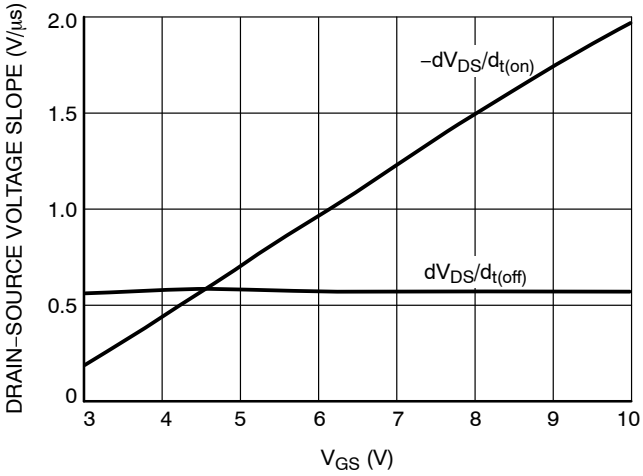


Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage (V_{DD} = 25 V, I_D = 5 A, R_G = 0 Ω)

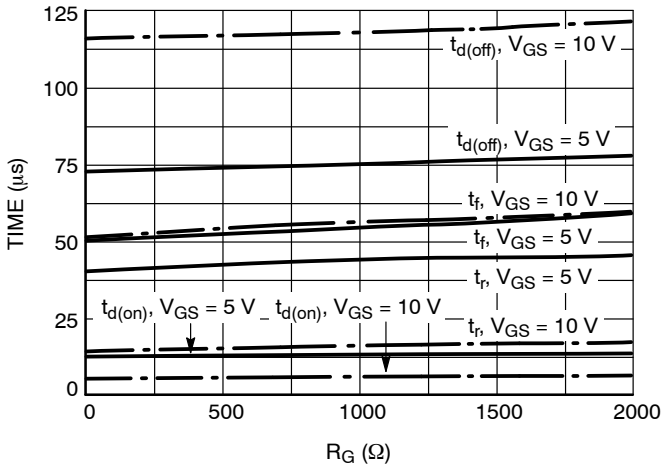


Figure 18. Resistive Load Switching Time vs. Gate Resistance (V_{DD} = 25 V, I_D = 5 A)

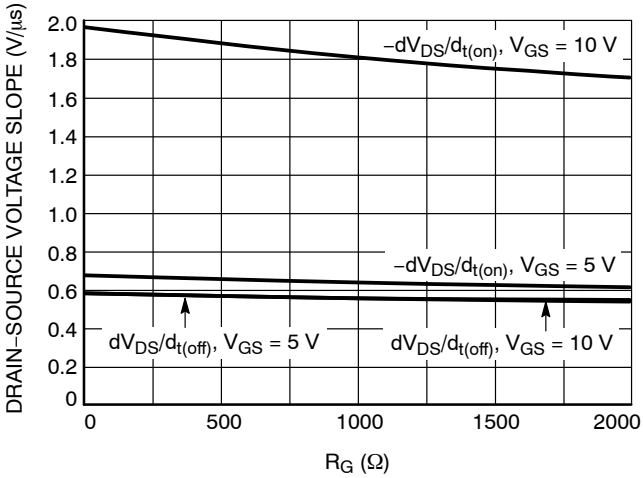


Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance (V_{DD} = 25 V, I_D = 5 A)

Share Feedback
Your Opinion Matters

TYPICAL PERFORMANCE CURVES

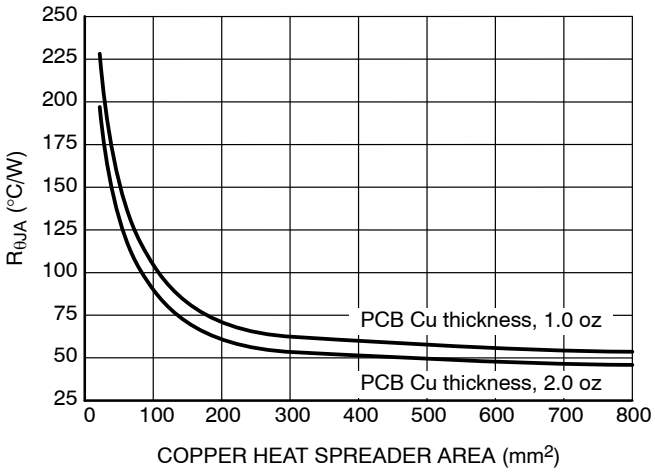


Figure 20. $R_{\theta JA}$ vs. Copper Area

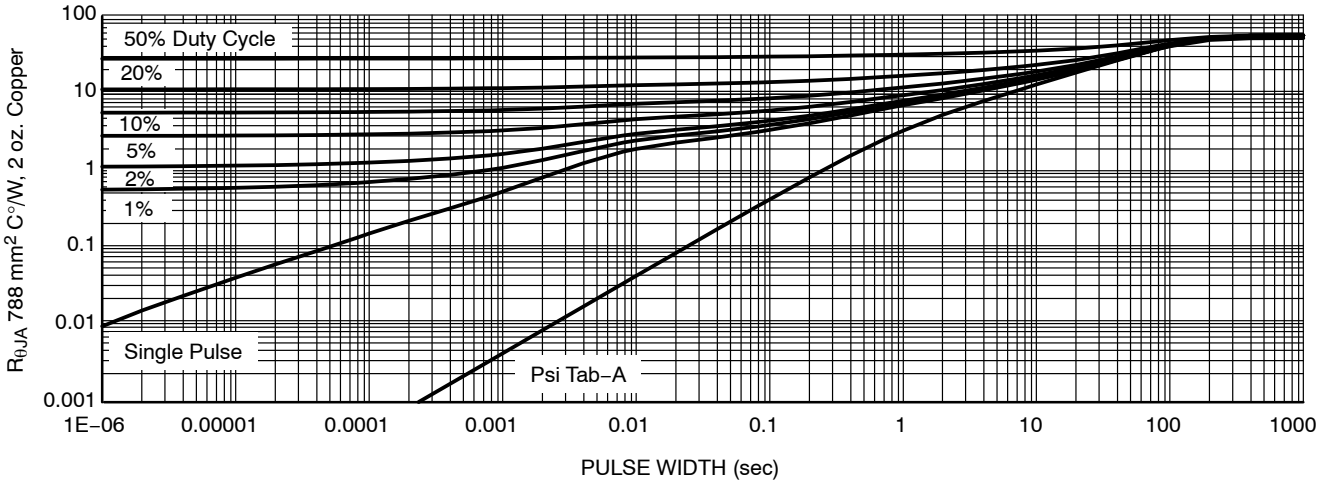


Figure 21. Transient Thermal Resistance

Share Feedback
Your Opinion Matters

TEST CIRCUITS AND WAVEFORMS

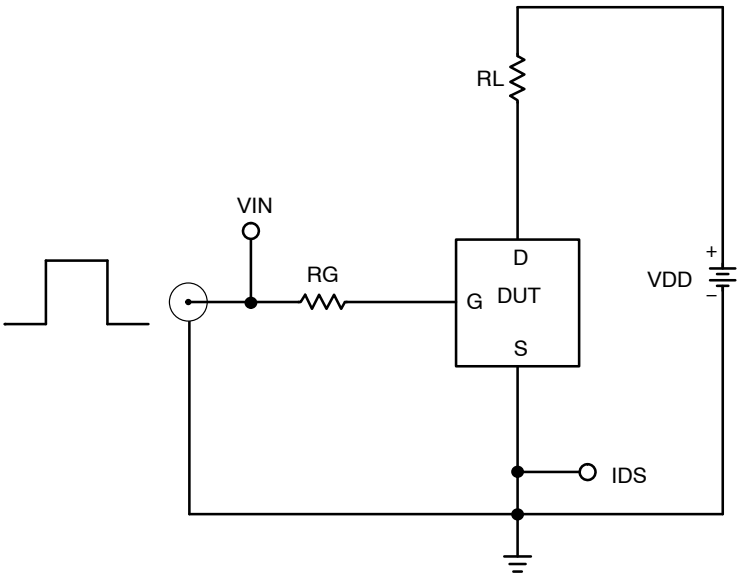


Figure 22. Resistive Load Switching Test Circuit

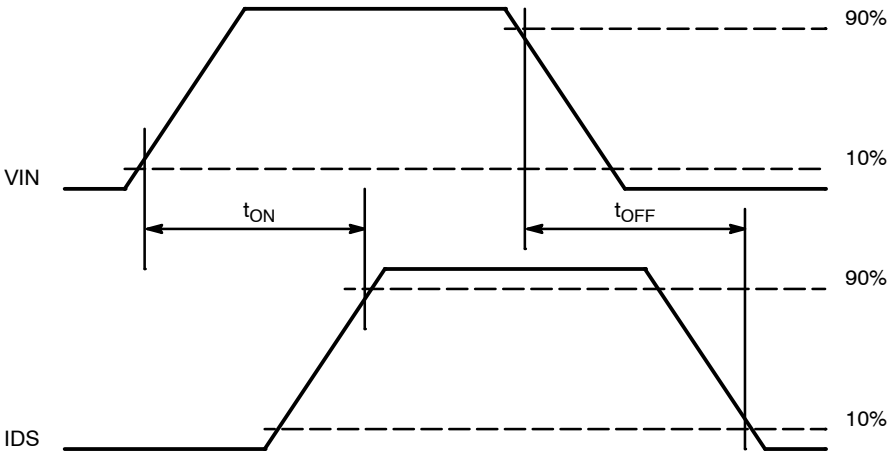


Figure 23. Resistive Load Switching Waveforms

Share Feedback
Your Opinion Matters

TEST CIRCUITS AND WAVEFORMS

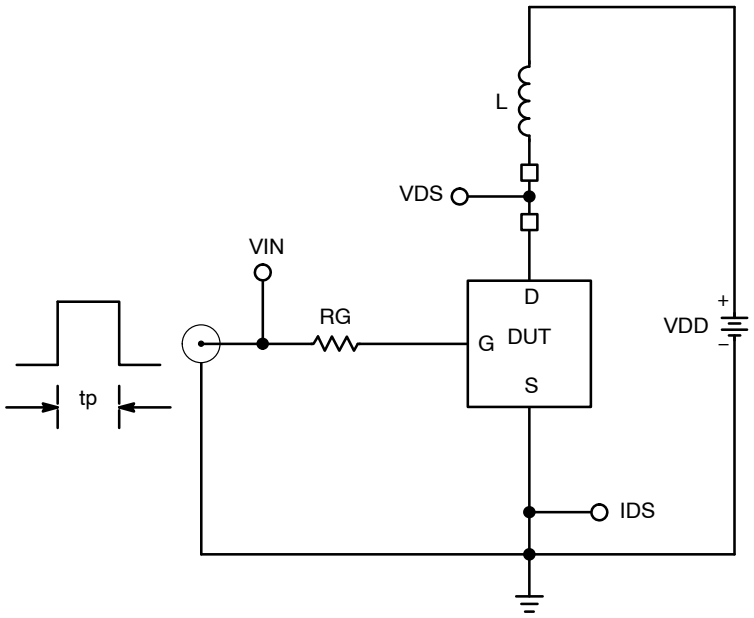


Figure 24. Inductive Load Switching Test Circuit

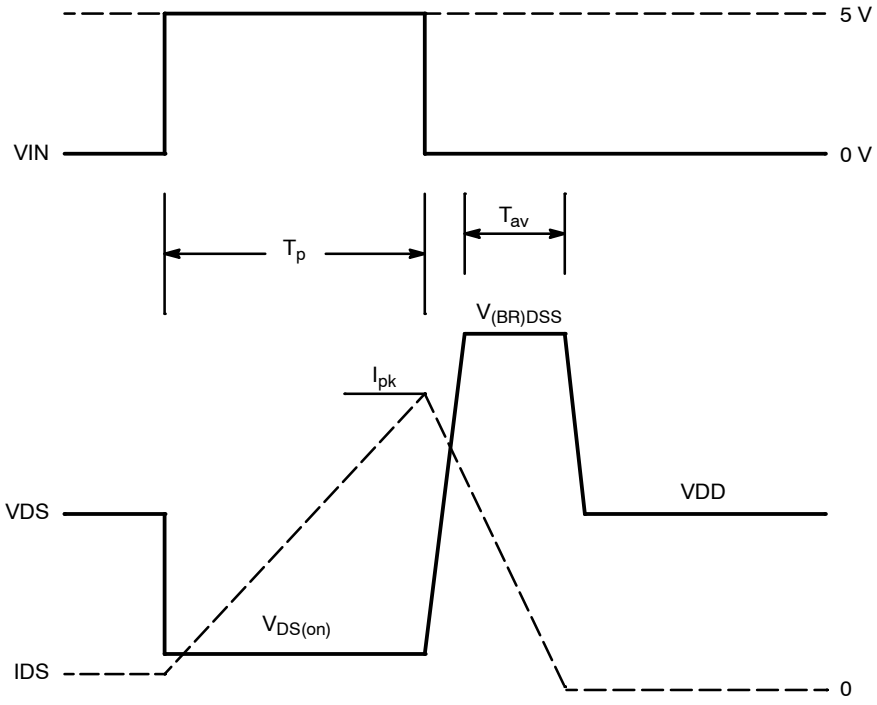
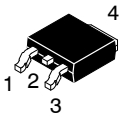


Figure 25. Inductive Load Switching Waveforms

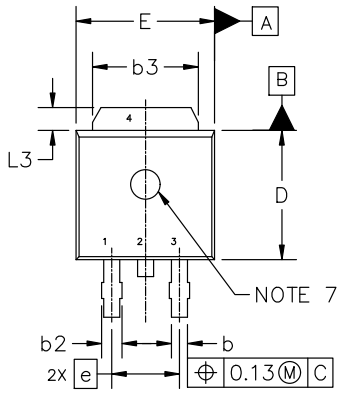
Share Feedback
Your Opinion Matters



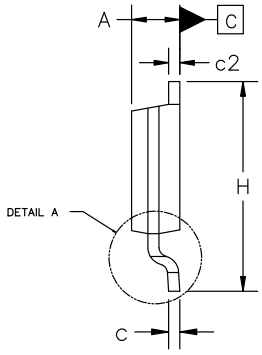
DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

SCALE 1:1

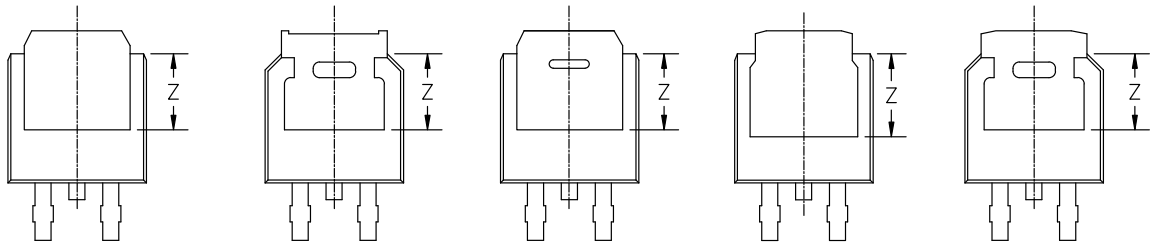


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−

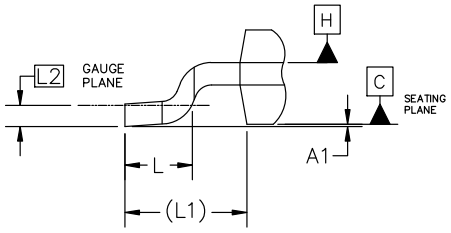


BOTTOM VIEW

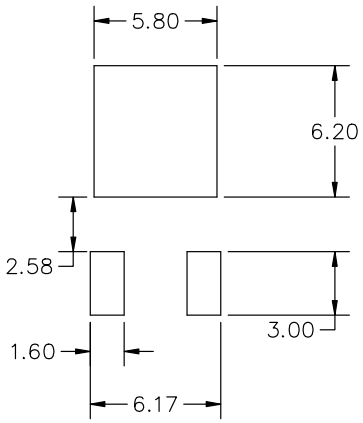
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

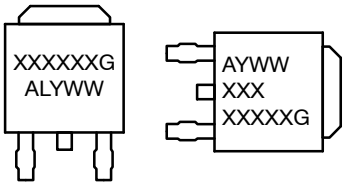
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2011

DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 13 MAY 2026

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2011

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales