High Voltage Linear Regulator
65 V, 100 mA

Product Preview

NCV8737

The NCV8737 is a high−voltage tolerant linear regulator that offers the benefits of thermally enhanced MSOP8 EP and DFNW8 3x3 (on request) packages and is able to withstand continuous DC or transient input voltages up to 65 V with Ultra−low Quiescent Current below 5 μA. The device is stable with small 1 μF Ceramic Output Capacitors which allows smaller PCB design. The devices features enable pin compatible with standard CMOS logic, internal power good circuit with a user programmable delay via external capacitor. The active high output of power good has open drain with internal current limitation.

Features

- Wide Input Voltage Range: 3 V to 65 V
- Output Voltage Versions:
  - Fixed: 3.3 V (other versions on request)
  - Adjustable: from 1.2 V up to 20.0 V
- ±0.5% Accuracy at T_J = 25°C
- Very Low Quiescent Current: 5 μA typ.
- Standby Current: 0.5 μA typ.
- Stable with 1 μF Ceramic Output Capacitor
- Power Good with Programmable Delay
- Thermal Shutdown and Current Limit Protection
- Built−in Soft Start Circuit to Suppress Inrush Current
- Available in Thermally Enhanced MSOP8 EP and DFNW8 3x3 (on request) Packages
- Output Active Discharge Functions
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−free Devices

Typical Applications

- Body Control and Sensor Modules
- On Board Charger
- Infotainment and Audio Systems
- General Purpose Automotive

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAMS

MSOP8 EP 3x3
(DN SUFFIX)
CASE 846AT

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

On Request

DFNW8 3x3
(ML SUFFIX)
CASE 507AD

XXXXX = Specific Device Marking
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

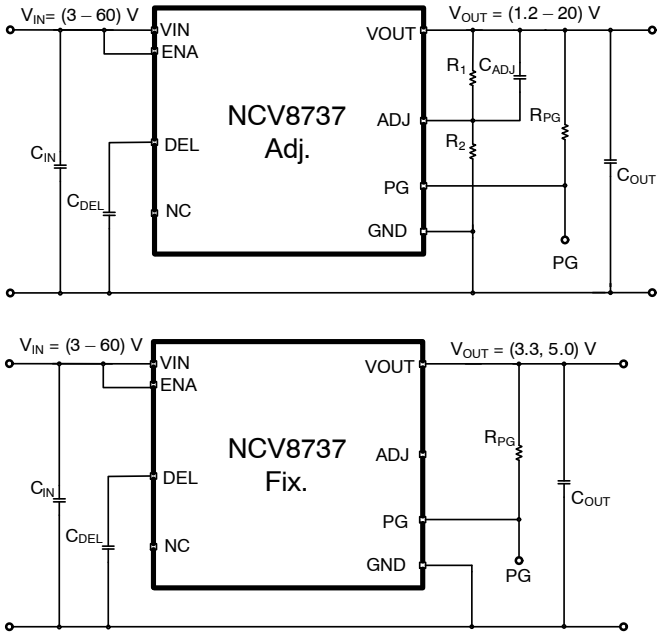


Figure 1. Typical Application Schematics

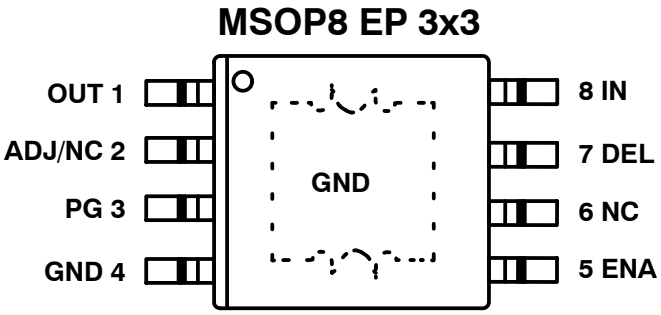


Figure 2. Pin Connections (Top view)

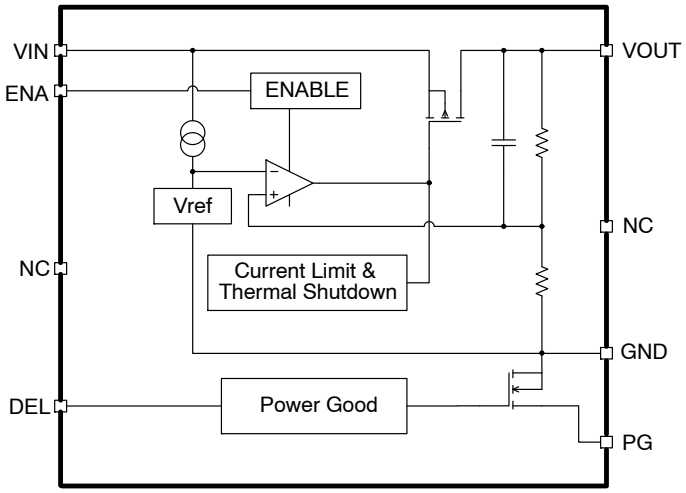


Figure 3. Simplified Block Diagram for Fixed V_{OUT} Options

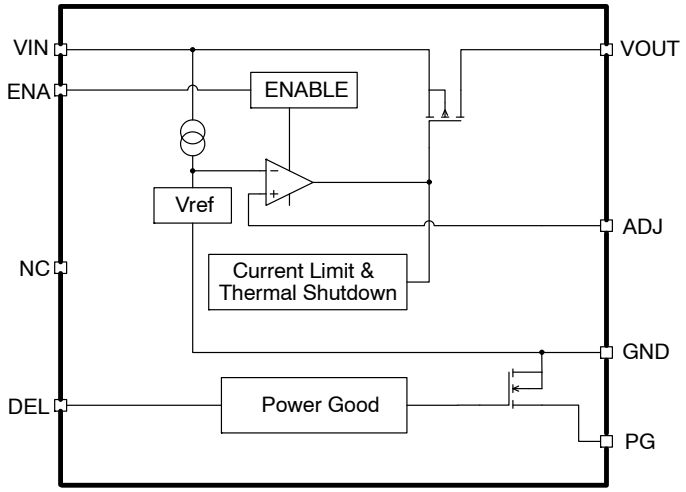


Figure 4. Simplified Block Diagram for Adjustable V_{OUT} Options

Table 1. PIN FUNCTION DESCRIPTION

Pin No. WDFNW8 3x3	Pin No. MSOP8−EP	Pin Name	Description
1	1	OUT	Regulator output pin. A capacitor ≥ 1 μF (effective) must be connected from this pin to GND to assure stability.
2	2	ADJ/NC	This pin is used for adjustable version to set the output voltage by external resistor divider. For fixed voltage versions leave this pin floating.
3	3	PG	Power good output pin. High−Z level for power ok, low level for fail. If not used, could be left unconnected or shorted to GND.
4	4	GND	Power supply ground pin.
5	5	ENA	Chip enable pin (active “H”). Do not leave this pin floating.
6	6	NC	Not connected pin. Leave this pin floating or connect to GND.
7	7	DEL	PG delay pin. Connect a capacitor to GND to adjust the PG delay time. Leave this pin floating if the function is not used.
8	8	IN	Power supply input pin.
EP	EP	EP	Exposed pad. Must be connected to GND potential.

Table 2. ABSOLUTE MAXIMUM RATING

Ratings		Symbol	Value	Unit
IN Pin Voltage Range (Note 1)		V_{IN}	−0.3 to 70	V
OUT Pin Voltage Range	ADJ Version	V_{OUT}	−0.3 to [(V_{IN} + 0.3) or 70; whichever is lower]	V
	FIX Versions		−0.3 to [(V_{IN} + 0.3) or (3 × $V_{OUT-NOM}$); whichever is lower]	
EN Pin Voltage Range		V_{ENA}	−0.3 to (Vin + 0.3) V	V
ADJ Pin Voltage Range		V_{ADJ}	−0.3 to 3.6	V
DEL Pin Voltage Range		V_{DEL}	−0.3 to 3.6	V
PG Pin Voltage Range		V_{PG}	−0.3 to (V_{in} + 0.3)	V
PG Pin Current		I_{PG}	5	mA
DEL Pin Current		I_{DEL}	5	μA
Maximum Junction Temperature		$T_{J(max)}$	150	°C
Storage Temperature Range		T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}	1	kV
Moisture Sensitivity Level		MSL	TBD	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)		T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: Pin voltages are related to GND pin.

1. Refer to ELECTRICAL CHARACTERISTIC and APPLICATION INFORMATION for Safe operating Area
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS − 002, EIA/JESD22 − C101 (AEC Q100 − 011D)
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 4)

Characteristic	Symbol	MSOP−8	DFNW8 3x3	Unit
Thermal Resistance, Junction−to−Air	R_{thJA}	38.7	35.4	°C/W
Thermal Resistance, Junction−to−Case (top)	R_{thJCt}	102.0	87.3	°C/W
Thermal Resistance, Junction−to−Case (bottom)	R_{thJCb}	14.7	10.3	°C/W
Thermal Resistance, Junction−to−Board (top)	R_{thJBt}	15.2	10.1	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Psi_{JCt}	10.3	7.4	°C/W
Thermal Characterization Parameter, Junction−to−Board [FEM]	Psi_{JB}	15.5	10.2	°C/W

4. Measured according to JEDEC board specification (board 2S2P, Cu layer thickness 1 oz, Cu area 645 mm^2, no airflow). Detailed description of the board can be found in JESD51−7.

Table 3. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 150°C$; $V_{IN} = V_{OUTNOM} + 0.5$ V or 3.0 V (whichever is greater), $I_{OUT} = 10$ μA, $C_{IN} = 1$ μF, $C_{OUT} = 1$ μF (Note 5), ADJ pin connected to V_{OUT} pin, unless otherwise noted. Typical values are at $T_A = +25°C$. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT						
Operating Input Voltage		V_{IN}	3	–	65	V
OUTPUT						
Output Voltage Accuracy (Note 7)	$T_J = 25°C$	V_{OUT}	−0.5	V_{NOM25}	0.5	%
Output Voltage Accuracy (Note 7)	$T_J = -40°C$ to 125°C		−1.5	–	1.5	
	$T_J = -40°C$ to 150°C		−2	–	1.5	
ADJ Reference Voltage	ADJ version only	V_{ADJ}	–	1.2	–	V
ADJ Input Current	ADJ version only, $V_{ADJ} = 1.2$ V	I_{ADJ}	−100	10	100	nA
Output Voltage Range	ADJ version only	$V_{OUT-ADJ}$	V_{ADJ}	–	20	V
Line Regulation	$V_{IN} = (V_{OUT-NOM} + 0.5$ V) to 65 V, $V_{IN} \ge 3.0$ V	$\Delta V_O/\Delta V_I$	–	0.01	0.2	$\%V_{OUT}$
Load Regulation	$I_{OUT} = 10$ μA to 100 mA	$\Delta V_O/\Delta I_O$	–	0.1	0.4	$\%V_{OUT}$
Dropout Voltage	$I_{OUT} = 100$ mA, all $V_{OUT-NOM}$ versions		–	265	600	mV
Output Current Limit	$V_{OUT-FORCED} = V_{OUT-NOM} - 100$ mV	I_{OLIM}	100	200	300	mA
Short Circuit Current	$V_{OUT} = 0$ V	I_{OSC}	100	200	300	
Active Discharge Resistance	$V_{EN} = 0$V	$R_{ACT-DIS}$	–	50	–	Ω
CURRENT CONSUMPTION						
Disable Current	$V_{EN} = 0$ V, $V_{IN} = (V_{OUT-NOM} + 0.5$ V) to 65 V, $V_{IN} \ge 3.0$ V	I_{DIS}	–	0.5	5	μA
Quiescent Current	$I_{OUT} = 0$ mA, $V_{IN} = (V_{OUT-NOM} + 0.5$ V) to 65 V, $V_{IN} \ge 3.0$ V	I_Q	–	5	15	μA
Ground Current	$I_{OUT} = 100$ mA	I_{GND}	–	300	500	μA
ENABLE THRESHOLDS						
Enable Input Threshold Voltage	$V_{IN} = V_{OUTNOM} + 0.5$ V	V_{ENA}				V
Voltage Increasing, Logic High	High		1.2	–	–	
Voltage Decreasing, Logic Low	Low		–	–	0.3	
Enable pin current	$V_{EN} \le 60$ V	I_{EN}	–	0.1	1	μA
PSRR AND NOISE						
Power Supply Ripple Rejection	$V_{OUT} = 3.3$ V (ADJ), $C_{FF} = 10$ nF, $C_{OUT} = 2.2$ μF, $I_{OUT} = 100$ mA	PSRR				dB
	f = 100 Hz, 0.1 V_{p-p}		–	77	–	
	f = 1 kHz, 0.1 V_{p-p}		–	73	–	
	f = 100 kHz, 0.1 V_{p-p}		–	30	–	

Table 3. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 150°C$; $V_{IN} = V_{OUTNOM} + 0.5$ V or 3.0 V (whichever is greater), I_{OUT} = 10 μA, C_{IN} = 1 μF, C_{OUT} = 1 μF (Note 5), ADJ pin connected to V_{OUT} pin, unless otherwise noted. Typical values are at T_A = +25°C. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PSRR AND NOISE						
Output Noise Voltage	V_{OUT} = 3.3 V (ADJ), C_{FF} = 10 nF, C_{OUT} = 2.2 μF, I_{OUT} = 100 mA	V_{NOISE}				μV_{rms}
	f = 10 Hz to 100 kHz		–	83	–	
	f = 10 Hz to 1 MHz		–	130	–	
POWER GOOD, DELAY						
Power Good Threshold	V_{OUT} rising	V_{PGUP}	85%	90%	95%	V_{OUTNOM}
	V_{OUT} falling	V_{PGDOWN}	83%	88%	93%	V_{OUTNOM}
Power Good Hysteresis		V_{PGDHYS}	–	2.3%	4%	V_{OUTNOM}
Power Good Voltage Low	$V_{ADJ-FORCED}$ = 80% V_{ADJ}, I_{PG} = 1 mA	V_{PGLO}	–	0.05	0.25	V
Power Good Leakage Current	$V_{PG} = V_{OUT-NOM}$	I_{PG}	–	0.02	1	μA
Delay pin Current	V_{DEL} = 0 V	I_{DEL}	0.3	0.9	2	μA
Delay pin Threshold Voltage	V_{DEL} rising	V_{DEL-TH}	1.1	1.2	1.3	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_{SD}	–	170	–	°C
Thermal Shutdown Hysteresis		T_{SH}	–	15	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Typical value of output voltage at 25°C is set during testing to value $V_{NOM25} = V_{NOM} * 1.003$ (what means +0.3% above V_{NOM}) to have symmetrical deviation of V_{OUT} to V_{NOM} over the whole temperature range. Note that V_{OUT} at 25°C is at it's maximum. See V_{OUT} vs. Temperature chart below for details.
8. Dropout voltage is measured when the output voltage falls 100 mV below the nominal output voltage. ADJ version is measured with ADJ pin connected to resistor divider which sets V_{OUT} to 3.3 V. Limits are valid for all voltage versions.

APPLICATIONS INFORMATION

The NCV8737 is high input voltage regulator with internal thermal shutdown and internal current limit. Typical application circuits are shown in Figures TBD to TBD.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected as close as possible to the input pin of NCV8737 regulator. Higher capacitance and lower ESR will improve the overall line and load transient response. Larger values help improve Line Transient response and minimize the impact of long input traces at the PCB path.

Output Decoupling (C_{out})

The NCV8737 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling effective value is 0.9 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors up to 100 μF. The larger values improve noise rejection and load regulation transient response.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. The turn−on/turn−off transient voltage being supplied to the enable pin should exceed a slew rate of TBD mV/μs to ensure correct operation. If the enable function is not to be used then the pin should be connected to VIN pin.

Output Voltage Adjust

The output voltage can be adjusted from 1.2 V to 20.0 V using resistors between the output and the ADJ input. The output voltage and resistors are chosen using Equation 1 and Equation 2.

$$V_{out} = TBD\left(1 + \frac{R_1}{R_2}\right) + \left(I_{ADJ} \times R_1\right) \quad \text{(eq. 1)}$$

$$R_2 \cong R_1 \frac{1}{\frac{V_{out}}{TBD} - 1} \quad \text{(eq. 2)}$$

Input bias current I_{ADJ} is typically less than TBD nA. Choose R_1 arbitrarily to minimize errors due to the bias current and to minimize noise contribution to the output voltage. Use Equation 2. in order to find the required value for R_2.

Thermal Considerations

As power in the NCV8737 regulator increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8737 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8737 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 3)}$$

See the chart in Typical Characteristic chapter for R_{thJA} versus PCB area relation. The power dissipated by the NCV8737 device can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_{GND}@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 4)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_{GND}} \quad \text{(eq. 5)}$$

Power Good

The power−good (PG) pin is an open−drain output and can be connected to any 5−V or lower rail through an external pull−up resistor. When C_{DELAY} is not used, the PG output is high−impedance when V_{OUT} is greater than the PG threshold. If V_{OUT} falls below PG threshold, the open−drain output turns on and pulls the PG pin to ground. The Current through PG pin is internally limited in order to avoid device damage by flowing a high current through this pin. If the output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

Power Good Delay

The power−good delay time (t_{DELAY}) is defined as the time period from when VOUT exceeds the PG trip threshold voltage to point when the PG output is high. This power−good delay time could be set by an external capacitor (C_{DEL}) connected from the DEL pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current (I_{DEL}) once VOUT exceeds the PG threshold .

When C_{DELAY} is used, the PG output is high−impedance when V_{OUT} exceeds PG threshold, and V_{DELAY} exceeds V_{REF}.

The Power Good Delay time can be calculated using: $t_{DELAY} = (C_{DEL} \text{ X } V_{REF}) / I_{DEL}$.

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8737, and make traces as short as possible.

ORDERING INFORMATION (Note 9)

Device pn.	Output Voltage	OUT Active Discharge	Marking	Package	Shipping†
NCV8737ADN330R2G	3.3 V	Yes	TBD	MSOP8 EP 3x3 Pb−free	3000 / Tape & Reel
NCV8737ADN500R2G	5 V	Yes	TBD		
NCV8737ADNADJR2G	Adj.	Yes	TBD		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. To order DFNW8 3x3 package, other FIX voltage version or non output active discharge version, please contact your **onsemi** sales representative.

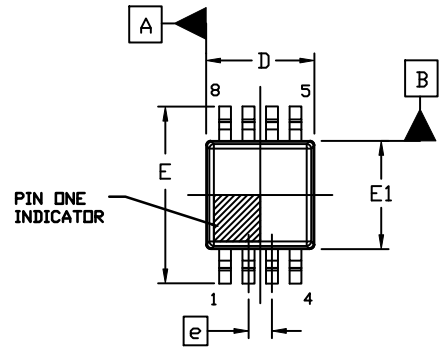
REVISION HISTORY

Revision	Description of Changes	Date
P5	Updated DFNW Thermal Characteristics values.	9/19/2025

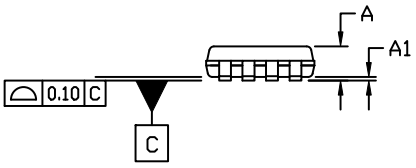
*Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

PACKAGE DIMENSIONS

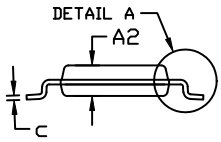
MSOP8 EP 3x3
CASE 846AT
ISSUE O



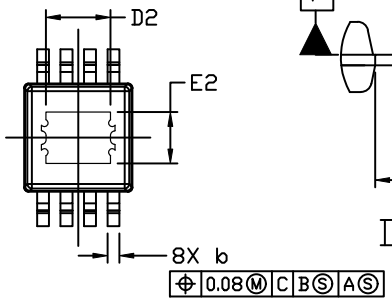
TOP VIEW



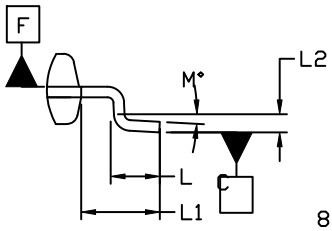
SIDE VIEW



END VIEW



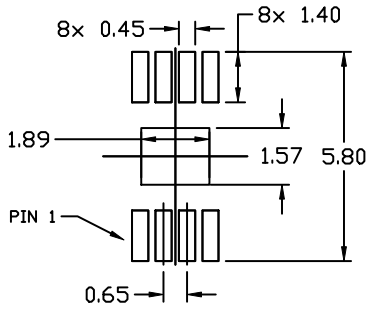
BOTTOM VIEW NOTE 3



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE PLATED LEADS.
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.813	0.863	0.914
b	0.28	---	0.38
c	0.139	---	0.23
D	2.90	3.00	3.10
D2	1.50	1.70	1.80
E	4.775	4.876	4.978
E1	2.90	3.00	3.10
E2	1.14	1.40	1.50
e	0.65 BSC		
L	0.40	---	---
L1	0.94 REF		
L2	0.25 REF		
M	0°	---	8°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales