

NDD01N60, NDT01N60

N-Channel Power MOSFET 600 V, 8.5 Ω

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	V_{DS}	600		V
Continuous Drain Current $R_{\theta JC}$ Steady State, $T_C = 25^\circ\text{C}$ (Note 1)	I_D	1.5	0.4	A
Continuous Drain Current $R_{\theta JC}$ Steady State, $T_C = 100^\circ\text{C}$ (Note 1)	I_D	1.0	0.25	A
Pulsed Drain Current, $t_p = 10 \mu\text{s}$	I_{DM}	6.0	1.5	A
Power Dissipation – $R_{\theta JC}$ Steady State, $T_C = 25^\circ\text{C}$	P_D	46	2.5	W
Gate-to-Source Voltage	V_{GS}	± 30		V
Single Pulse Drain-to-Source Avalanche Energy ($I_{PK} = 1.0 \text{ A}$)	EAS	13		mJ
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Source Current (Body Diode)	I_S	1.5	0.4	A
Lead Temperature for Soldering Leads	T_L	260		$^\circ\text{C}$
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to $+150$		$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Limited by maximum junction temperature
2. $I_S = 1.5 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDD01N60	$R_{\theta JC}$	2.7	$^\circ\text{C}/\text{W}$
Junction-to-Ambient (Note 4) NDD01N60	$R_{\theta JA}$	38	$^\circ\text{C}/\text{W}$
(Note 3) NDD01N60-1		96	
(Note 4) NDT01N60		58	
(Note 5) NDT01N60		141	

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

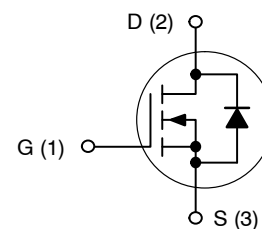


ON Semiconductor®

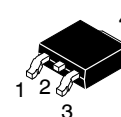
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$
600 V	8.5 Ω @ 10 V

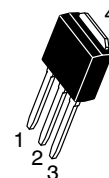
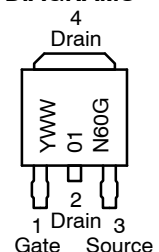
N-Channel MOSFET



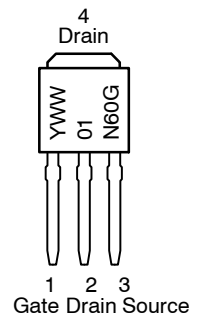
MARKING DIAGRAMS



**DPACK
CASE 369C
STYLE 2**



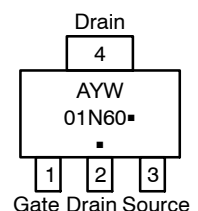
**IPACK
CASE 369D
STYLE 2**



Y = Year
WW = Work Week
G = Pb-Free Package



**SOT-223
CASE 318E
STYLE 3**



A = Assembly Location
Y = Year
W = Work Week
01N60 = Specific Device Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NDD01N60, NDT01N60

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
----------------	--------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	Reference to 25°C, I _D = 1 mA		660		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	T _J = 25°C		1	μA
			T _J = 125°C		50	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 50 μA	2.2	3.3	3.7	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			7.0		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 0.2 A		8.0	8.5	Ω
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 0.2 A		0.9		S

CHARGES, CAPACITANCES & GATE RESISTANCES

Input Capacitance (Note 7)	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		160		pF
Output Capacitance (Note 7)	C _{oss}			22		
Reverse Transfer Capacitance (Note 7)	C _{rss}			4.0		
Total Gate Charge (Note 7)	Q _g	V _{DS} = 300 V, I _D = 0.4 A, V _{GS} = 10 V		7.2		nC
Gate-to-Source Charge (Note 7)	Q _{gs}			1.2		
Gate-to-Drain Charge (Note 7)	Q _{gd}			3.1		
Plateau Voltage	V _{GP}			4.5		V
Gate Resistance	R _g			6.7		Ω

SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 0.4 A, V _{GS} = 10 V, R _G = 0 Ω		8.0		ns
Rise Time	t _r			5.1		
Turn-off Delay Time	t _{d(off)}			16.5		
Fall Time	t _f			21.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Diode Forward Voltage	V _{SD}	I _S = 0.4 A, V _{GS} = 0 V	T _J = 25°C		0.78	1.6	V
			T _J = 125°C		0.63		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, V _{DD} = 30 V I _S = 1.0 A, d _i /d _t = 100 A/μs		179			ns
Charge Time	t _a			37			
Discharge Time	t _b			141			
Reverse Recovery Charge	Q _{rr}			288			nC

6. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

7. Guaranteed by design.

8. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NDD01N60-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD01N60T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel
NDT01N60T1G	SOT-223 (Pb-Free, Halogen-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

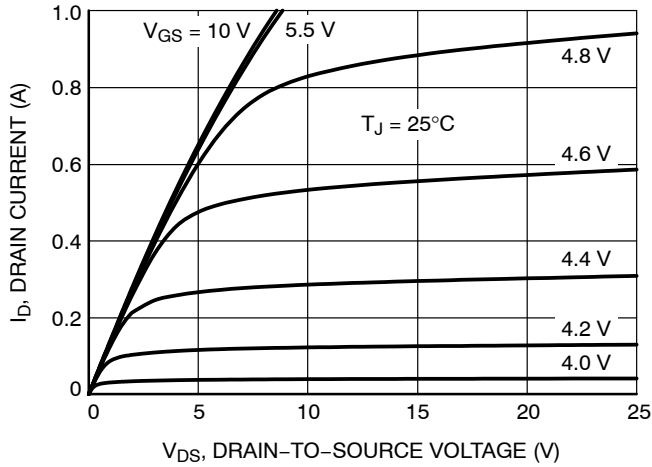


Figure 1. On-Region Characteristics

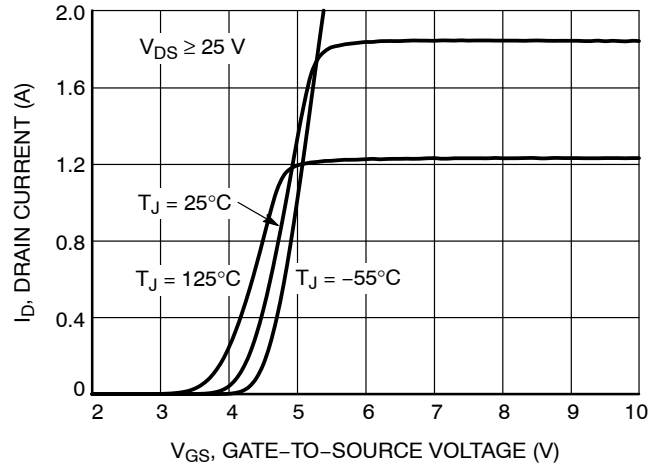


Figure 2. Transfer Characteristics

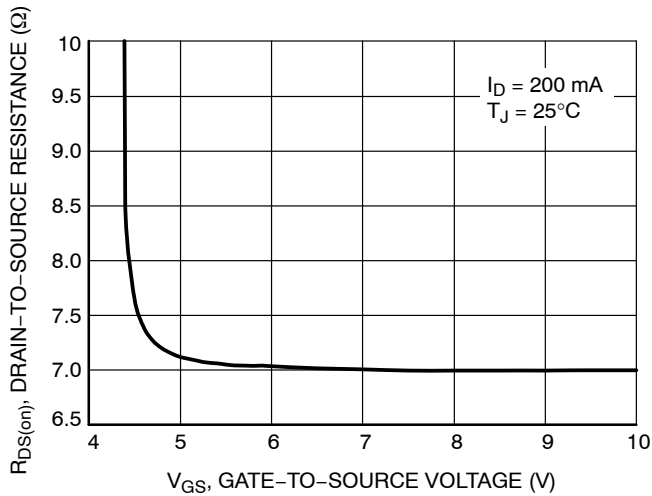


Figure 3. On-Resistance vs. Gate Voltage

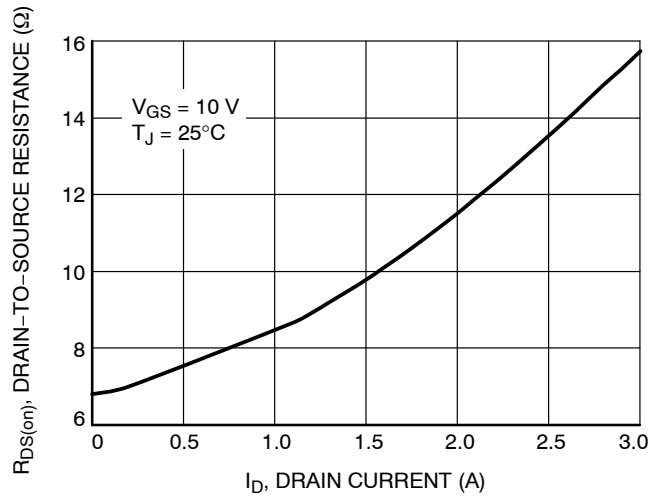


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

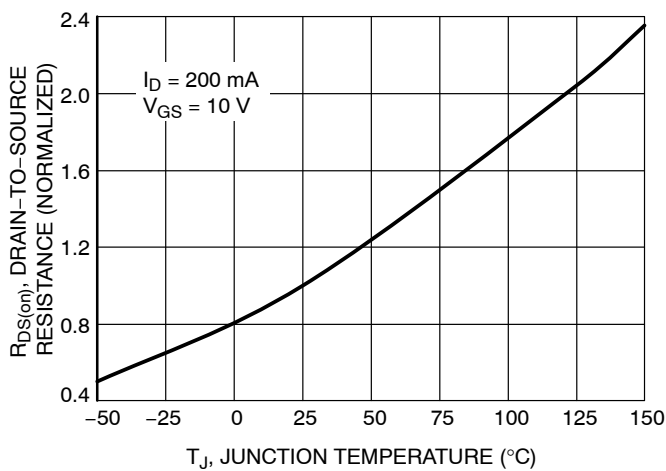


Figure 5. On-Resistance Variation with Temperature

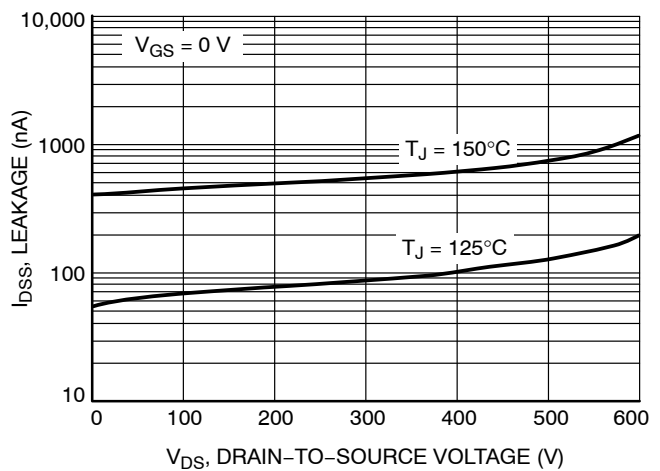


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NDD01N60, NDT01N60

TYPICAL CHARACTERISTICS

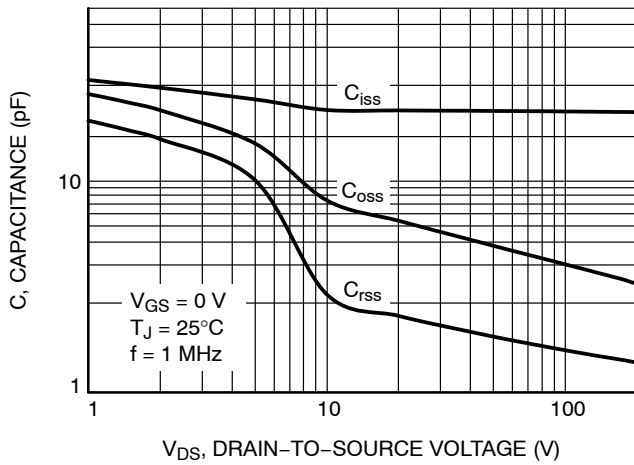


Figure 7. Capacitance Variation

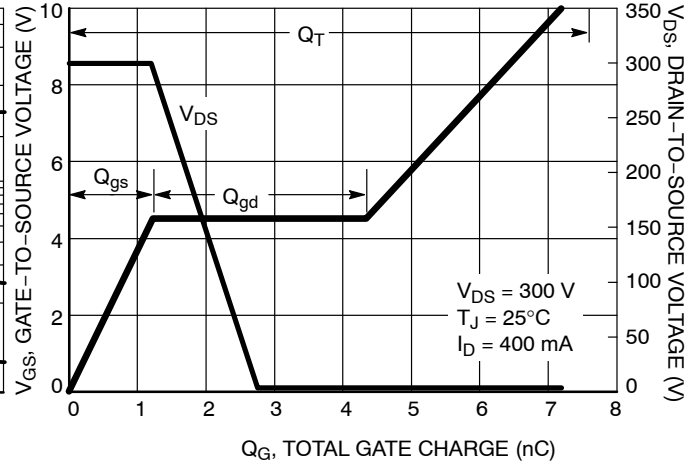


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

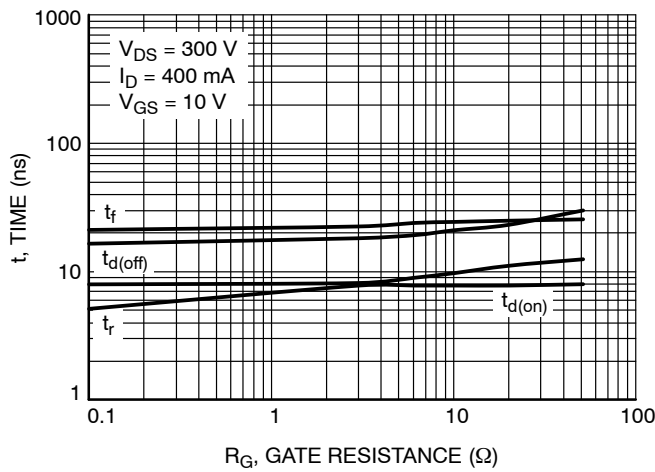


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

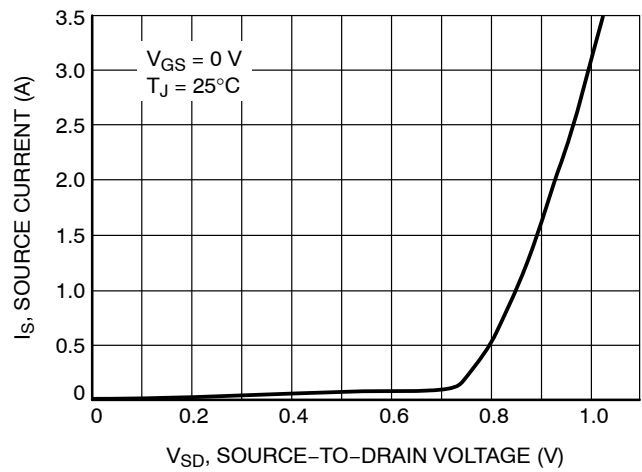


Figure 10. Diode Forward Voltage vs. Current

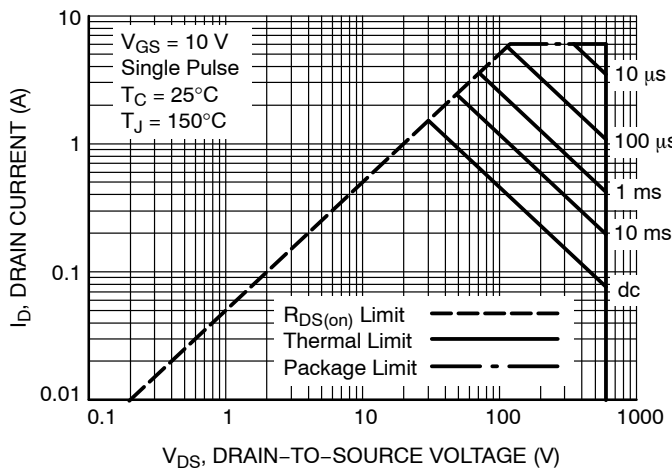


Figure 11. Maximum Rated Forward Biased Safe Operating Area NDD01N60

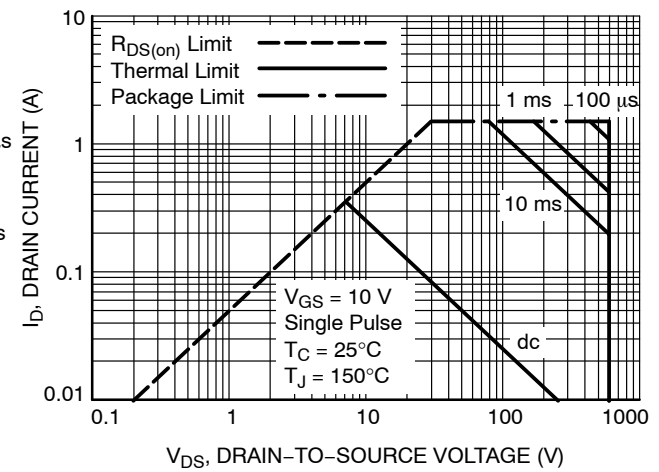


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDT01N60

NDD01N60, NDT01N60

TYPICAL CHARACTERISTICS

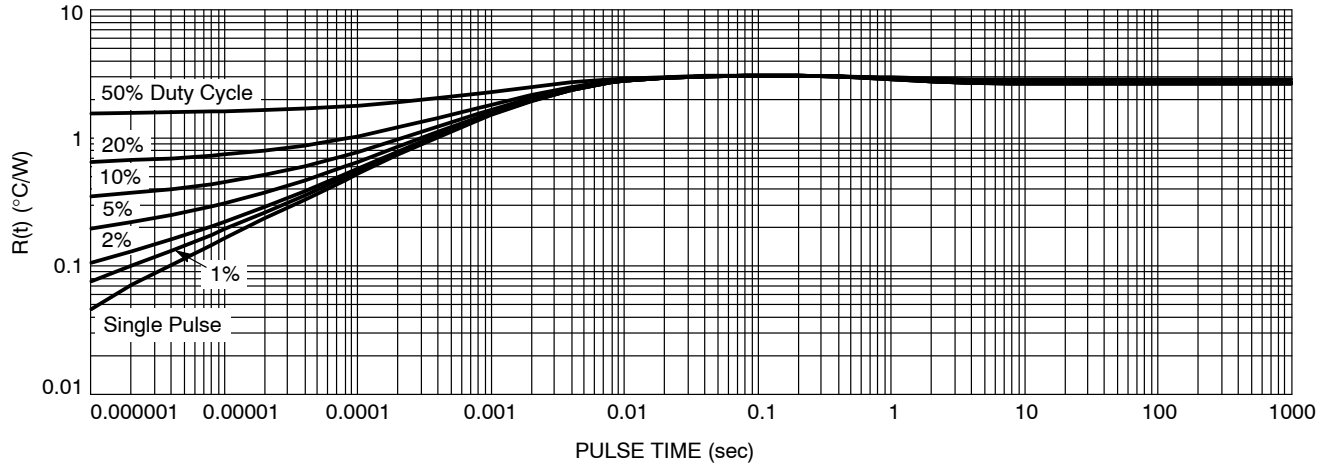


Figure 13. Thermal Impedance (Junction-to-Case) for NDD01N60

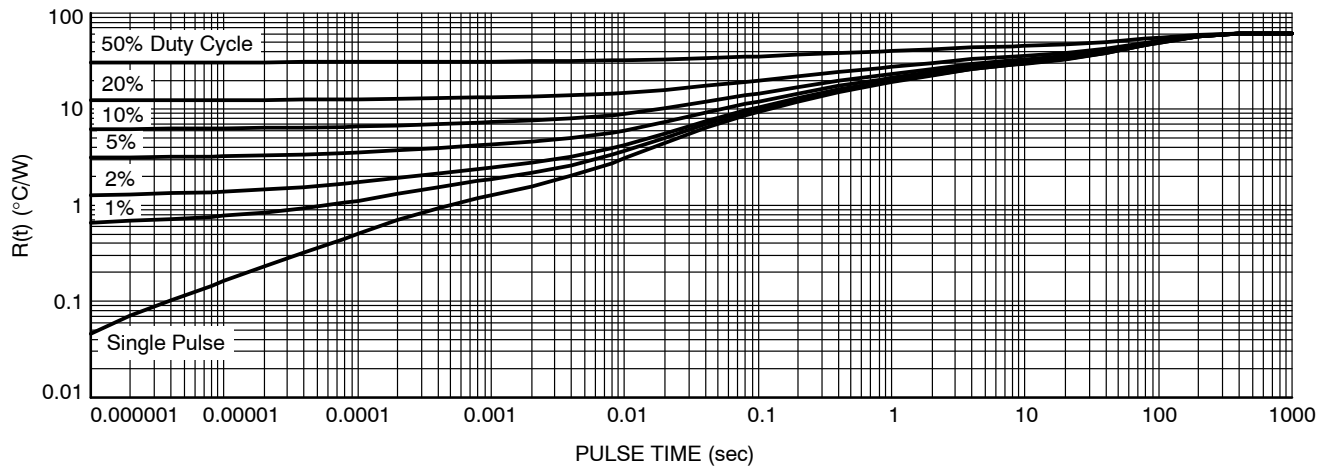
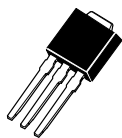


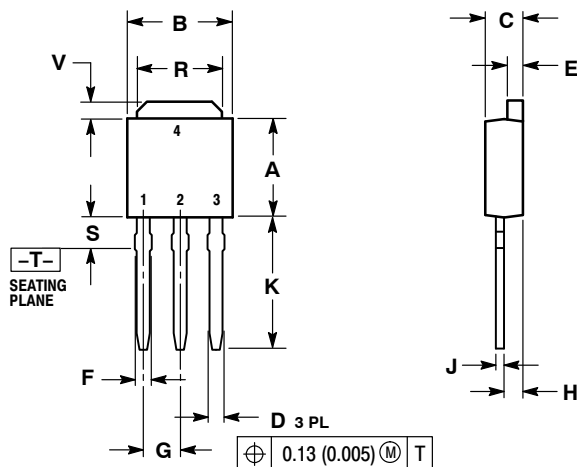
Figure 14. Thermal Impedance (Junction-to-Ambient) for NDT01N60



DPAK INSERTION MOUNT
CASE 369
ISSUE O

DATE 02 JAN 2000

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DOCUMENT NUMBER:	98ASB42319B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK INSERTION MOUNT	PAGE 1 OF 1

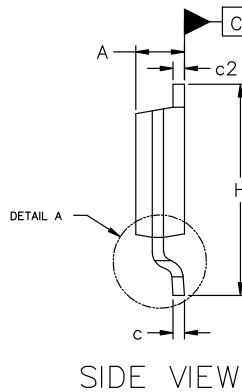
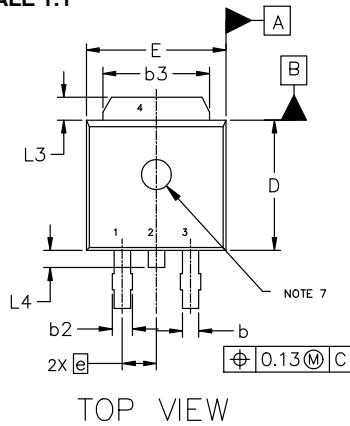
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



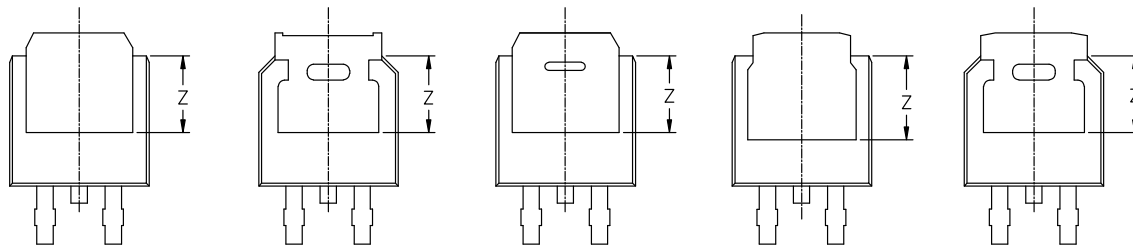
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1

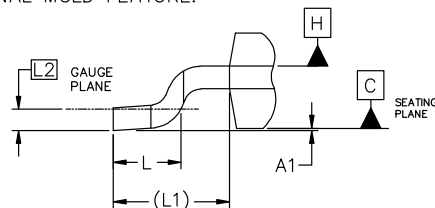


MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 2 OF 2

onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales