

1 Ω SPDT Switch

NL5S4157A

The NL5S4157A is a low R_{ON} SPDT analog switch. The device is designed for low operating voltage, high current switching of speaker output for mobile applications. It can switch a balanced stereo output. It can handle a balanced microphone/speaker/ringtone generator in monophone mode.

Features

- Wide V_{CC} Operating Range: 1.65 V to 5.5 V
- OVT up to +5.5 V for Control pin
- R_{ON} : Typically $< 1 \Omega$ at $V_{CC} = 4.5$ V
- Rail-to-Rail Input/Output
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

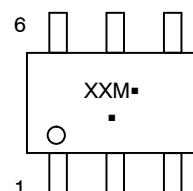
Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Stereo Balanced (Push-Pull) Switching
- RF PA Routing
- General Switching



SC-88/SC70-6/SOT-363
CASE 419B-02

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NL5S4157A

PIN ASSIGNMENTS

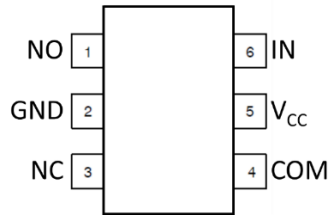


Figure 1. NL5S4157A (Top View)

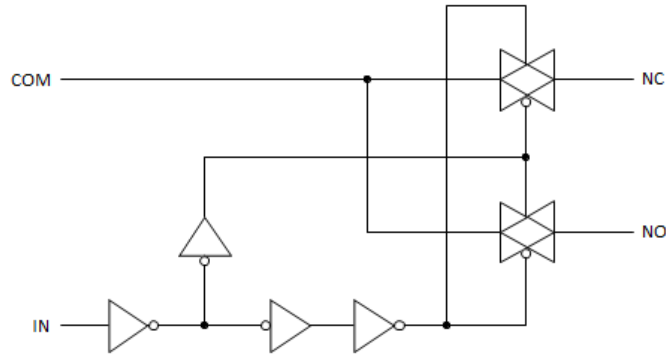


Figure 2. Analog Symbol

PIN DESCRIPTION

Pin	Name	Description
1	NO	Normally-Open Port
2	GND	Supply Ground
3	NC	Normally-Closed Port
4	COM	Common Port
5	V _{CC}	Supply
6	IN	Switch Select Input

FUNCTION TABLE

IN	Switch
L	NC to COM
H	NO to COM

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +6.0	V
V_{IS}	Switch Input / Output Voltage	-0.5 to $V_{CC}+0.5$	V
V_{IN}	Digital Select Input Voltage	-0.5 to +6.0	V
I_{OK}	I/O Port Diode Current	± 100	mA
I_{IK}	Select Input Diode Current	-100	mA
$I_{I/O}$	Continuous DC Current Through Analog Switch	± 100	mA
$I_{I/O-pk}$	Peak Current Through Analog Switch, 10% Duty Cycle	± 300	mA
T_s	Storage Temperature	-65 to +150	°C
ESD	Human Body Model (HBM)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IS}	Switch Input / Output Voltage	GND	V_{CC}	V
V_{IN}	Digital Select Input Voltage	GND	5.5	V
T_A	Operating Temperature Range	-40	+125	°C
t_r, t_f	Input Transition Rise or Fall Time (Select Input IN)	$V_{CC} \leq 3.0\text{ V}$	0	ns/V
		$V_{CC} > 3.0\text{ V}$	10	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	Guaranteed Limit							Unit
				25°C			–40°C to 85°C		–40°C to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Input High Voltage		2.7	1.1			1.1		1.1		V
			5.0	1.42			1.42		1.42		
V _{IL}	Input Low Voltage		2.7			0.4		0.4		0.4	V
			5.0			0.7		0.7		0.7	
I _{IN}	Input Leakage Current	V _{IN} = 0 V to 5.5 V	1.65 – 5.5			±0.1		±1		±1	µA
I _{OFF}	Input Leakage Current	V _{IN} = 0 to 5.5 V	0			0.05		1		1	µA
I _{S(ON)}	ON-State Switch Leakage Current	V _{IS} = GND to V _{CC} , V _{OS} = Open	5.5			±10		±200		±600	nA
I _{S(OFF)}	OFF-State Switch Leakage Current	V _{IS} = V _{CC} and V _{OS} = GND, or I _S = GND and V _{OS} = V _{CC}	5.5			±10		±200		±600	nA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OS} = 0 mA	5.5			0.5		5		5	µA

ANALOG SWITCH CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	Guaranteed Limit					Unit
				25°C			–40°C to 125°C		
				Min	Typ	Max	Min	Max	
R _{ON} (Note 1)	Switch ON Resistance	V _{IS} = 0 to V _{CC} , I _O = 100 mA	2.7		0.9	1.2		1.4	Ω
			4.5		0.6	0.8		1.0	
ΔR _{ON} (Notes 1, 2, 3)	ON Resistance Match	V _{IS} = 1.5 V, I _A = 100 mA	2.7		0.05	0.15		0.15	Ω
	Between Channels	V _{IS} = 2.5 V, I _A = 100 mA	4.5		0.04	0.12		0.15	
R _{FLAT} (Notes 1, 2, 4)	ON Resistance Flatness	V _{IS} = 0 to V _{CC} , I _O = 100 mA	2.7		0.3	0.4		0.4	Ω
			4.5		0.2	0.4		0.4	
Q (Note 5)	Charge Injection	C _L = 1 nF, V _{GEN} = 0 V,	2.7		38				pC
		R _{GEN} = 0 Ω	4.5		55				
V _{ISO} (Note 6)	Off–Isolation	R _L = 50 Ω, f = 1 MHz	2.7 – 5.5		–66				dB
V _{CT}	Crosstalk	R _L = 50 Ω, f = 1 MHz	2.7 – 5.5		–66				dB
BW	–3 dB Bandwidth	R _L = 50 Ω	2.7 – 5.5		57				MHz
THD (Note 5)	Total Harmonic Distortion	R _L = 600 Ω, V _{IS} = 0.5 V _{P–P} , f = 20 Hz to 20 kHz	2.7 – 5.5		0.004				%
C _I	Select Input Capacitance	f = 1 MHz	0		3.0				pF
C _{OFF}	NC/NO Port Off Capacitance	f = 1 MHz	4.5		23				pF
C _{ON}	COM Port ON Capacitance	f = 1 MHz	4.5		93				pF

1. Measured by the voltage drop between NC/NO and COM pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (NO, NC, COM).
2. Parameter is characterized but not tested in production.
3. ΔR_{ON} = R_{ON} max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
4. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
5. Guaranteed by Design.
6. V_{ISO} = 20 log₁₀ [V_{COM}/V_{NO,NC}].

SWITCHING CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	Guaranteed Limit					Unit
				25°C			−40°C to 125°C		
				Min	Typ	Max	Min	Max	
t _{PD} (Note 7)	Propagation Delay	V _{IN} = V _{IH} or V _{IL}	2.7			2.0		2.0	ns
			4.5			0.3		0.3	
t _{ON}	Turn-on Time, (COM to NO or NC)	R _L = 50 Ω, C _L = 35 pF,							ns
		V _{IS} = 1.5 V	2.7			30		35	
		V _{IS} = 3.0 V	4.5			20		25	
		R _L = 50 Ω, C _L = 100 pF,							
		V _{IS} = 1.5 V	3.3			100		100	
t _{OFF}	Turn-off Time, (COM to NO or NC)	R _L = 50 Ω, C _L = 35 pF,							ns
		V _{IS} = 1.5 V	2.7			20		25	
		V _{IS} = 3.0 V	4.5			15		20	
		R _L = 50 Ω, C _L = 100 pF,							
		V _{IS} = 1.5 V	3.3			100		100	
T _{BBM} (Note 5)	Break Before Make Time	R _L = 50 Ω, C _L = 35 pF	2.7	0.5			0.5		ns
			4.5	0.5			0.5		

7. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping [†]
NL5S4157ADFT2G	SC – 88/SC70 – 6/SOT – 363	AT	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

PIN 1 ORIENTATION IN TAPE AND REEL

Pin 1 Orientation in Tape and Reel
Direction of Feed

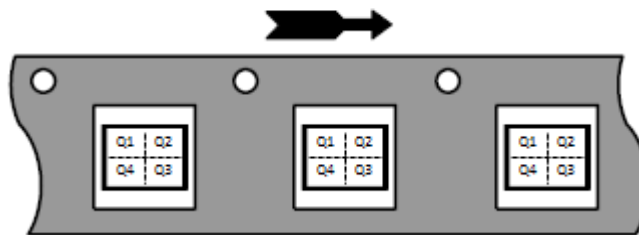


Figure 3.

Test Setups

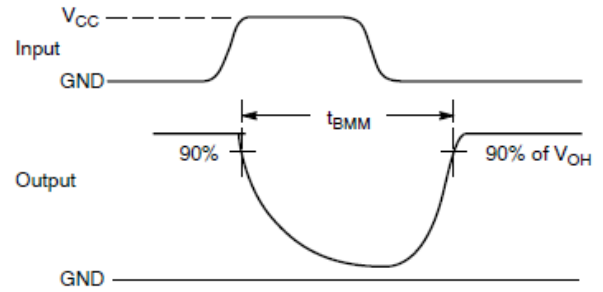
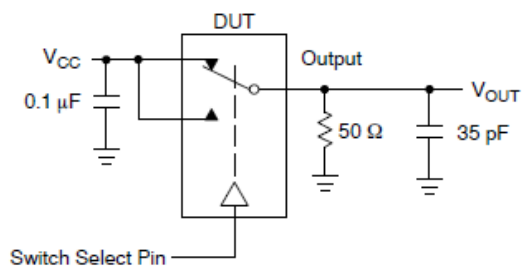


Figure 4. t_{BBM} (Time Break-Before-Make)

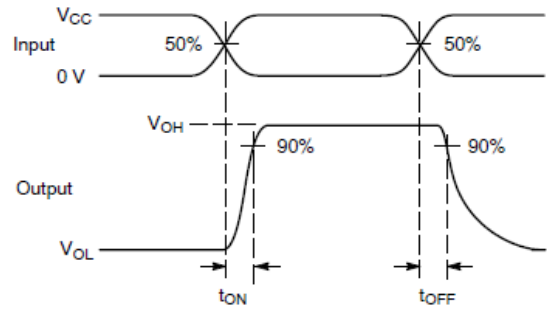
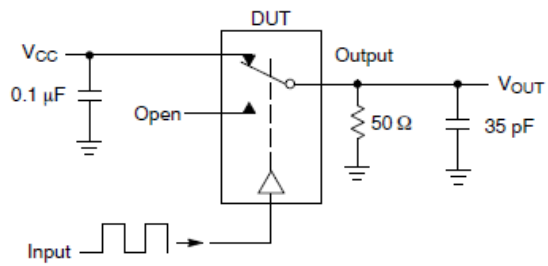
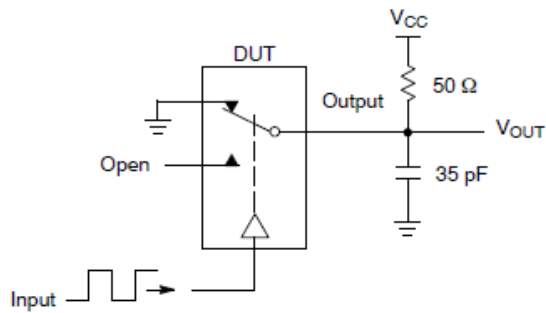


Figure 5. $t_{\text{ON}}/t_{\text{OFF}}$



Test Set-Up

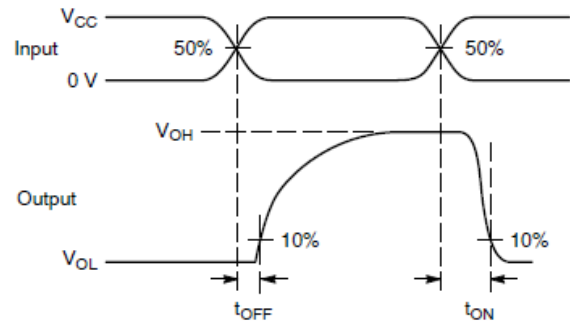
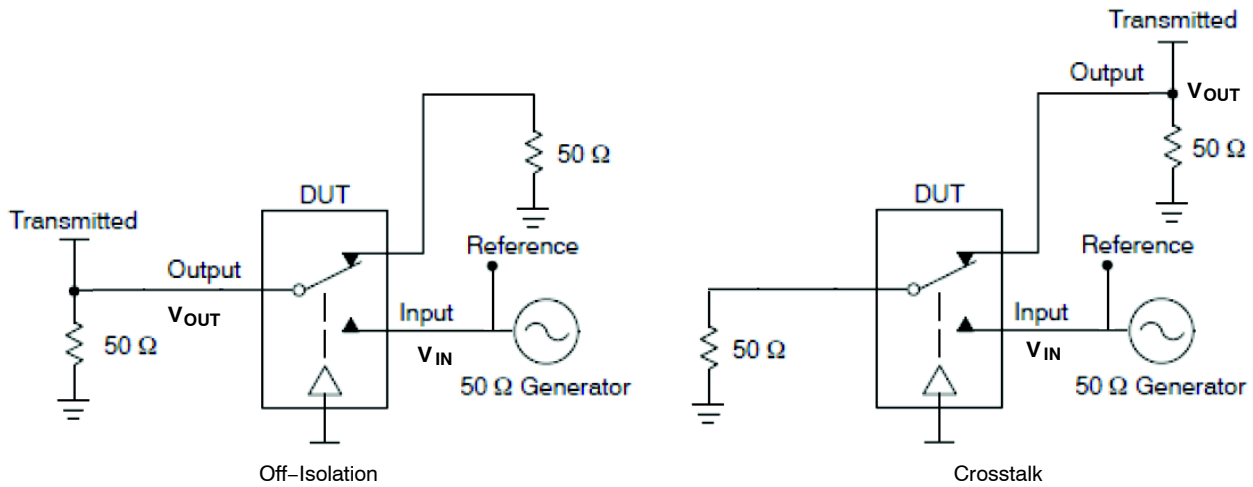


Figure 6. $t_{\text{ON}}/t_{\text{OFF}}$



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. Crosstalk is measured from an off channel to an on channel. On loss is the bandwidth of an On switch. V_{ISO} , V_{CT} , Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} or V_{CT} = Off Channel Isolation or crosstalk = $20 \text{ Log for } V_{OUT} / V_{IN}$

V_{ONL} = On Channel Loss = $20 \text{ Log for } V_{OUT} / V_{IN}$ at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

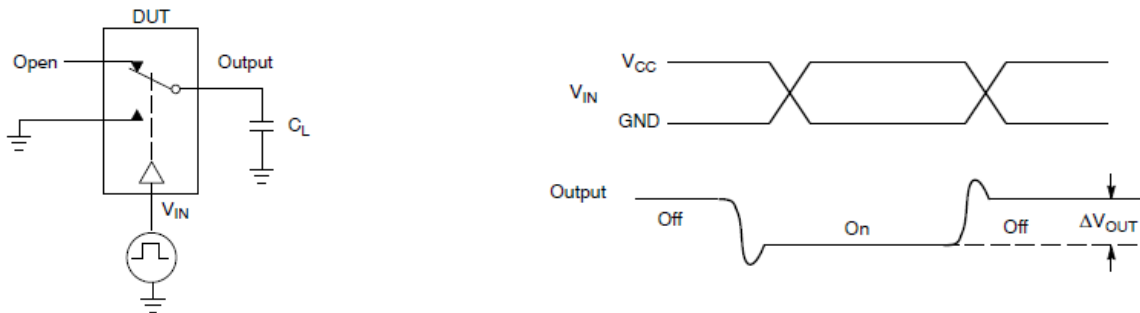


Figure 8. Charge Injection: (Q)

TYPICAL CHARACTERISTICS

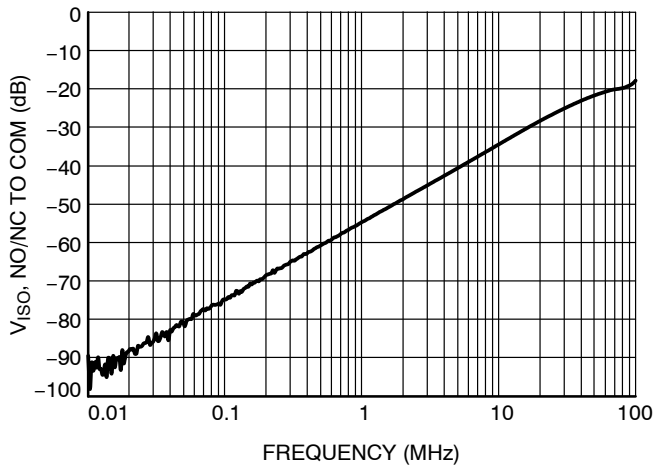


Figure 9. V_{ISO} vs. Frequency
@ $V_{CC} = 4.5$ V

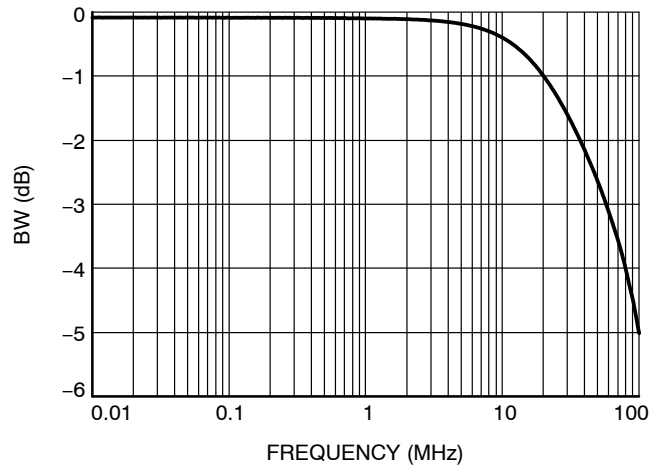


Figure 10. Bandwidth vs. Frequency

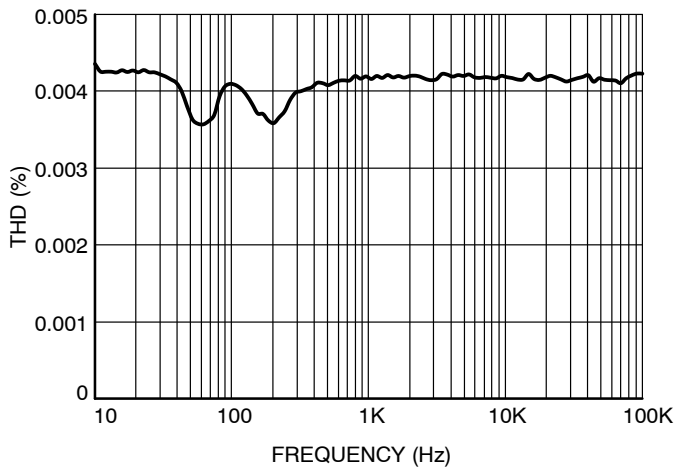


Figure 11. Total Harmonic Distortion

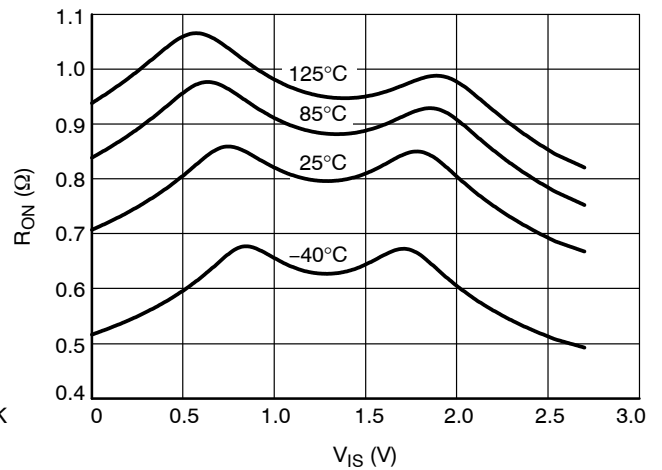


Figure 12. ON Resistance vs. Switch Voltage
@ $V_{CC} = 2.7$ V

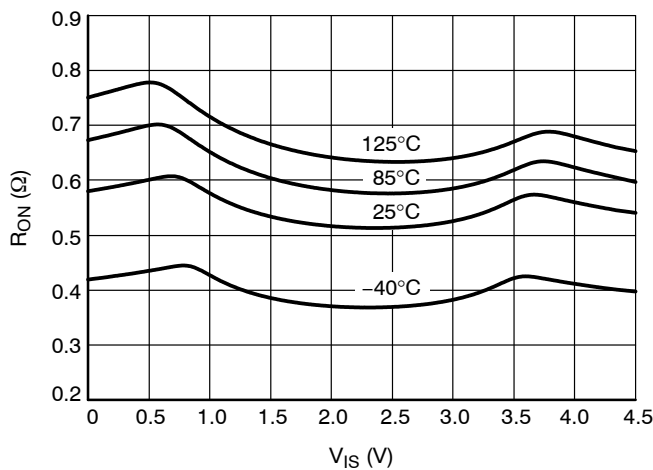


Figure 13. ON Resistance vs. Switch Voltage
@ $V_{CC} = 4.5$ V

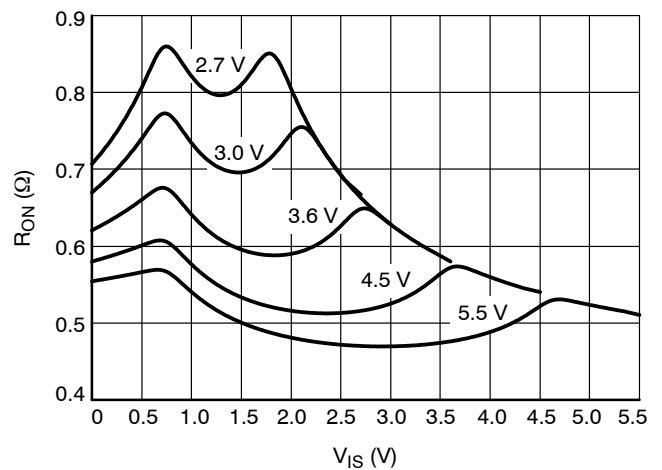


Figure 14. ON Resistance vs. Switch Voltage

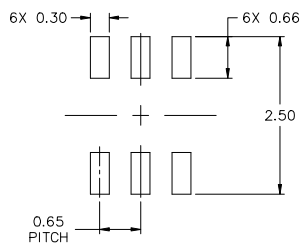
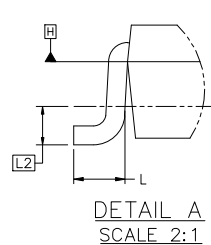
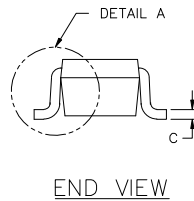
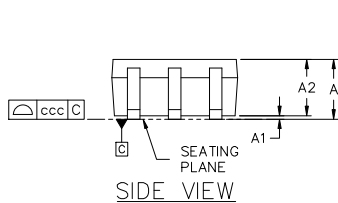
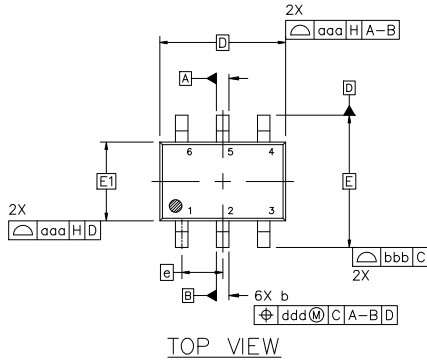


SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

NOTES:

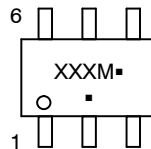
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		

STYLES ON PAGE 2

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SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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