

Low V_{CE(sat)} PNP Transistors 60 V, 2 A

NSS60200DMT

onsemi's e^2 PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage $(V_{CE(sat)})$ and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and LED lightning, power management...etc. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Package for optimal Automated Optical Inspection (AOI); NSV60200DMTWTBG – Wettable Flanks Device
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS $(T_A = 25^{\circ}C)$

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	6	Vdc
Collector Current – Continuous	I _C	2	Α
Collector Current - Peak	I _{CM}	3	Α

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient (Notes 1 and 2)	$R_{\theta JA}$	55	°C/W
Total Power Dissipation per Package @ $T_A = 25^{\circ}C$ (Note 2)	P _D	2.27	W
Thermal Resistance Junction-to-Ambient (Note 3)	$R_{\theta JA}$	69	°C/W
Power Dissipation per Transistor @ T _A = 25°C (Note 3)	P _D	1.8	W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

- 1. Per JESD51-7 with 100 mm² pad area and 2 oz. Cu (Dual Operation).
- 2. P_D per Transistor when both are turned on is one half of Total P_D or 1.13 Watts.

1

3. Per JESD51-7 with 100 mm² pad area and 2 oz. Cu (Single-Operation).

60 Volt, 2 Amp PNP Low $V_{CE(sat)}$ Transistors

MARKING DIAGRAM



WDFN6 CASE 506AN





WDFNW6 CASE 515AM



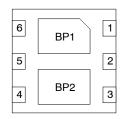
AD = Specific Device Code

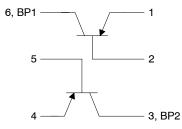
M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS





ORDERING INFORMATION

Device	Package	Shipping [†]
NSS60200DMTTBG	WDFN6 (Pb-Free)	3000/Tape & Reel
NSV60200DMTWTBG	WDFNW6 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. ELECTRICAL CHARACTERISTICS ($T_A = 25$ °C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•		<u> </u>		
Collector–Emitter Breakdown Voltage (I _C = -10 mA, I _B = 0)	V _{(BR)CEO}	-60			V
Collector-Base Breakdown Voltage (Ic = -0.1 mA, I _E = 0)	V _{(BR)CBO}	-80			V
Emitter-Base Breakdown Voltage (I _E = -0.1 mA, I _C = 0)	V _{(BR)EBO}	-6			V
Collector Cutoff Current (V _{CB} = -60 V, I _E = 0)	I _{CBO}			-100	nA
Emitter Cutoff Current (V _{BE} = -5.0 V)	I _{EBO}			-100	nA
ON CHARACTERISTICS				•	
DC Current Gain (Note 4) $ (I_C = -100 \text{ mA}, V_{CE} = -2.0 \text{ V}) $ $ (I_C = -500 \text{ mA}, V_{CE} = -2.0 \text{ V}) $ $ (I_C = -1 \text{ A}, V_{CE} = -2.0 \text{ V}) $ $ (I_C = -2 \text{ A}, V_{CE} = -2.0 \text{ V}) $	h _{FE}	150 120 90 40	230 180 140 80		
Collector–Emitter Saturation Voltage (Note 4) $ \begin{aligned} &(I_C = -500 \text{ mA}, \ I_B = -50 \text{ mA}) \\ &(I_C = -700 \text{ mA}, \ I_B = -7.0 \text{ mA}) \\ &(I_C = -1 \text{ A}, \ I_B = -50 \text{ mA}) \\ &(I_C = -1 \text{ A}, \ I_B = -100 \text{ mA}) \\ &(I_C = -2 \text{ A}, \ I_B = -200 \text{ mA}) \end{aligned} $	V _{CE(sat)}		-0.115 -0.295 -0.250 -0.200 -0.365	-0.160 -0.420 -0.350 -0.300 -0.450	V
Base – Emitter Saturation Voltage (Note 4) $ (I_C = -500 \text{ mA}, I_B = -50 \text{ mA}) $ $ (I_C = -1 \text{ A}, I_B = -50 \text{ mA}) $ $ (I_C = -1 \text{ A}, I_B = -100 \text{ mA}) $	V _{BE} (sat)			-1.0 -1.0 -1.1	V
Base-Emitter Turn-on Voltage (Note 4) (I _C = -500 mA, V _{CE} = -2.0 V)	V _{BE(on)}			-0.9	V
DYNAMIC CHARACTERISTICS				•	
Output Capacitance (V _{CB} = 10 V, f = 1.0 MHz)	C _{obo}		18		pF
Cutoff Frequency ($I_C = 50 \text{ mA}, V_{CE} = 2.0 \text{ V}, f = 100 \text{ MHz}$)	f _T		155		MHz
SWITCHING TIMES	•		•	•	•
Delay Time ($V_{CC} = -10 \text{ V}, I_{C} = -0.5 \text{ A}, I_{B1} = -25 \text{ mA}, I_{B2} = 25 \text{ mA}$)	t _d		15		ns
Rise Time ($V_{CC} = -10 \text{ V}, I_C = -0.5 \text{ A}, I_{B1} = -25 \text{ mA}, I_{B2} = 25 \text{ mA}$)	t _r		13		ns
Storage Time (V_{CC} = -10 V, I_{C} = -0.5 A, I_{B1} = -25 mA, I_{B2} = 25 mA)	t _s		360		ns
Fall Time ($V_{CC} = -10 \text{ V}, I_{C} = -0.5 \text{ A}, I_{B1} = -25 \text{ mA}, I_{B2} = 25 \text{ mA}$)	t _f		22		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Condition: Pulse Width = $300 \mu sec$, Duty Cycle $\leq 2\%$

TYPICAL CHARACTERISTICS

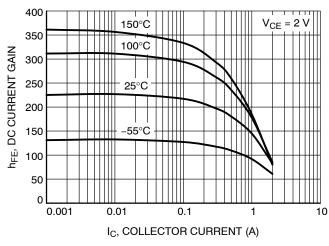


Figure 1. DC Current Gain

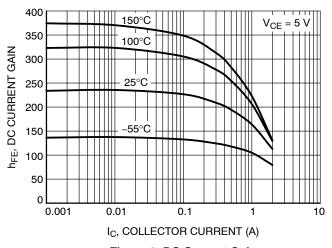


Figure 2. DC Current Gain

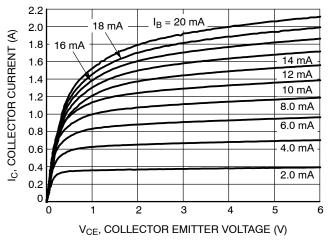


Figure 3. Collector Current as a Function of Collector Emitter Voltage

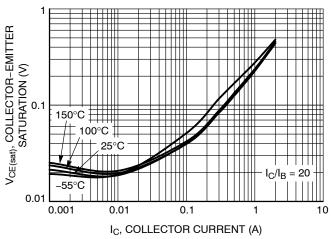


Figure 4. Collector-Emitter Saturation Voltage

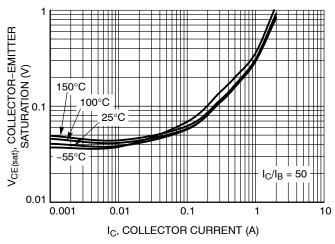


Figure 5. Collector-Emitter Saturation Voltage

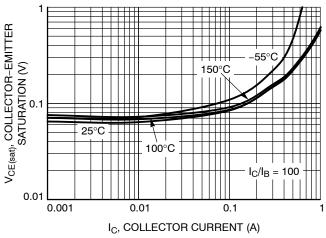


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL CHARACTERISTICS

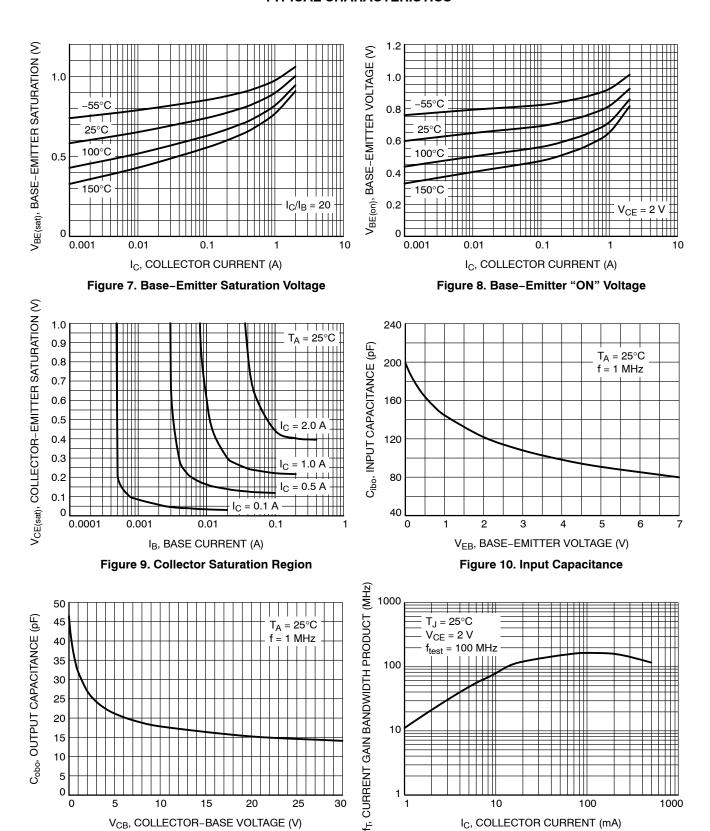


Figure 12. f_T, Current Gain Bandwidth Product

Figure 11. Output Capacitance

TYPICAL CHARACTERISTICS

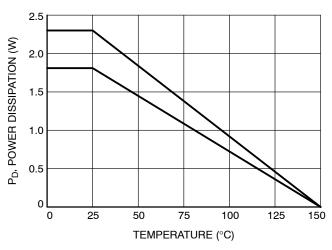


Figure 13. Power Derating

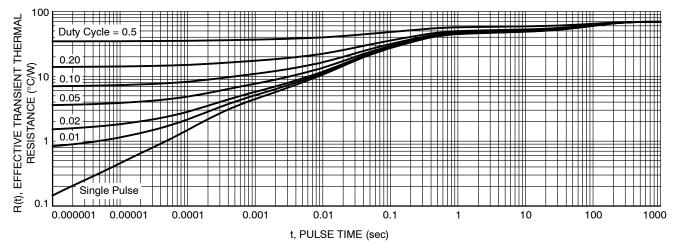


Figure 14. Thermal Resistance by Transistor

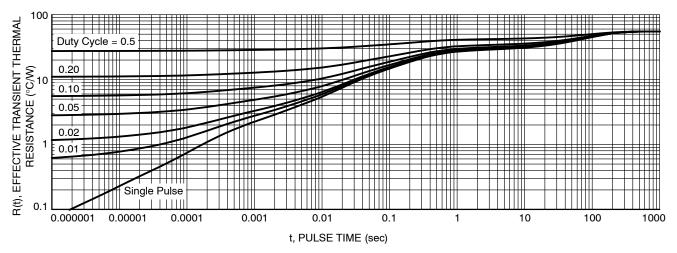
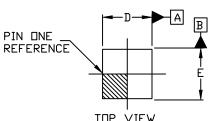


Figure 15. Thermal Resistance for Both Transistors

PACKAGE DIMENSIONS

WDFNW6 2x2, 0.65P

CASE 515AM **ISSUE O**

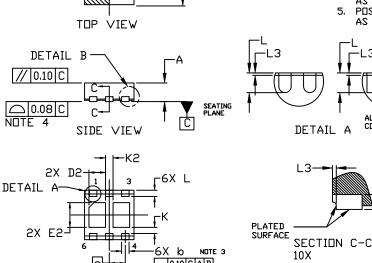


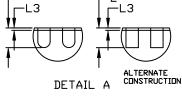
BOTTOM VIEW



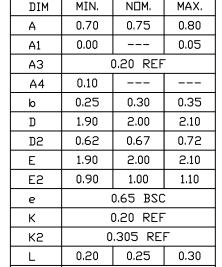
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
 DIMENSION 6 APPLIES TO PLATED TERMINALS AND IS
 MEASURED BETWEEN 0.15 AND 0.30MM FROM THE
- TERMINAL TIP.
 COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL
- AS THE TERMINALS.

 POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



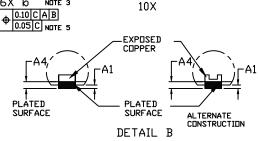


-A3



0.05 REF

MILLIMETERS



2X 0.83+	 0.15
PACKAGE —	F6X 0.70
1	₽₩₽₽₽
2X 1.10 1 0.65	2.80 2.80
	COMMENDED ING FOOTPRINT

L3

For additional information on our Pb-Free strategy and soldering details, please download the IIN Seniconductor Soldering and Mounting Techniques Reference Manual, SIDLERRWIN.



PIN ONE REFERENCE

□ 0.10 C

0.10 C

// 0.10 C



TOP VIEW

- DETAIL B

WDFN6 2x2, 0.65P CASE 506AN **ISSUE H**

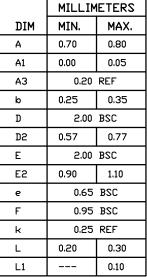
DETAIL A

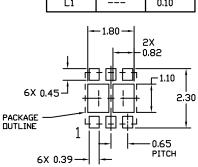
OPTIONAL CONSTRUCTIONS

DATE 25 JAN 2022

NOTES:

- DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- 4. COPLANARITY APPLIES TO THE EXPOSED





RECOMMENDED MOUNTING FOOTPRINT SOLDERMASK DEFINED

- 2.
- DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
- PADS AS WELL AS THE TERMINALS.

0.08 C NOTE 4 A1	(A3)	SEATING PLANE		EXPOSED COPPER
	SIDE VIEW	PLATIN		MOLD COMPOUND
DETAIL A	6 4 6X k	0.10 (M C A B	DETA OPTIONAL COM	

В

XX	= Specific Device Code
M	= Date Code

GENERIC

MARKING DIAGRAM*

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN6 2x2, 0.65P		PAGE 1 OF 1	

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