DATA SHEET
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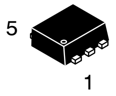
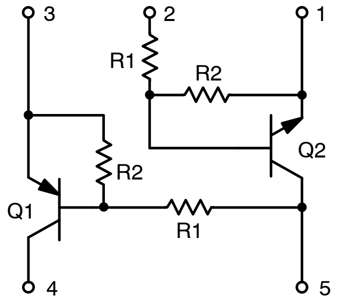
Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

NSTB1005DXV5T1G



SOT−553
CASE 463B

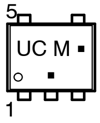


The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. The NSTB1005DXV5T1 contains two complementary BRT devices are housed in the SOT−553 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- This is a Pb−Free Device

MARKING DIAGRAM



UC = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Symbol	Rating	Value	Unit
V_{CBO}	Collector-Base Voltage	50	Vdc
V_{CEO}	Collector-Emitter Voltage	50	Vdc
I_C	Collector Current	100	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
NSTB1005DXV5T1G	SOT−553 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Characteristic (One Junction Heated)	Max	Unit
P_D	Total Device Dissipation T_A = 25°C (Note 1) Derate above 25°C (Note 1)	357 2.9	mW mW/°C
$R_{\theta JA}$	Thermal Resistance − Junction-to-Ambient (Note 1)	350	°C/W
Symbol	**Characteristic (Both Junctions Heated)**	**Max**	**Unit**
P_D	Total Device Dissipation T_A = 25°C (Note 1) Derate above 25°C (Note 1)	500 4.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance − Junction-to-Ambient (Note 1)	250	°C/W
T_J, T_{stg}	Junction and Storage Temperature	−55 to +150	°C

1. FR−4 @ Minimum Pad

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
Q1 TRANSISTOR: PNP − OFF CHARACTERISTICS					
I_{CBO}	Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	−	−	100	nAdc
I_{CEO}	Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	−	−	500	nAdc
I_{EBO}	Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	−	−	0.1	mAdc
$V_{(BR)CBO}$	Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	50	−	−	Vdc
$V_{(BR)CEO}$	Collector−Emitter Breakdown Voltage (I_C = 2.0 mA, I_B = 0)	50	−	−	Vdc
ON CHARACTERISTICS					
h_{FE}	DC Current Gain	80	140	−	
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 10 mA, I_E = 0.3 mA)	−	−	0.25	Vdc
V_{OL}	Output Voltage (on) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	−	−	0.2	Vdc
V_{OH}	Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	4.9	−	−	Vdc
R1	Input Resistor	32.9	47	61.1	kΩ
R_1/R_2	Resistor Ratio	0.8	1.0	1.2	
Q2 TRANSISTOR: NPN − OFF CHARACTERISTICS					
I_{CBO}	Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	−	−	100	nAdc
I_{CEO}	Collector-Emitter Cutoff Current (V_{CB} = 50 V, I_B = 0)	−	−	500	nAdc
I_{EBO}	Emitter-Base Cutoff Current (V_{EB} = 6.0, I_C = 0)	−	−	0.1	mAdc
ON CHARACTERISTICS					
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	50	−	−	Vdc
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (I_C = 2.0 mA, I_B = 0)	50	−	−	Vdc
h_{FE}	DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	80	140	−	
$V_{CE(SAT)}$	Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)	−	−	0.25	Vdc
V_{OL}	Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	−	−	0.2	Vdc
V_{OH}	Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	4.9	−	−	Vdc
R1	Input Resistor	33	47	61	kΩ
R1/R2	Resistor Ratio	0.8	1.0	1.2	

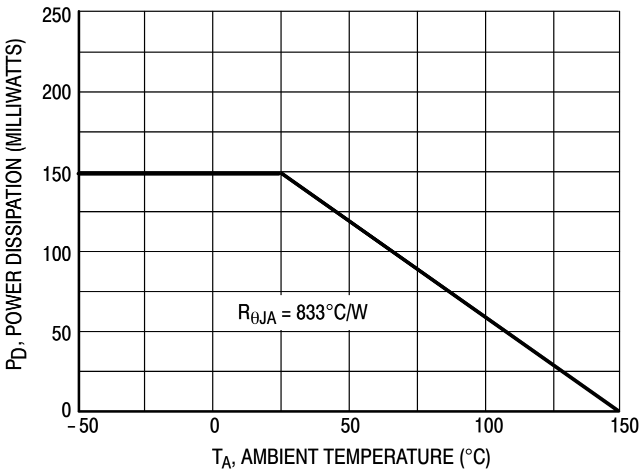


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS – PNP TRANSISTOR

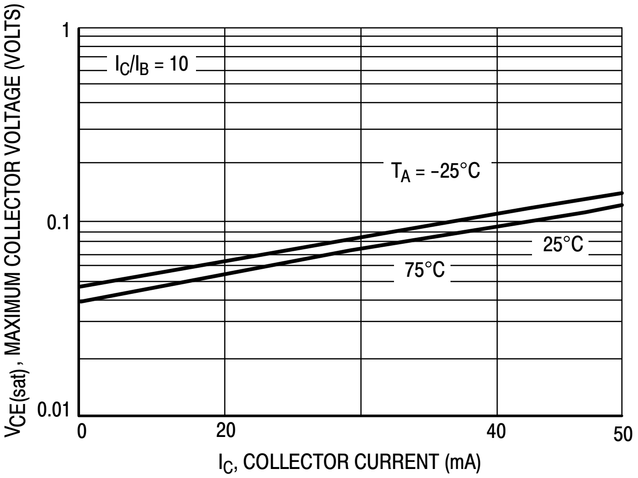


Figure 2. $V_{CE(sat)}$ versus I_C

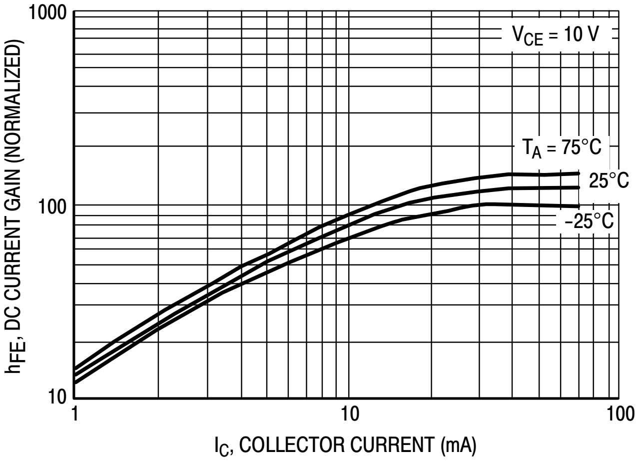


Figure 3. DC Current Gain

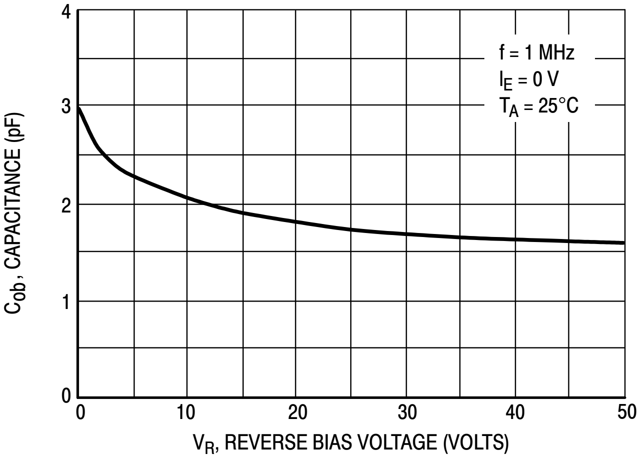


Figure 4. Output Capacitance

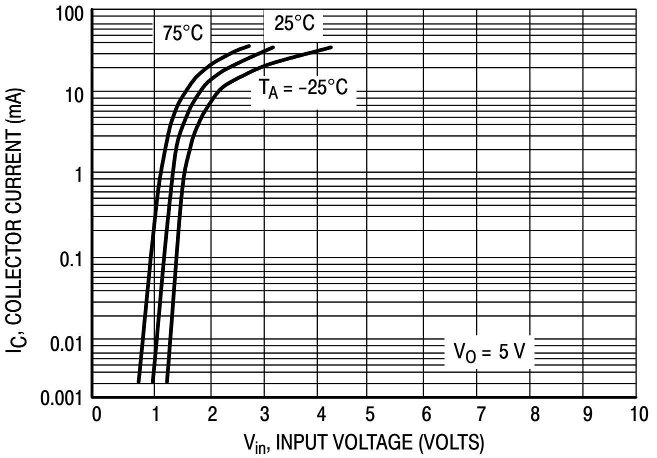


Figure 5. Output Current versus Input Voltage

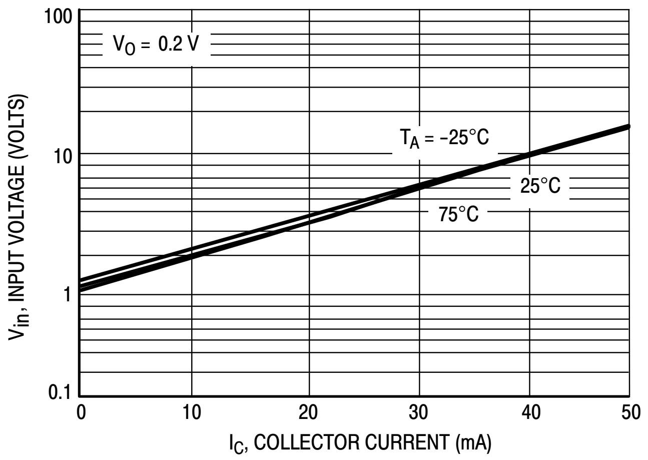


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

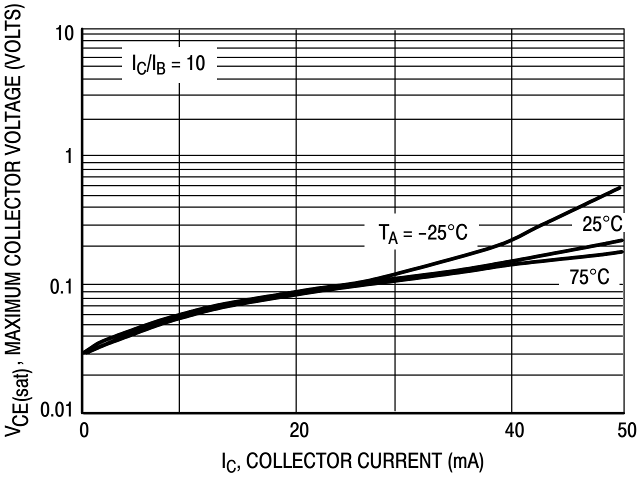


Figure 7. $V_{CE(sat)}$ versus I_C

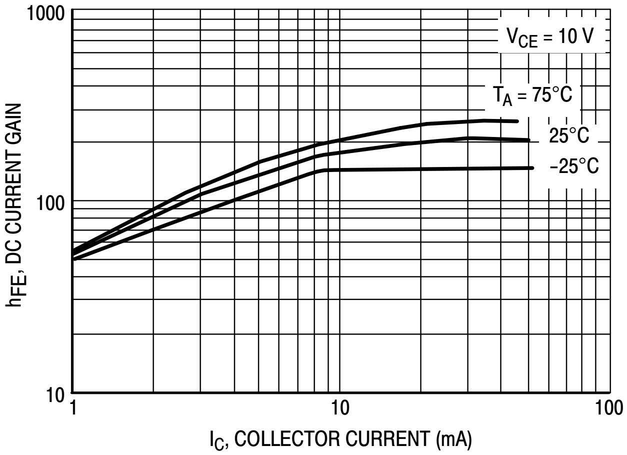


Figure 8. DC Current Gain

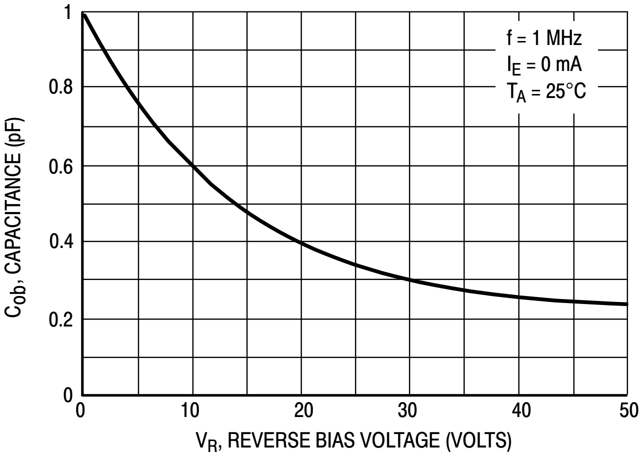


Figure 9. Output Capacitance

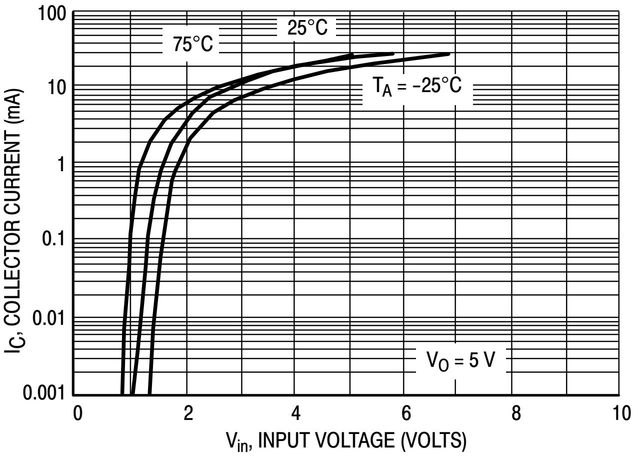


Figure 10. Output Current versus Input Voltage

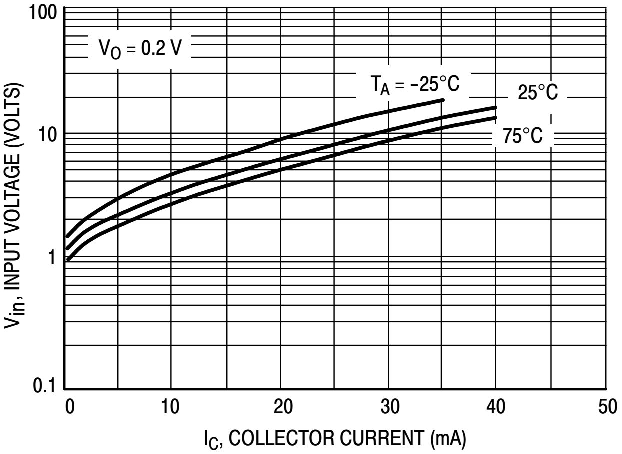
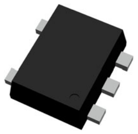


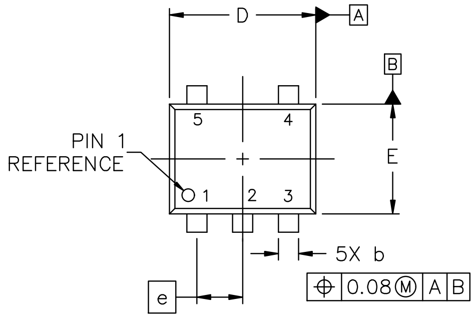
Figure 11. Input Voltage versus Output Current

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

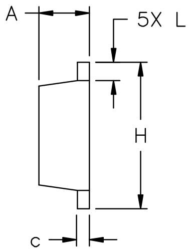


SOT-553-5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

DATE 21 FEB 2024



TOP VIEW

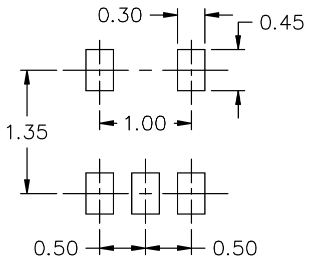


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

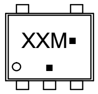
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.55	1.60	1.65
E	1.15	1.20	1.25
e	0.50 BSC		
H	1.55	1.60	1.65
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

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