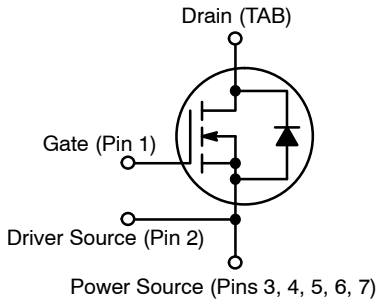
Silicon Carbide (SiC) MOSFET – EliteSiC, 160 mohm, 1200 V, M1, D2PAK-7L

NTBG160N120SC1

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
1200 V	224 mΩ @ 20 V	19.5 A



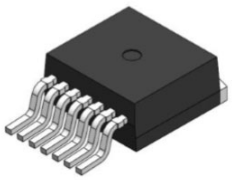
N−CHANNEL MOSFET

Features

- Typ. $R_{DS(on)}$ = 160 mΩ
- Ultra Low Gate Charge (typ. $Q_{G(tot)}$ = 33.8 nC)
- Low Effective Output Capacitance (typ. C_{oss} = 50.7 pF)
- 100% Avalanche Tested
- T_J = 175°C
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

- UPS
- DC-DC Converter
- Boost Inverter



D2PAK−7L
CASE 418BJ

MARKING DIAGRAM

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability
NTBG160120SC1 = Specific Device Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	1200	V
Gate−to−Source Voltage			V_{GS}	−15/+25	V
Recommended Operation Values of Gate−Source Voltage		T_C < 175°C	V_{GSop}	−5/+20	V
Continuous Drain Current (Note 1)	Steady State	T_C = 25°C	I_D	19.5	A
Power Dissipation (Note 1)			P_D	136	W
Continuous Drain Current (Note 1)	Steady State	T_C = 100°C	I_D	13.7	A
Power Dissipation (Note 1)			P_D	68	W
Pulsed Drain Current (Note 2)		T_A = 25°C	I_{DM}	78	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	13.6	A
Single Pulse Drain−to−Source Avalanche Energy (I_L = 15.5 A_{pk}, L = 1 mH) (Note 3)			E_{AS}	120	mJ
Maximum Lead Temperature for Soldering, 1/8″ from Case for 10 Seconds			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Repetitive rating, limited by max junction temperature.
3. E_{AS} of 120 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 15.5 A, V_{DD} = 120 V, V_{GS} = 18 V.

ORDERING INFORMATION

Device	Package	Shipping†
NTBG160N120SC1	D2PAK−7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2019

Table 1. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance Junction−to−Case (Note 1)	$R_{\theta JC}$	1.1	°C/W
Thermal Resistance Junction−to−Ambient (Note 1)	$R_{\theta JA}$	40	°C/W

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		1200			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$/ T_J	I_D = 1 mA, refer to 25°C			0.7		V/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	T_J = 25°C			100	μA
			T_J = 175°C			1	mA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = +25/−15 V, V_{DS} = 0 V				±1	μA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 2.5 mA		1.8	3	4.3	V
Recommended Gate Voltage	V_{GOP}			−5		+20	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 12 A, T_J = 25°C			160	224	mΩ
		V_{GS} = 20 V, I_D = 12 A, T_J = 175°C			239	365	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 12 A			5.5		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V			678		pF
Output Capacitance	C_{OSS}				50.7		
Reverse Transfer Capacitance	C_{RSS}				5.87		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −5/20 V, V_{DS} = 600 V, I_D = 16 A			33.8		nC
Threshold Gate Charge	$Q_{G(TH)}$				6.1		
Gate−to−Source Charge	Q_{GS}				11.6		
Gate−to−Drain Charge	Q_{GD}				9.6		
Gate−Resistance	R_G	f = 1 MHz			1.39		Ω
SWITCHING CHARACTERISTICS							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −5/20 V, V_{DS} = 800 V, I_D = 16 A, R_G = 6 Ω, Inductive Load			11	20	ns
Rise Time	t_r				11	20	
Turn−Off Delay Time	$t_{d(OFF)}$				15	27	
Fall Time	t_f				7.4	15	
Turn−On Switching Loss	E_{ON}				120		μJ
Turn−Off Switching Loss	E_{OFF}				28		
Total Switching Loss	E_{TOT}				148		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Continuous Drain−Source Diode Forward Current	I_{SD}	V_{GS} = −5 V, T_J = 25°C				13.6	A
Pulsed Drain−Source Diode Forward Current (Note 2)	I_{SDM}	V_{GS} = −5 V, T_J = 25°C				78	A
Forward Diode Voltage	V_{SD}	V_{GS} = −5 V, I_{SD} = 6 A, T_J = 25°C			3.9		V

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = −5/20 V, I_{SD} = 16 A, dI_S/dt = 1000 A/μs		15		ns
Reverse Recovery Charge	Q_{RR}			47		nC
Reverse Recovery Energy	E_{REC}			3.9		μJ
Peak Reverse Recovery Current	I_{RRM}			6.6		A
Charge Time	Ta			7.0		ns
Discharge Time	Tb			7.4		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

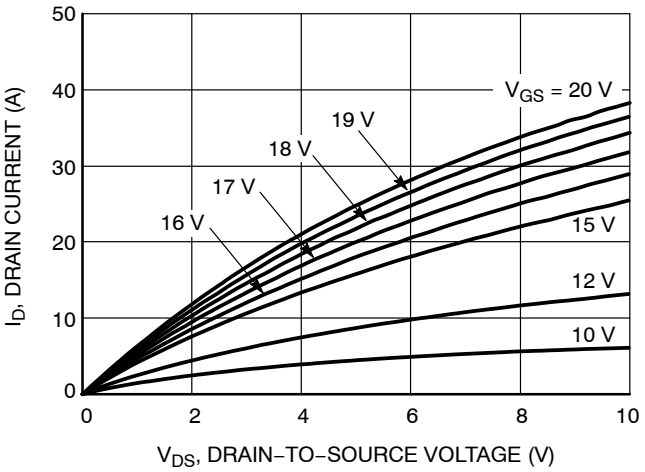


Figure 1. On−Region Characteristics

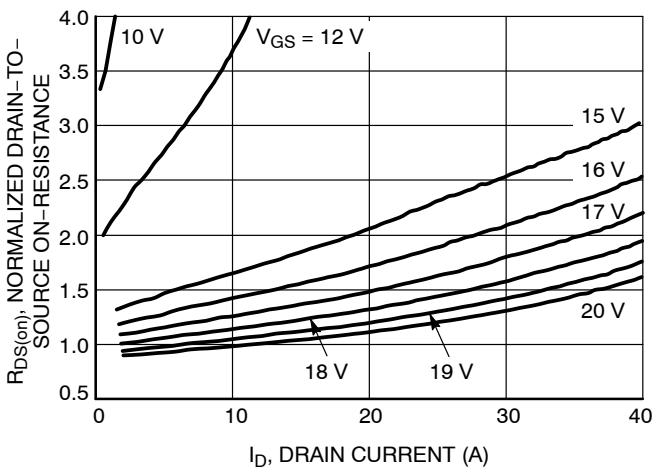


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

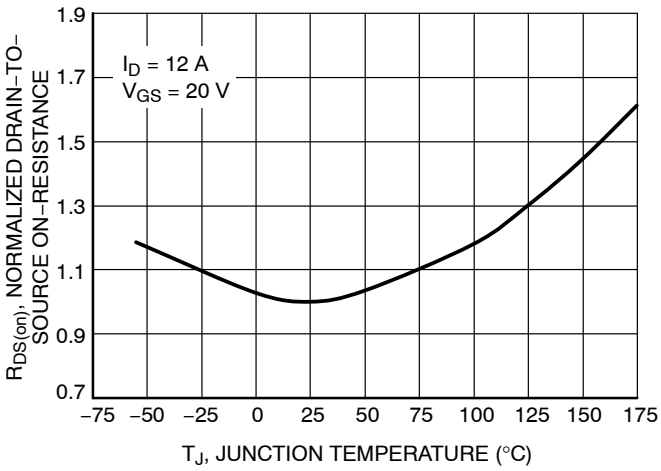


Figure 3. On−Resistance Variation with Temperature

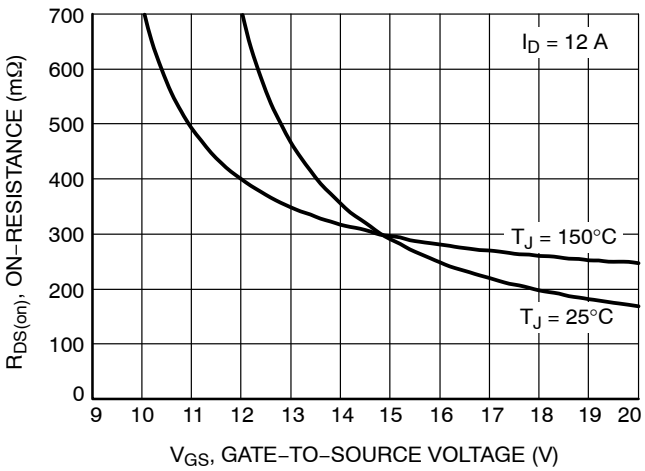


Figure 4. On−Resistance vs. Gate−to−Source Voltage

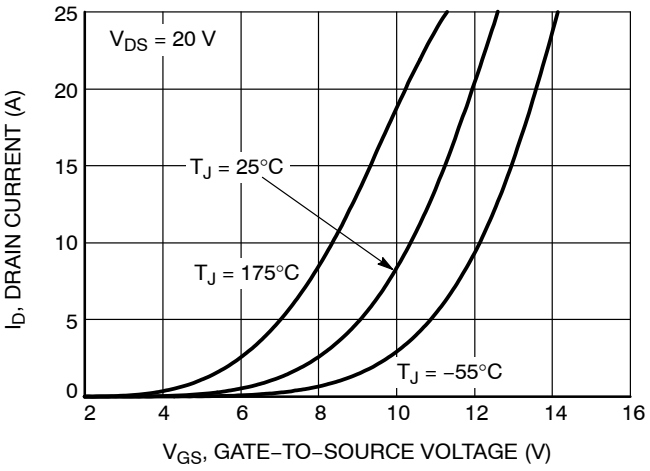


Figure 5. Transfer Characteristics

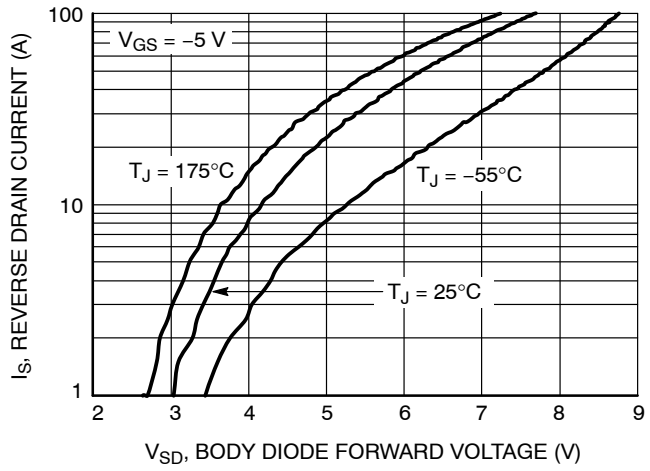


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (continued)

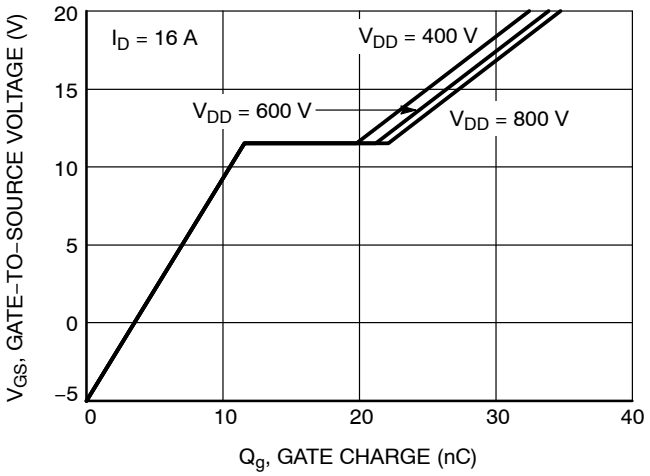


Figure 7. Gate−to−Source Voltage vs. Total Charge

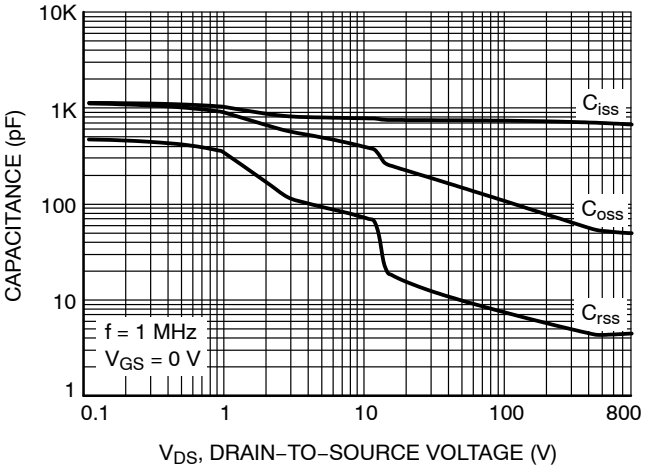


Figure 8. Capacitance vs. Drain−to−Source Voltage

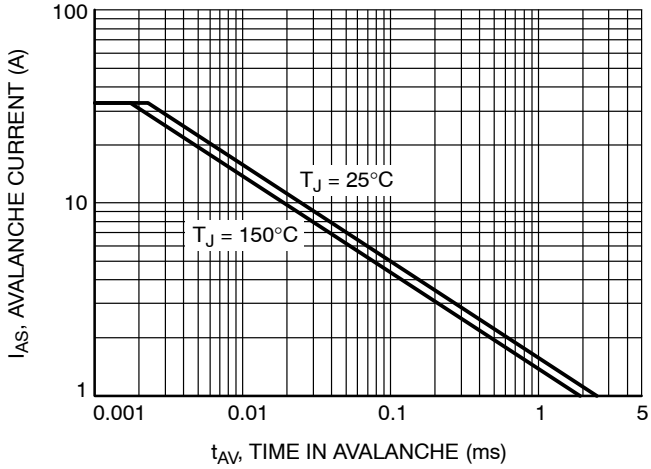


Figure 9. Unclamped Inductive Switching Capability

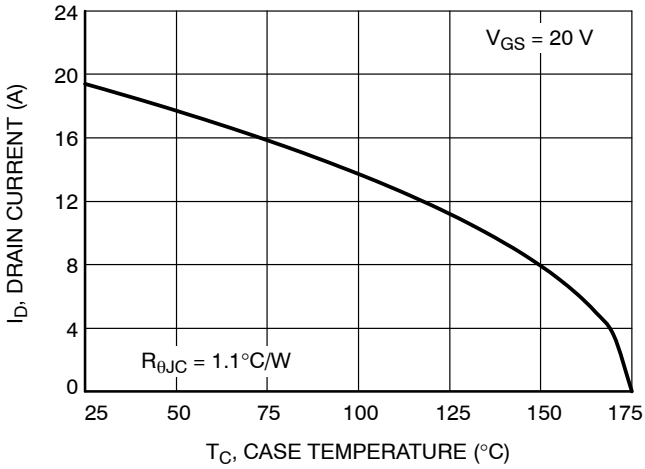


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

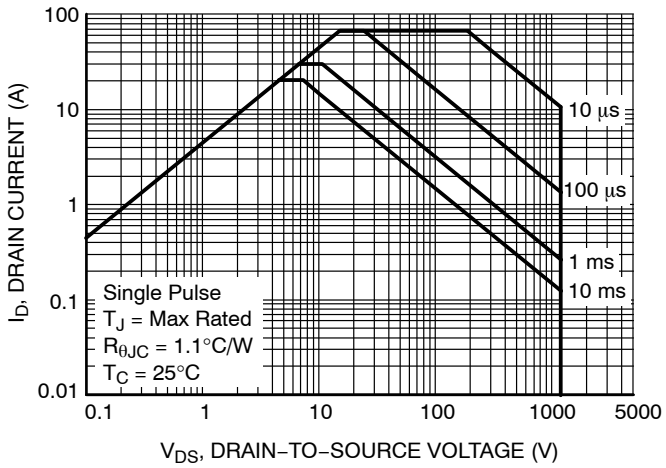


Figure 11. Safe Operating Area

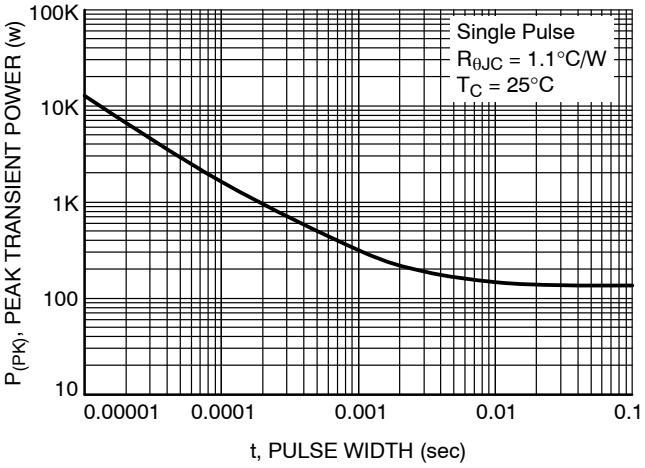


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

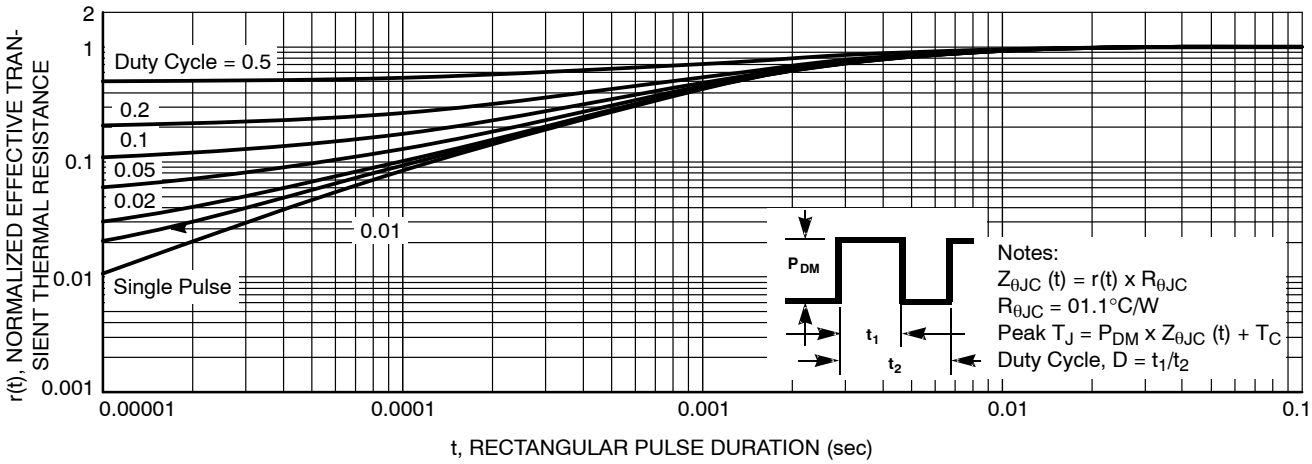
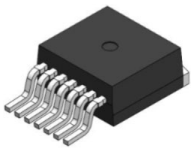
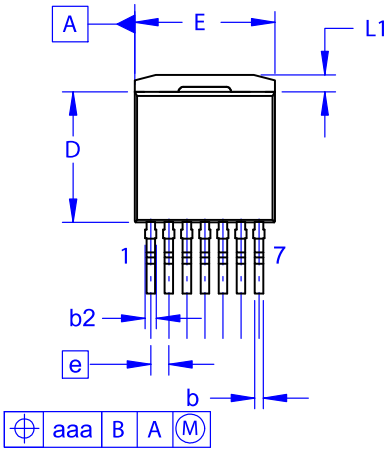


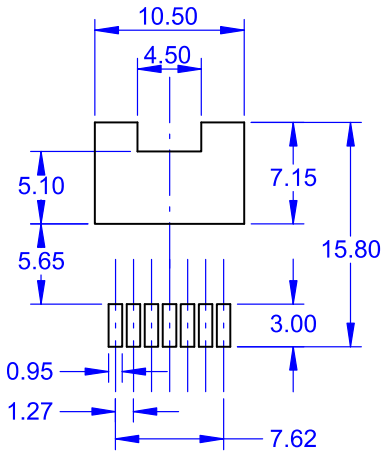
Figure 13. Junction−to−Ambient Transient Thermal Response Curve



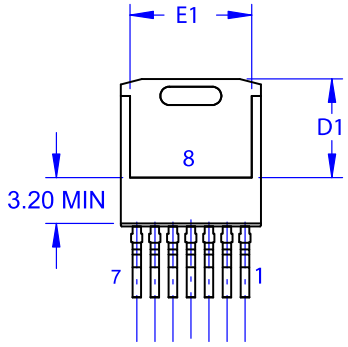
D²PAK7 (TO−263−7L HV)
CASE 418BJ
ISSUE B

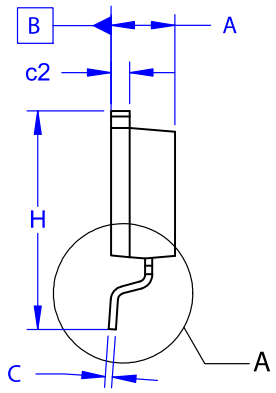
DATE 16 AUG 2019





LAND PATTERN RECOMMENDATION





NOTES:

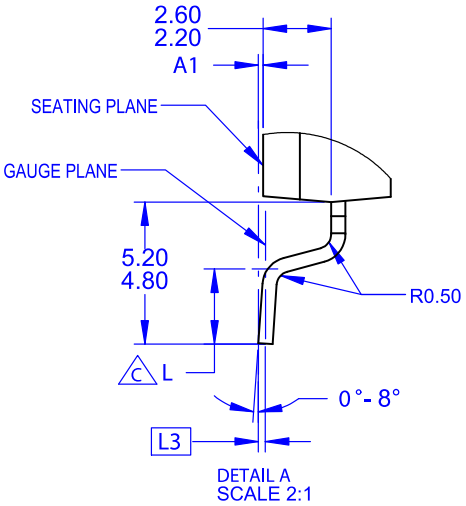
A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



DOCUMENT NUMBER:	**98AON84234G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**D²PAK7 (TO−263−7L HV)**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales