NTHD3101F

MOSFET – Power, P-Channel, Schottky Diode, ChipFET, FETKY, Schottky Barrier Diode

-20 V, -4.4 A, 4.1 A

Features

- Leadless SMD Package Featuring a MOSFET and Schottky Diode
- 40% Smaller than TSOP−6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Independent Pinout to each Device to Ease Circuit Design
- Trench P−Channel for Low On Resistance
- Ultra Low V_F Schottky
- Pb−Free Packages are Available

Applications

- Li−Ion Battery Charging
- High Side DC−DC Conversion Circuits
- High Side Drive for Small Brushless DC Motors
- Power Management in Portable, Battery Powered Products

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_J = 25°C	I_D	−3.2	A
		T_J = 85°C		−2.3	
	t ≤ 5 s	T_J = 25°C		−4.4	
Power Dissipation (Note 1)	Steady State	T_J = 25°C	P_D	1.1	W
	t ≤ 5 s			2.1	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−13	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	2.5	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

SCHOTTKY DIODE MAXIMUM RATINGS
(T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Units
Peak Repetitive Reverse Voltage	V_{RRM}	20	V
DC Blocking Voltage	V_R	20	V

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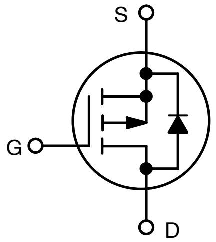
MOSFET

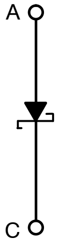
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	64 mΩ @ −4.5 V	−4.4 A
	85 mΩ @ −2.5 V	

SCHOTTKY DIODE

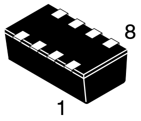
V_R MAX	V_F TYP	I_F MAX
20 V	0.510 V	4.1 A



P−Channel MOSFET

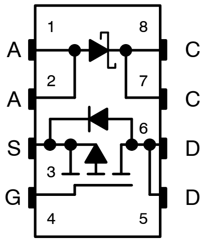


Schottky Diode

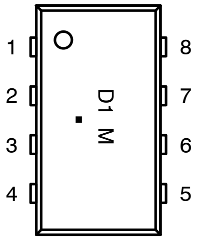


ChipFET
CASE 1206A
STYLE 3

PIN CONNECTIONS



MARKING DIAGRAM



D1 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

SCHOTTKY DIODE MAXIMUM RATINGS

(T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Units
Average Rectified Forward Current	Steady State	T_J = 25°C	I_F	2.2	V
	t ≤ 5 s			4.1	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	113	°C/W
Junction–to–Ambient – t ≤ 10 s (Note 2)	$R_{\theta JA}$	60	°C/W

2. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = –250 μA		–20			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				–15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –16 V, V_{GS} = 0 V	T_J = 25°C			–1.0	μA
			T_J = 125°C			–5.0	
Gate–to–Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = –250 μA		–0.45		–1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.7		mV/°C
Drain–to–Source On–Resistance	$R_{DS(on)}$	V_{GS} = –4.5, I_D = –3.2 A			64	80	mΩ
		V_{GS} = –2.5, I_D = –2.2 A			85	110	
		V_{GS} = –1.8, I_D = –1.0 A			120	170	
Forward Transconductance	g_{FS}	V_{DS} = –10 V, I_D = –2.9 A			8.0		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = –10 V			680		pF
Output Capacitance	C_{OSS}				100		
Reverse Transfer Capacitance	C_{RSS}				70		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = –4.5 V, V_{DS} = –10 V, I_D = –3.2 A			7.4		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.6		
Gate–to–Source Charge	Q_{GS}				1.4		
Gate–to–Drain Charge	Q_{GD}				2.5		
SWITCHING CHARACTERISTICS (Note 4)							
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = –4.5 V, V_{DD} = –10 V, I_D = –3.2 A, R_G = 2.4 Ω			5.8		ns
Rise Time	t_r				11.7		
Turn–Off Delay Time	$t_{d(OFF)}$				16		
Fall Time	t_f				12.4		
DRAIN–SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = –2.5 A	T_J = 25°C		–0.8	–1.2	V

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DRAIN−SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = −1.0 A , dI_S/dt = 100 A/μs		13.5		ns
Charge Time	t_a			9.5		
Discharge Time	t_b			4.0		
Reverse Recovery Charge	Q_{RR}			6.5		nC

SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Maximum Instantaneous Forward Voltage	V_F	I_F = 0.1 A		0.425		V
		I_F = 1.0 A		0.510	0.575	
Maximum Instantaneous Reverse Current	I_R	V_R = 10 V			1.0	μA
		V_R = 20 V			5.0	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL P−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

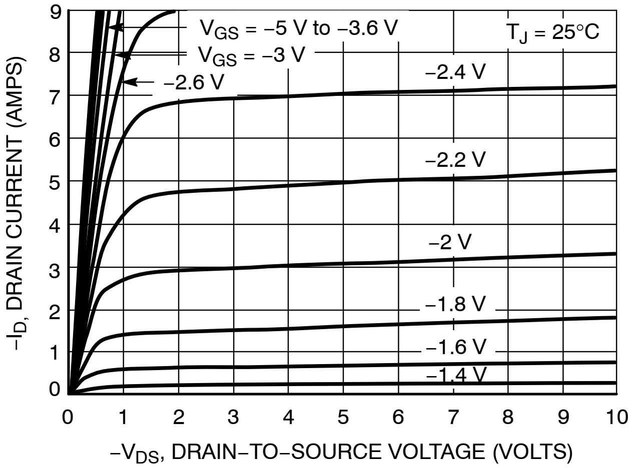


Figure 1. On−Region Characteristics

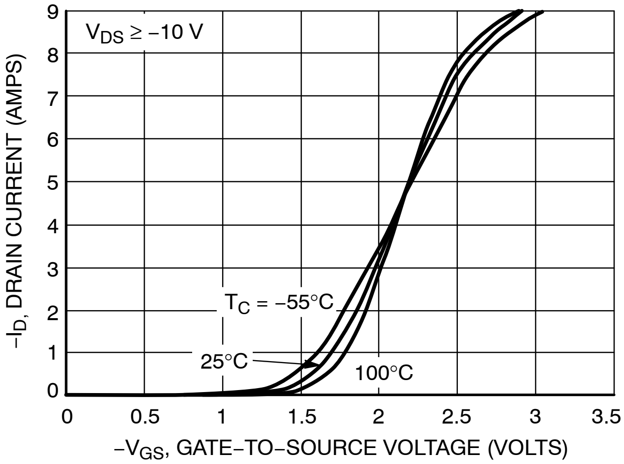


Figure 2. Transfer Characteristics

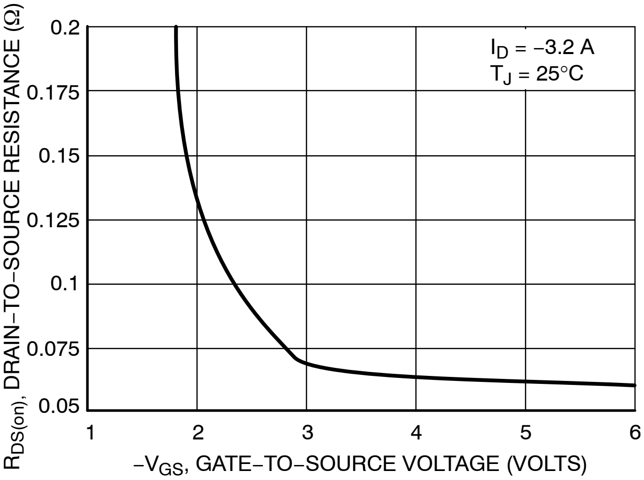


Figure 3. On−Resistance vs. Gate−to−Source Voltage

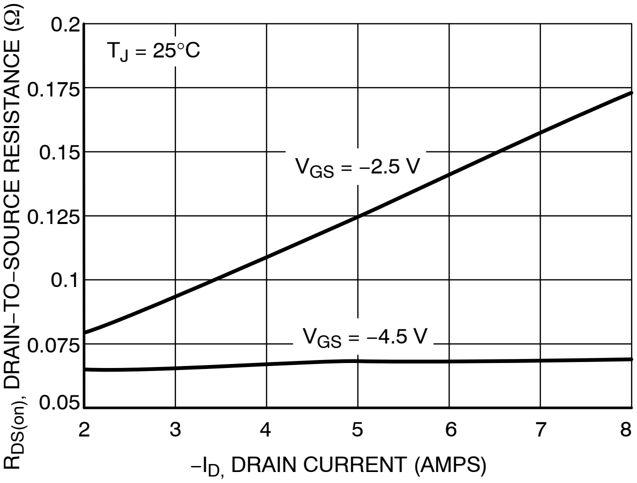


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

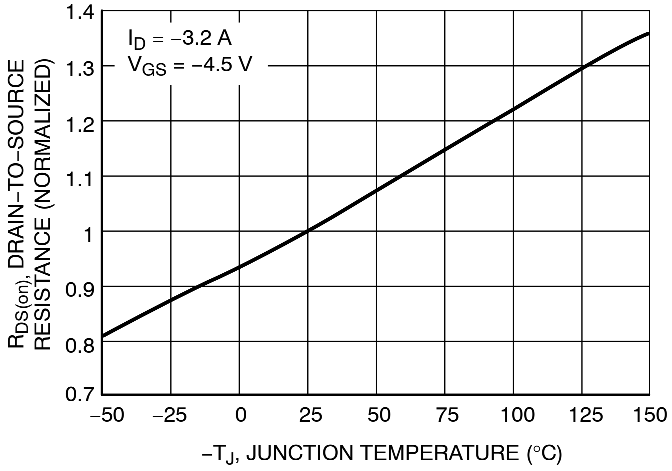


Figure 5. On−Resistance Variation with Temperature

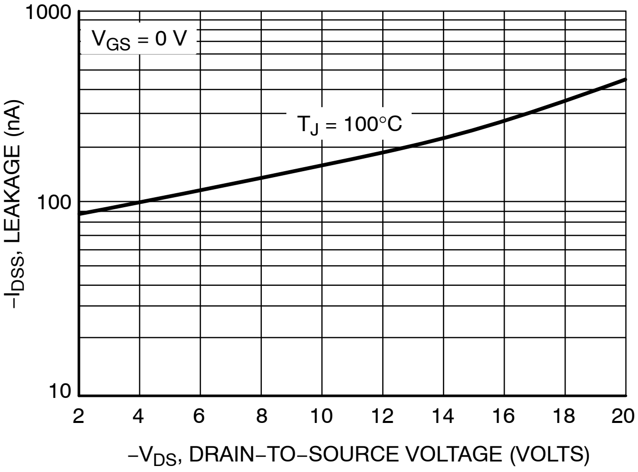


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL P−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

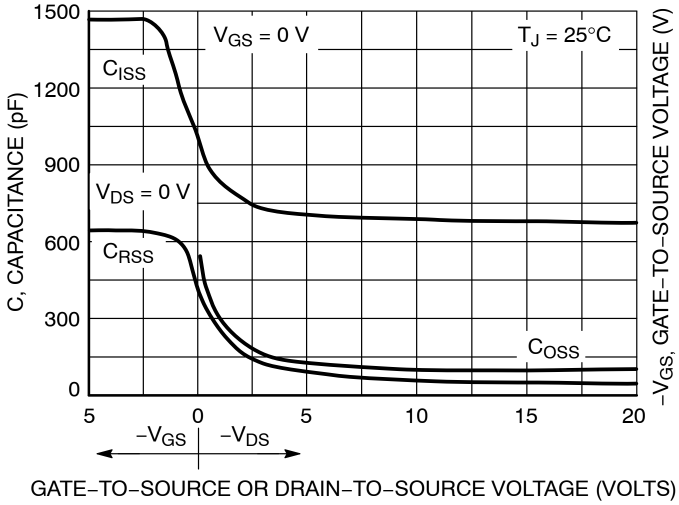


Figure 7. Capacitance Variation

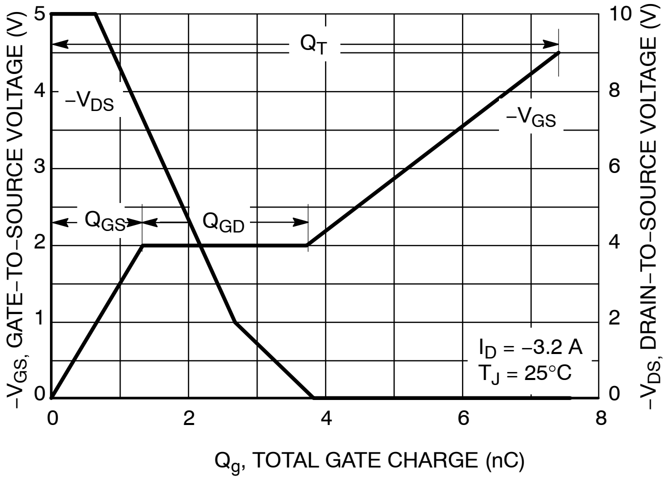


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

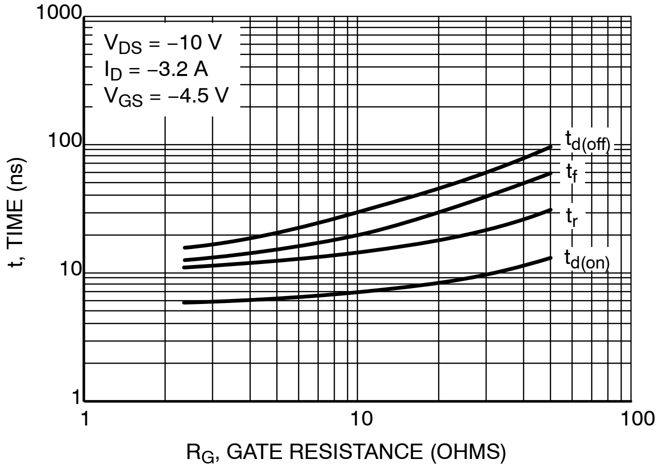


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

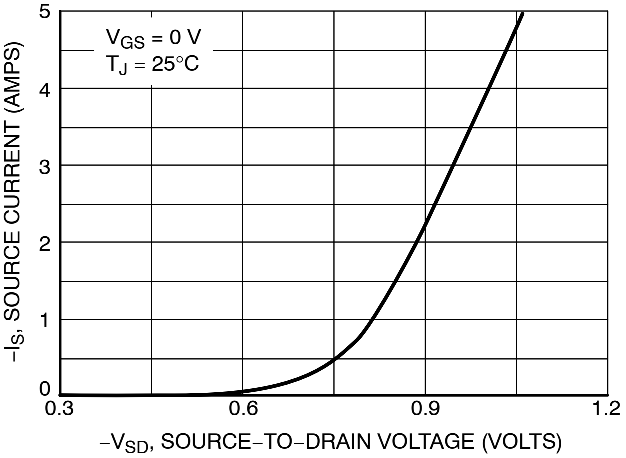


Figure 10. Diode Forward Voltage vs. Current

TYPICAL SCHOTTKY PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

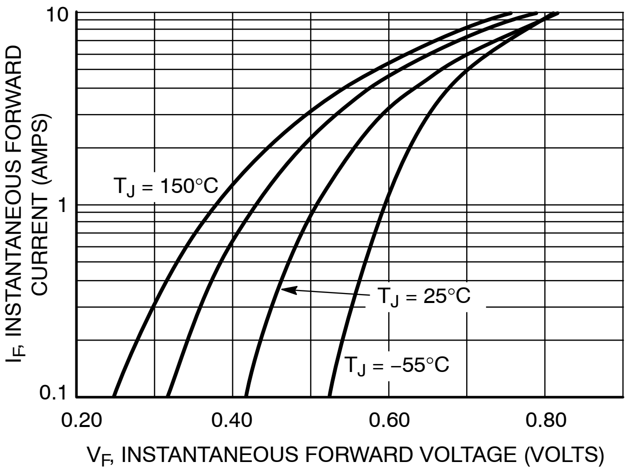


Figure 11. Typical Forward Voltage

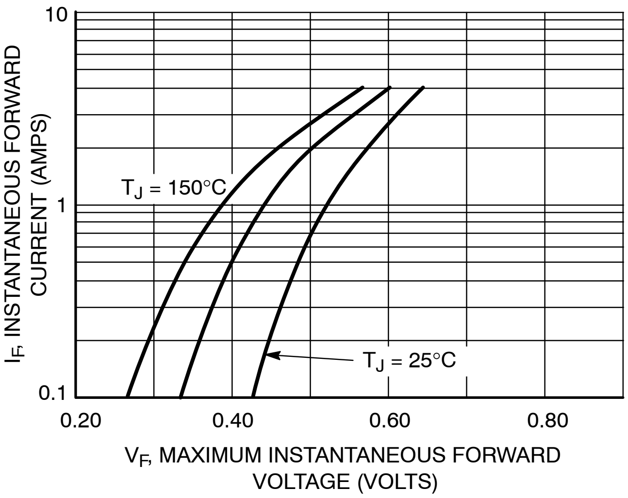


Figure 12. Maximum Forward Voltage

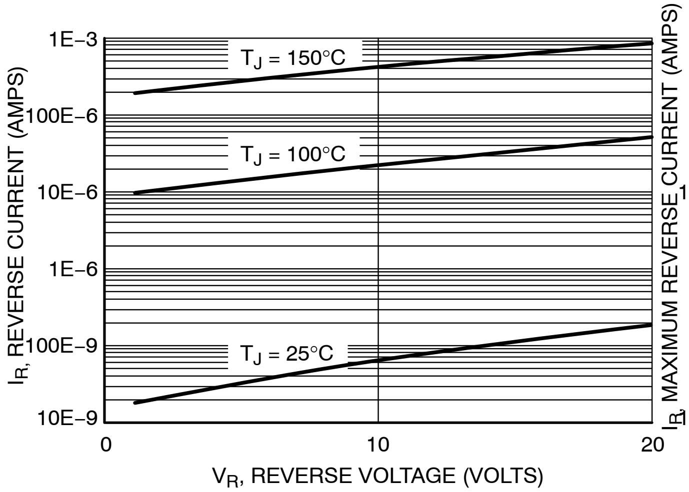


Figure 13. Typical Reverse Current

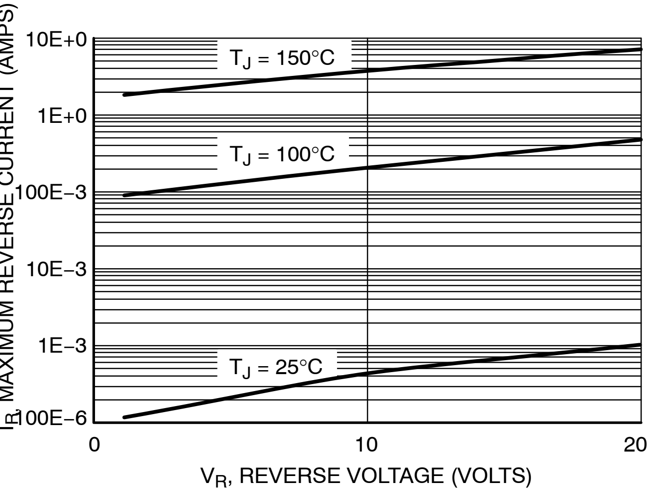


Figure 14. Maximum Reverse Current

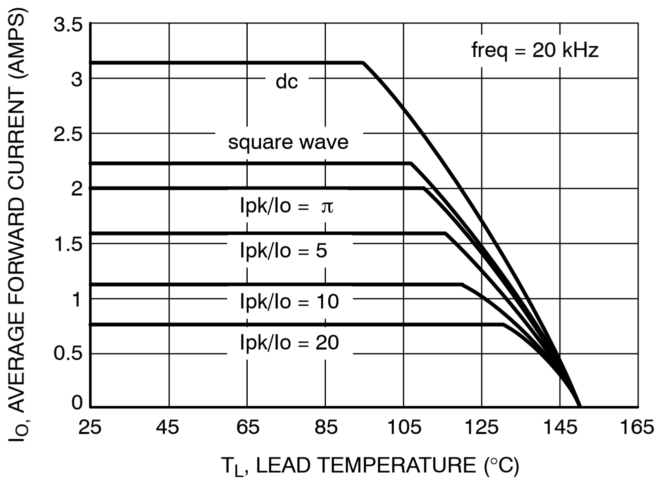


Figure 15. Current Derating

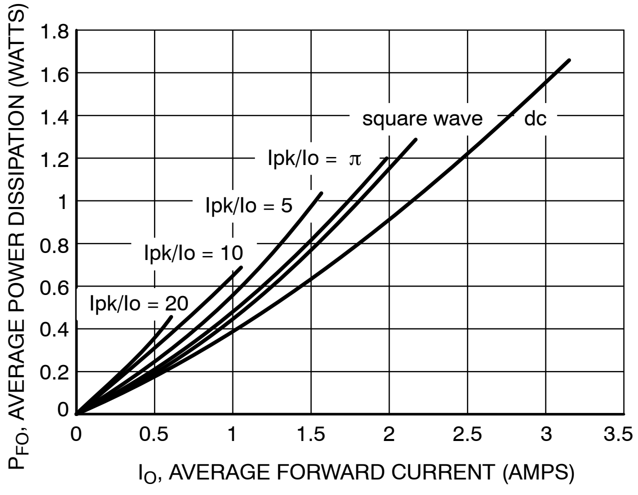


Figure 16. Forward Power Dissipation

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTHD3101FT1	ChipFET	3000 / Tape & Reel
NTHD3101FT1G	ChipFET (Pb−Free)	3000 / Tape & Reel
NTHD3101FT3	ChipFET	10000 / Tape & Reel
NTHD3101FT3G	ChipFET (Pb−Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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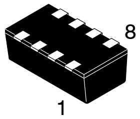
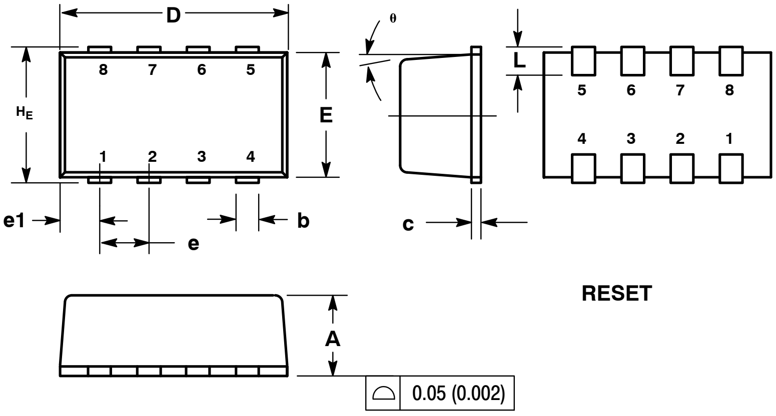
FETKY is a registered trademark of International Rectifier Corporation.



SCALE 1:1

ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

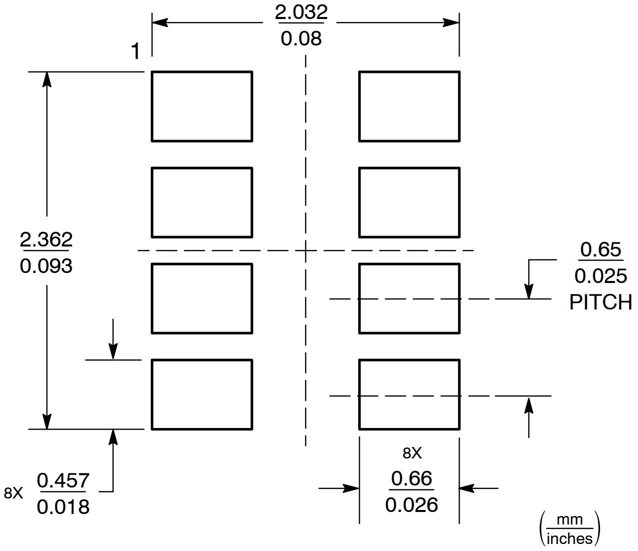
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

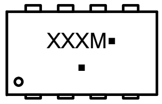
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

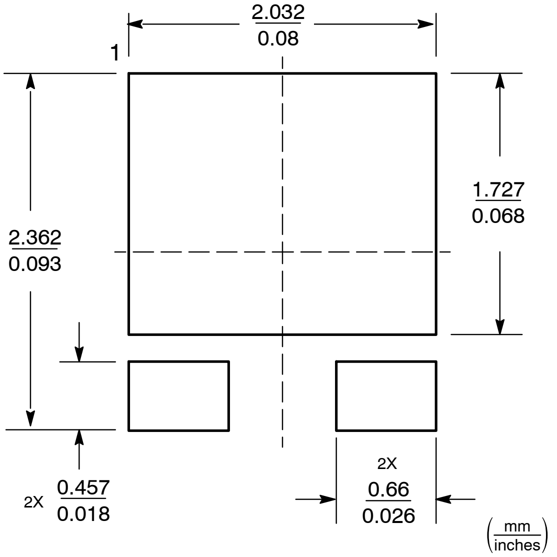
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

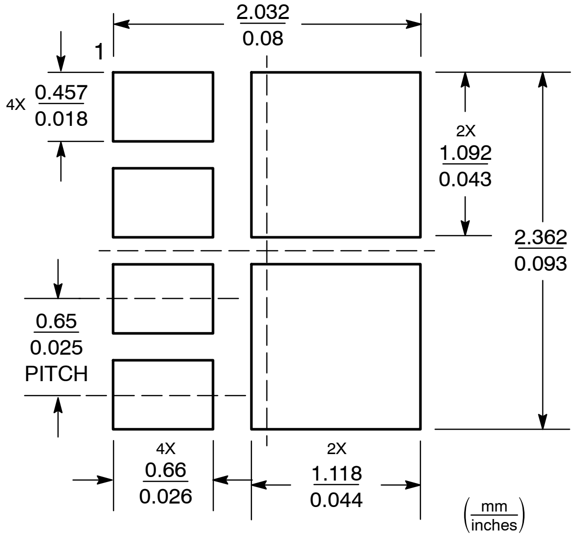
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

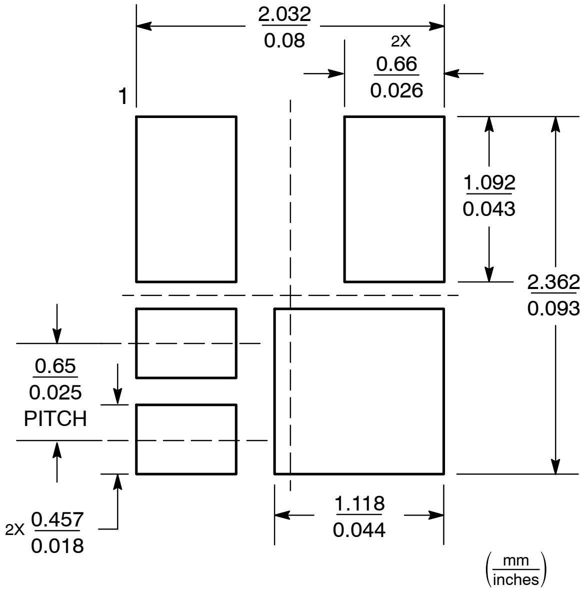
ADDITIONAL SOLDERING FOOTPRINTS*



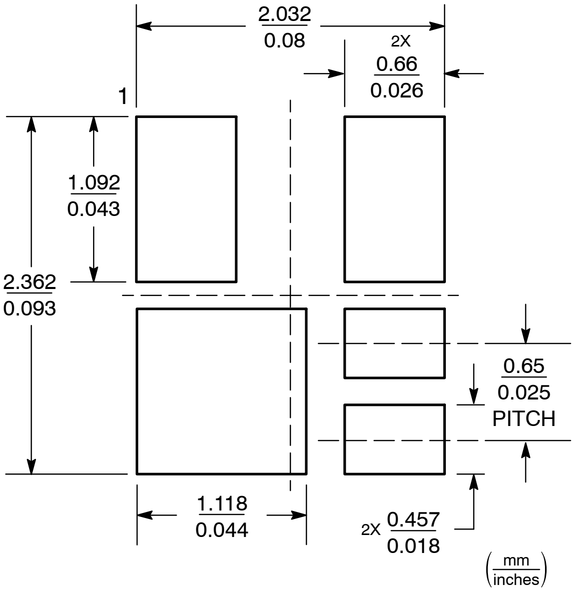
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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