

MOSFET – Power, Single P-Channel, WDFN6

-20 V

NTLJS7D2P02P8Z

Features

- Small Footprint (4 mm²) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

Applications

- Battery Management
- Protection
- Power Load Switch

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	−20	V
Gate-to-Source Voltage			V _{GS}	±8.0	V
Continuous Drain Current R _{θJA} (Notes 1, 3)	Steady State	T _A = 25 °C	I _D	−13.1	A
		T _A = 85 °C		−9.5	
Power Dissipation R _{θJA} (Notes 1, 3)		T _A = 25 °C	P _D	2.40	W
Continuous Drain Current R _{θJA} (Notes 2, 3)	Steady State	T _A = 25 °C	I _D	−7.9	A
		T _A = 85 °C		−5.7	
Power Dissipation R _{θJA} (Notes 2, 3)		T _A = 25 °C	P _D	0.86	W
Pulsed Drain Current	T _A = 25 °C, t _p = 10 μs		I _{DM}	52	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	−55 to +150	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

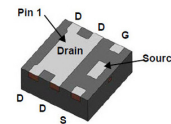
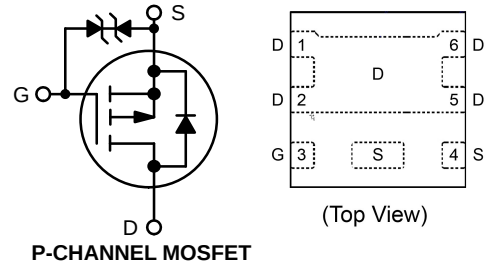
THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	R _{θJA}	52	°C/W
Junction-to-Ambient – Steady State (Note 2)	R _{θJA}	145	

1. Surface-mounted on FR4 board using 1 in² pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. R_{θCA} is determined by the user's board design.

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
-20 V	9 mΩ @ -4.5 V	-13.1 A
	11 mΩ @ -2.5 V	

ELECTRICAL CONNECTION



WDFN6 (2.05x2.05)
CASE 483AV

MARKING DIAGRAM



YW = Date Code
ZZ = Assembly Lot Code
A = Assembly Site Code
7D2 = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

NTLJS7D2P02P8Z

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\text{ }\mu\text{A}$, ref to $25\text{ }^{\circ}\text{C}$		14.4		mV/ $^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$	$T_J = 25\text{ }^{\circ}\text{C}$		-1	μA
			$T_J = 125\text{ }^{\circ}\text{C}$		-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			± 10	μA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	-0.4		-1.5	V
Threshold Temperature Coefficient	V_{GS}/T_J	$I_D = -250\text{ }\mu\text{A}$, ref to $25\text{ }^{\circ}\text{C}$		-3.3		mV/ $^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		7.1	9.0	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -5\text{ A}$		9.1	11	
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -10\text{ A}$		59		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -10\text{ V}, f = 1.0\text{ MHz}$		2790		pF
Output Capacitance	C_{oss}			412		
Reverse Transfer Capacitance	C_{rss}			369		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -10\text{ A}$		26.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.4		
Gate-to-Source Charge	Q_{GS}			3.7		
Gate-to-Drain Charge	Q_{GD}			6.7		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -15\text{ V}, I_D = -10\text{ A}, R_G = 6\text{ }\Omega$		9.3		ns
Rise Time	t_r			25.1		
Turn-Off Delay Time	$t_{d(off)}$			224		
Fall Time	t_f			130		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -10\text{ A}$	$T_J = 25\text{ }^{\circ}\text{C}$		0.74	1.2	V
			$T_J = 125\text{ }^{\circ}\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = -100\text{ A}/\mu\text{s}, I_S = -10\text{ A}$			20		ns
Reverse Recovery Charge	Q_{RR}				5.4		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.



TYPICAL CHARACTERISTICS

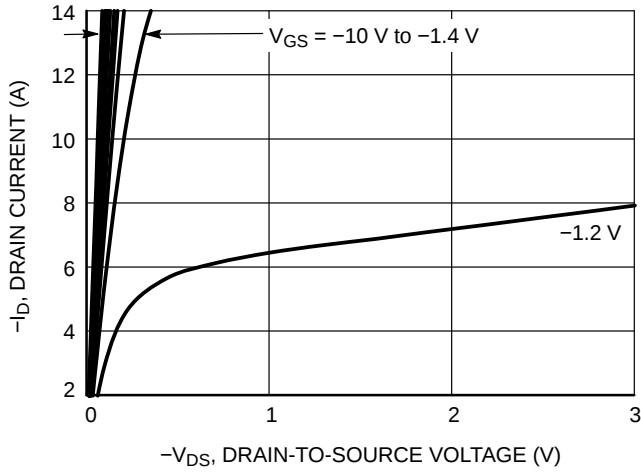


Figure 1. On-Region Characteristics

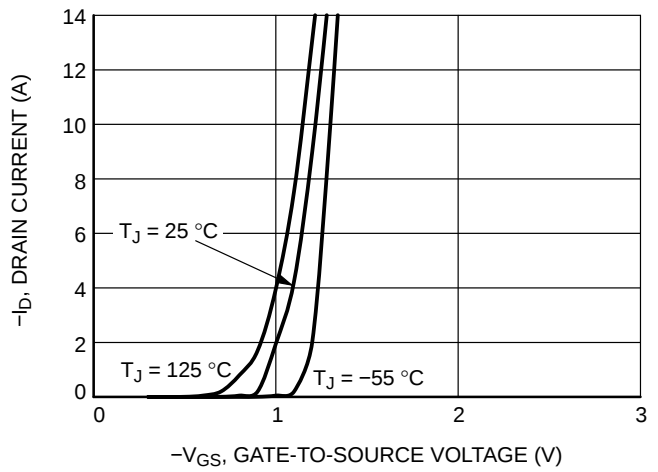


Figure 2. Transfer Characteristics

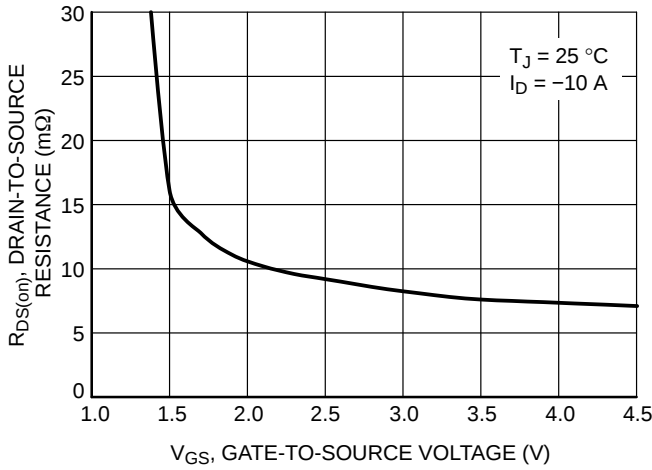


Figure 3. On-Resistance vs. Gate-to-Source Voltage (V)

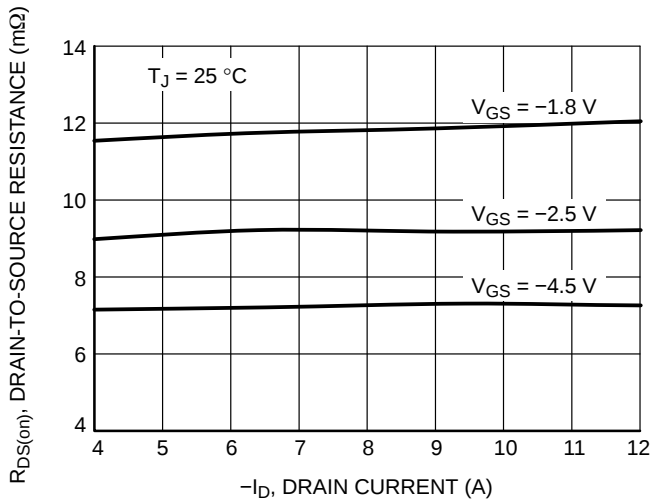


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

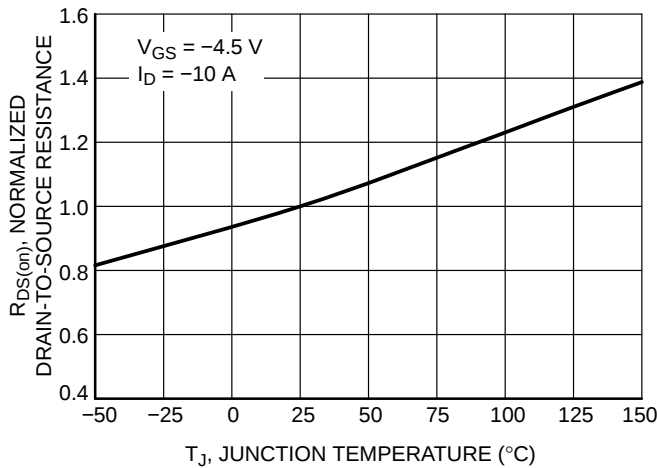


Figure 5. On-Resistance Variation with Temperature

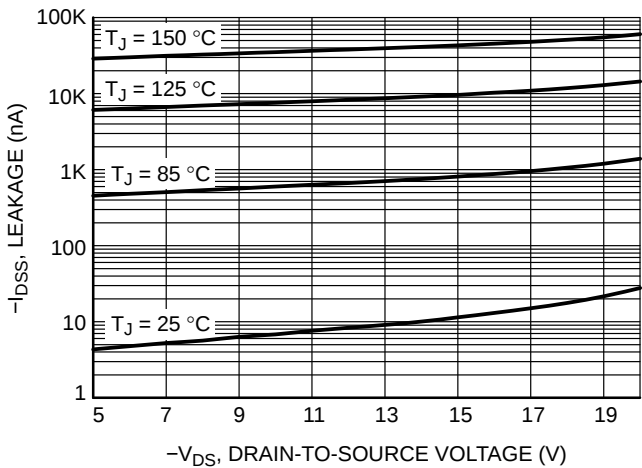


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

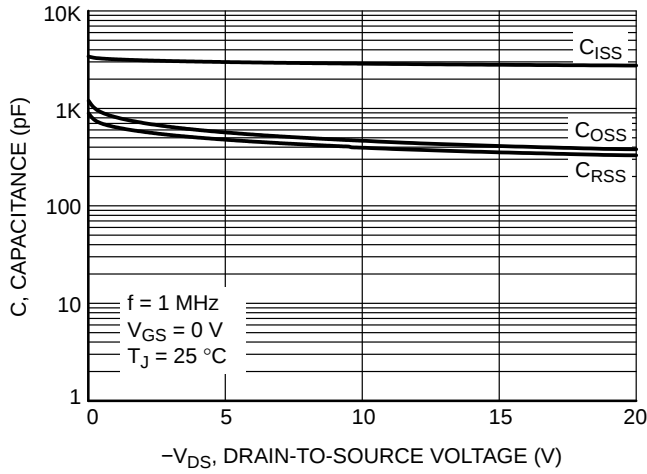


Figure 7. Capacitance Variation

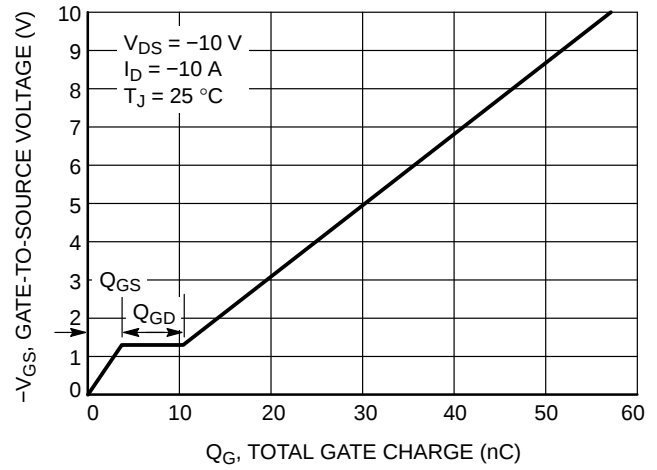


Figure 8. Gate-to-Source vs. Total Charge

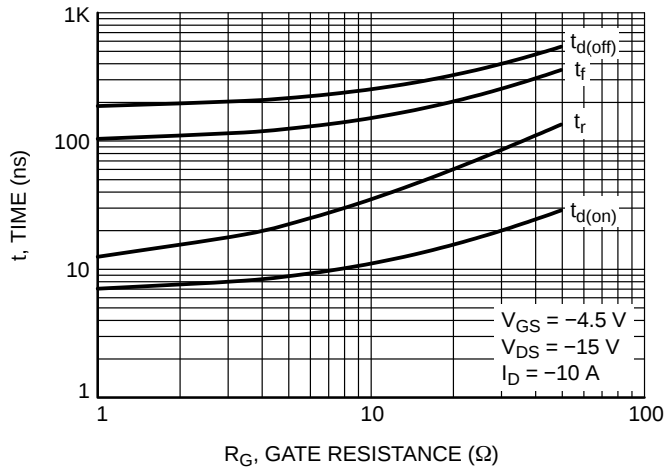


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

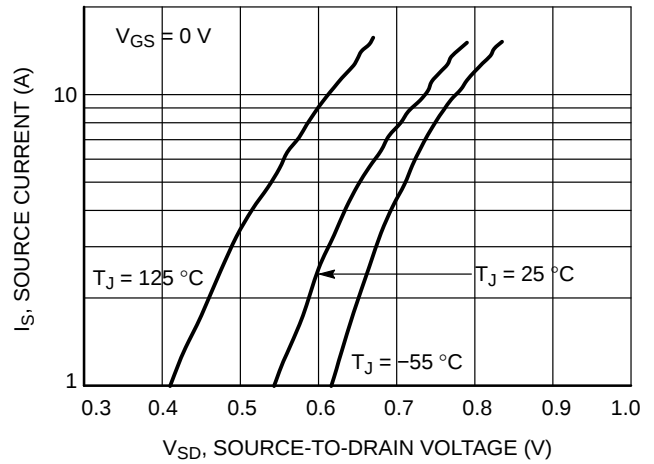


Figure 10. Diode Forward Voltage vs. Current

DEVICE ORDERING INFORMATION

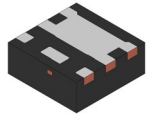
Device	Package	Shipping [†]
NTLJS7D2P02P8ZTAG	WDFN6 (Pb-Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

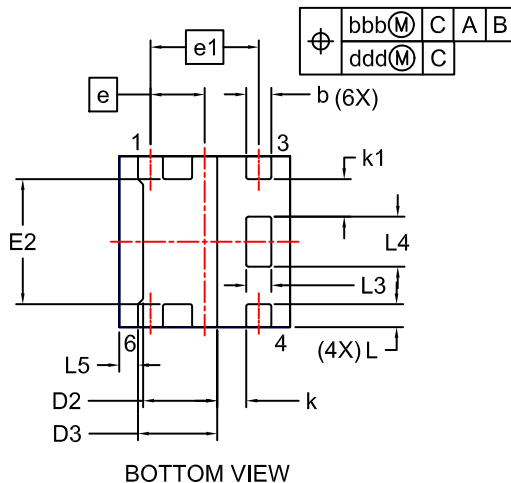
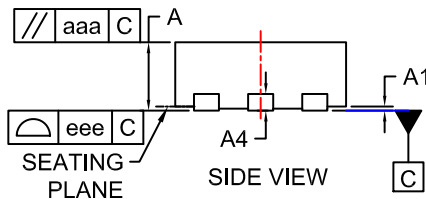
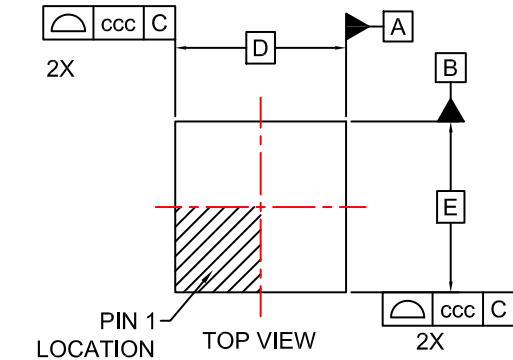
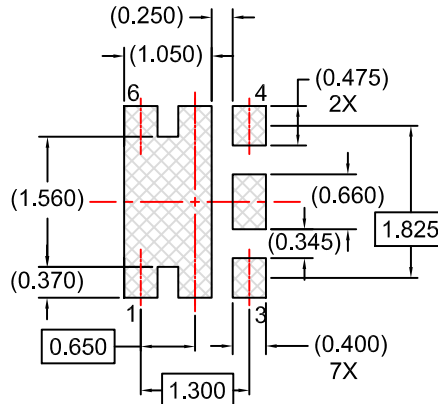
REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	8/14/2020
1	Rebranded the document to onsemi format.	1/27/2026




WDFN6 2.05X2.05, 0.65P
CASE 483AV
ISSUE A

DATE 02 APR 2019


LAND PATTERN RECOMMENDATION

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4	(0.20)		
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3	(0.95)		
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e	0.65 BSC		
e1	1.30 BSC		
k	(0.35)		
k1	(0.45)		
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5	(0.23)		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		
eee	0.05		

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