

MOSFET – Power, Single, N-Channel

100 V, 4.8 mΩ, 132 A



ON Semiconductor®

www.onsemi.com

NTMFS6B03N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	100	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D 132	A
		$T_C = 100^\circ\text{C}$	83	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	P_D 165	W
		$T_C = 100^\circ\text{C}$	65	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 19	A
		$T_A = 100^\circ\text{C}$	12	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D 3.4	W
		$T_A = 100^\circ\text{C}$	1.4	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} 470	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	160	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 60 \text{ A}$)	E_{AS}	180	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

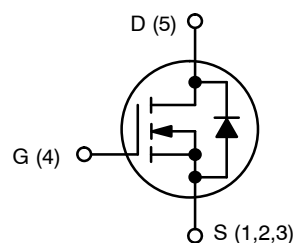
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.76	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	38	

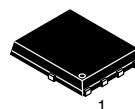
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	4.8 mΩ @ 10 V	132 A

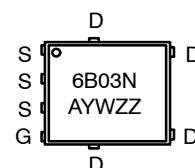


N-CHANNEL MOSFET

MARKING DIAGRAM



DFN5 (SO-8FL)
CASE 506EZ



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			67.3		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-8.1		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	3.8	4.8	m Ω
		$V_{GS} = 6.0\text{ V}$	$I_D = 10\text{ A}$	6.0	7.8	

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		4200		pF
Output Capacitance	C_{OSS}			760		
Reverse Transfer Capacitance	C_{RSS}			31		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 50\text{ A}$		58		nC
Threshold Gate Charge	$Q_{G(TH)}$			6.2		
Gate-to-Source Charge	Q_{GS}			19		
Gate-to-Drain Charge	Q_{GD}			17		
Plateau Voltage	V_{GP}			5.4		V
Gate Resistance	R_G	$T_J = 25^\circ\text{C}$		1.0		Ω

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 50\text{ A}, R_G = 1.0\ \Omega$		16		ns
Rise Time	t_r			46		
Turn-Off Delay Time	$t_{d(OFF)}$			29		
Fall Time	t_f			11		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$	0.9	1.2	V
			$T_J = 125^\circ\text{C}$	0.8		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 25\text{ A}$		67		ns
Charge Time	t_a			35		
Discharge Time	t_b			31		
Reverse Recovery Charge	Q_{RR}			120		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

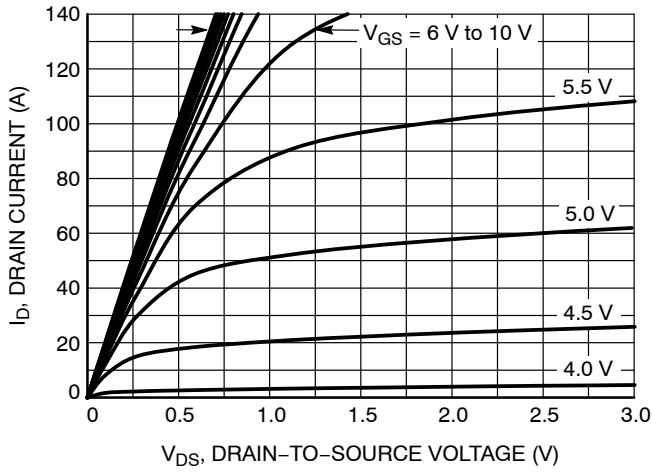


Figure 1. On-Region Characteristics

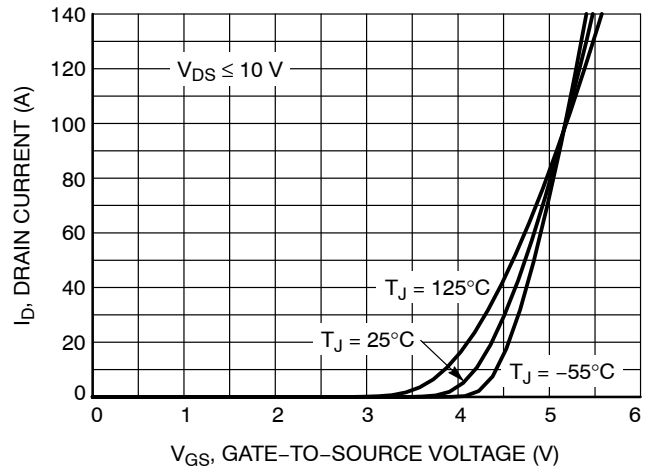


Figure 2. Transfer Characteristics

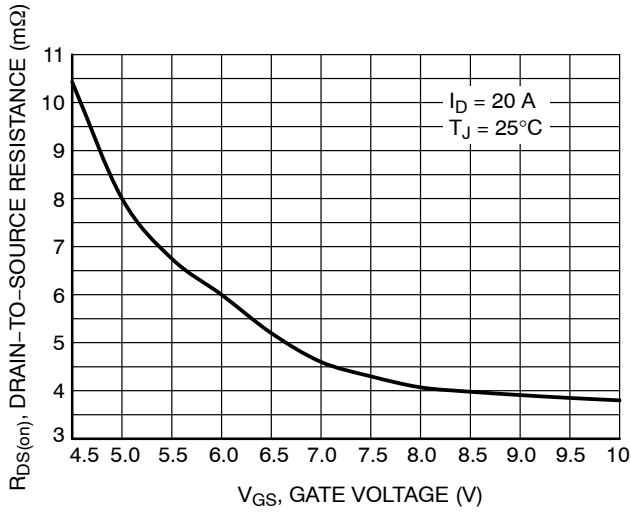


Figure 3. On-Resistance vs. Gate-to-Source Voltage

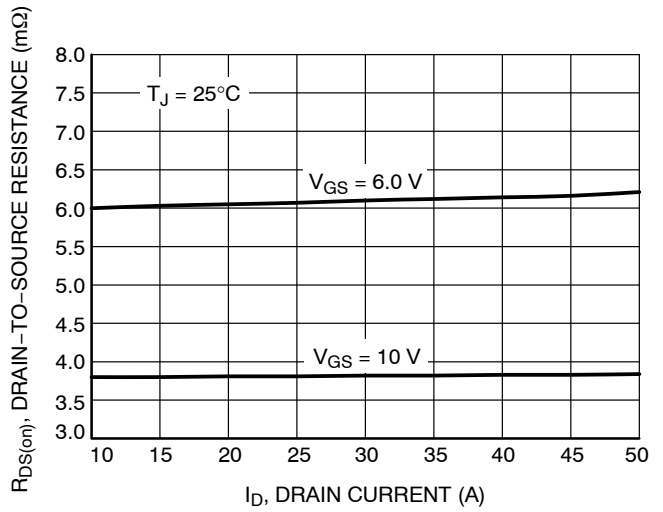


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

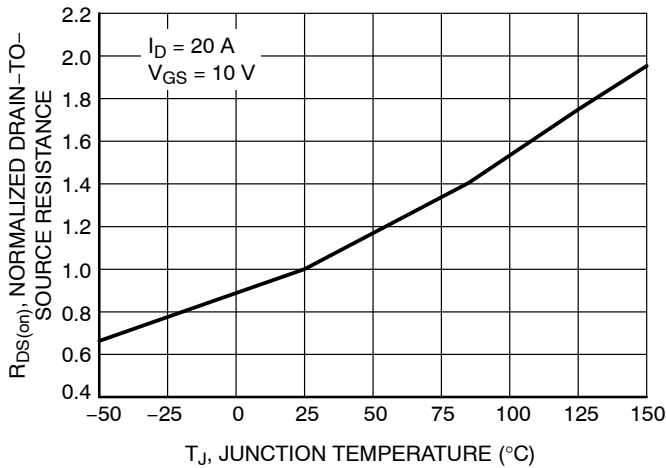


Figure 5. On-Resistance Variation with Temperature

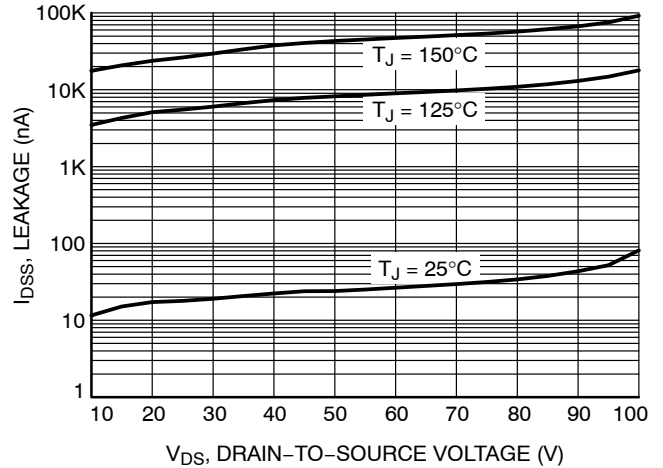


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

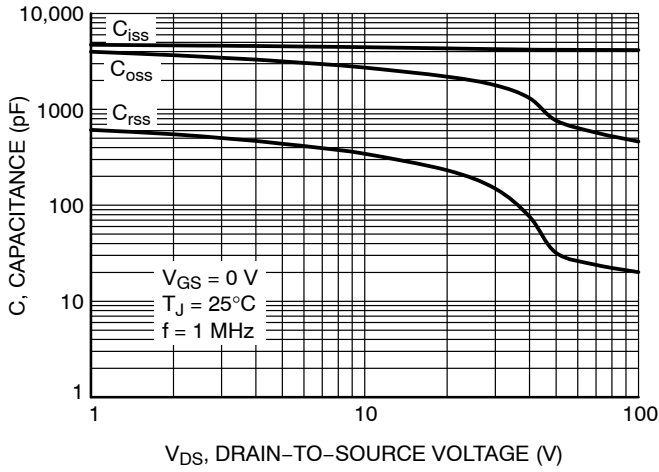


Figure 7. Capacitance Variation

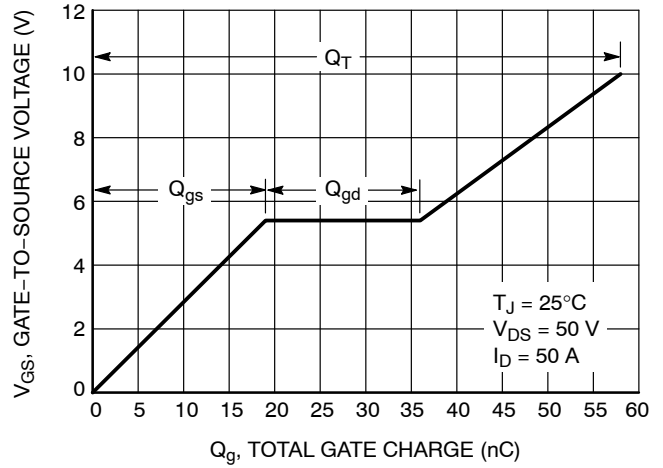


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

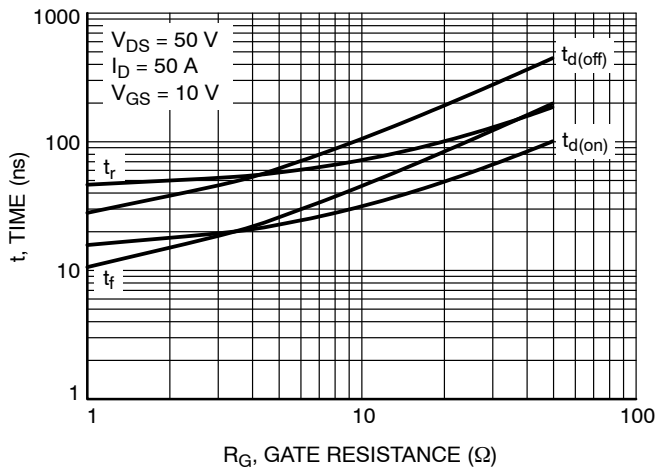


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

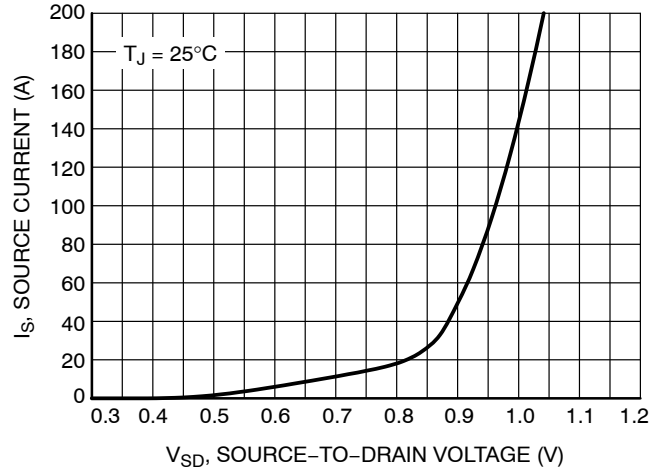


Figure 10. Diode Forward Voltage vs. Current

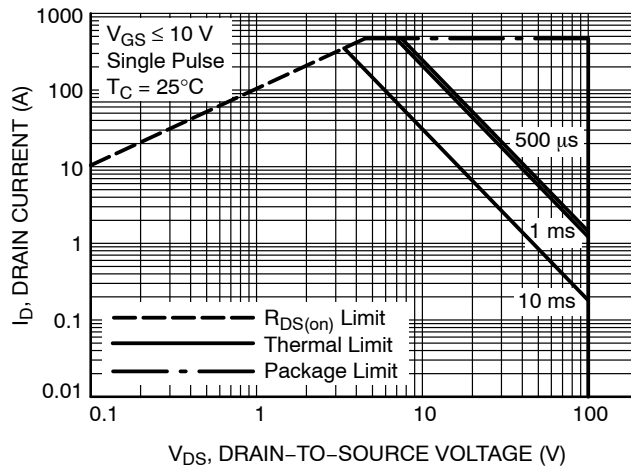


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

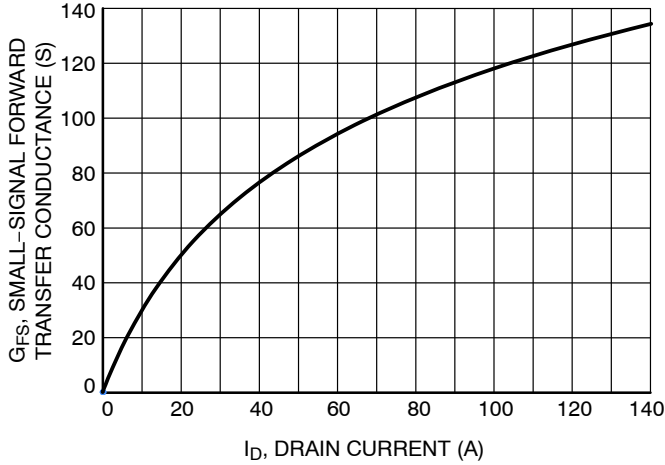


Figure 12. G_{FS} vs. I_D

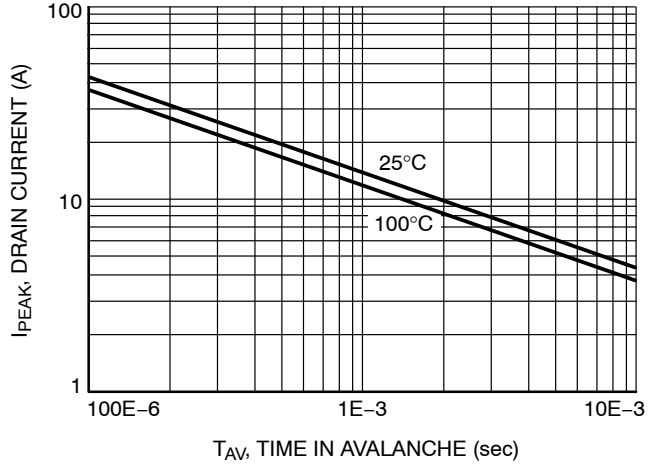


Figure 13. I_{PEAK} vs. T_{AV}

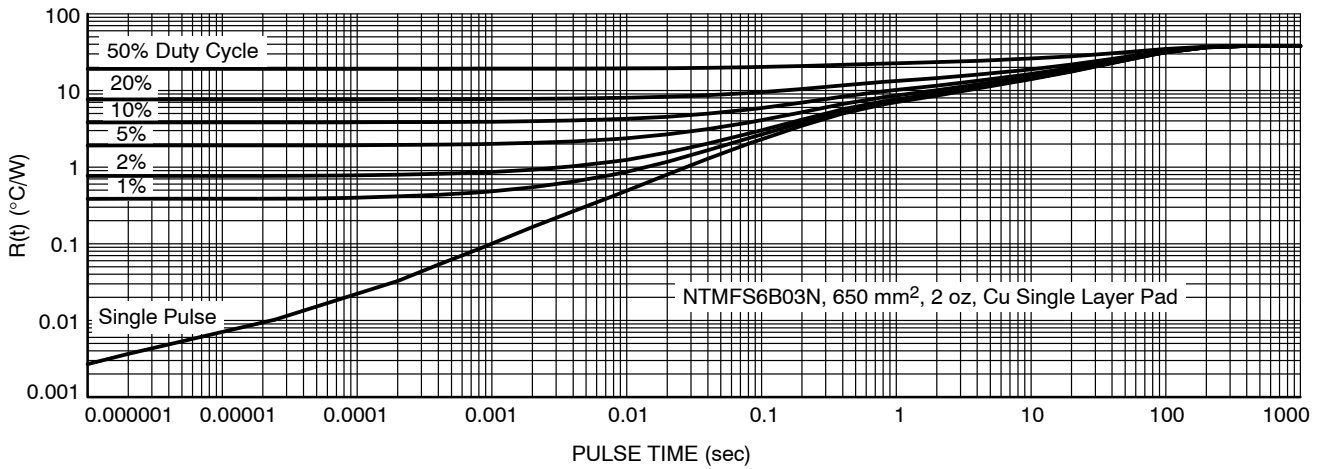


Figure 14. Thermal Response

DEVICE ORDERING INFORMATION

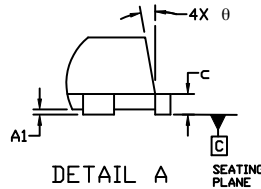
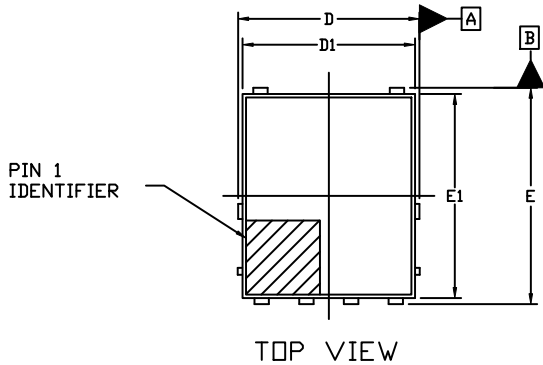
Device	Marking	Package	Shipping†
NTMFS6B03NT1G	6B03N	DFN5 (Pb-Free)	1500 / Tape & Reel
NTMFS6B03NT3G	6B03N	DFN5 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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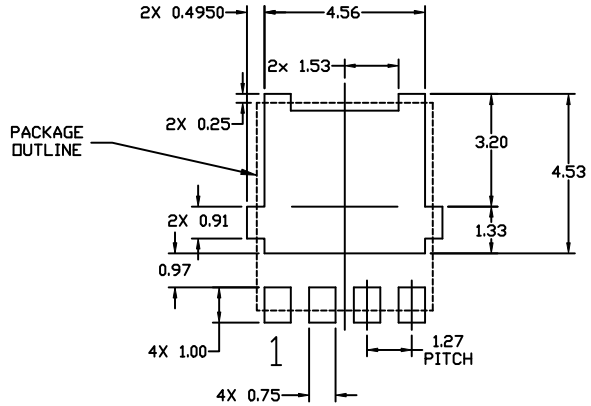
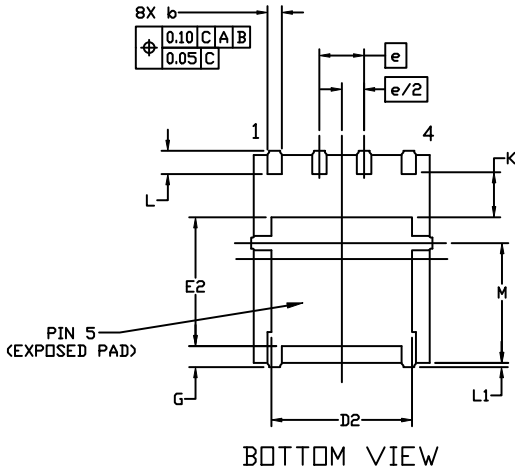
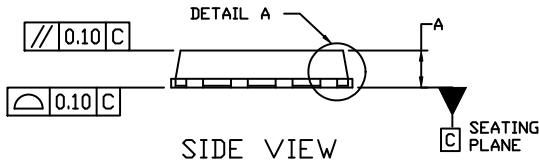
PACKAGE DIMENSIONS

DFN5 5x6, 1.27P (SO-8FL)
CASE 506EZ
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	1.25 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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